PROBLEM SOLUTIONS CHAPTER 4

SOLUTION 4.1. First, find V_{out} / V_s for each circuit. Then solve for R knowing $V_{out} = \sqrt{P\ 10} = \pm 14.142V$.

(a) Writing KCL at the inverting terminal, $1/1k(v_- - v_s) = 1/\ R(V_{out} - v_-)$ $V_{out} / V_s = -R/1k$, since the inverting terminal is a virtual short. Solving for $R = -V_{out}\ \ 1k / V_s = 2.828k\Omega$.

(b) Writing KCL at the inverting terminal, $V_s /1.5k = (V_{out} - V_s)/\ R$ $V_{out} / V_s = R/1.5k + 1$, solving for $R = 1.5k(V_{out} / V_s - 1) = 2.743k\Omega$.

(c) From (a) $V_{out} / V_s = -12k / R$, thus $R = -12k\ \ V_s / V_{out} = 4.243k\Omega$.

(d) This is the same circuit as (b) except the output voltage is taken across two resistors. Thus $V_{out} = \sqrt{\frac{P}{10}}(10 + 6) = 22.627V$. Using the general form from (b), $R = 400\left(V_{out} / V_s - 1\right) = 1.410k\Omega$

SOLUTION 4.2. (a) First, find the voltage at the non-inverting terminal as $v_+ = 1/\ 2\ \ V_s$. Then write KCL at the inverting terminal, and make use of the virtual short property,

$(V_s / 2)/10k = (V_{out} - V_s / 2) / 30k$ $V_{out} / V_s = 30k(1/\ 20k + 1/\ 60k) = 2$.

(b) Relating the output of the amplifier to the output of the circuit, $V_{out} = V_{amp}(500 / 800)$. Then writing KCL at the inverting terminal, $V_s / 400 = (V_{amp} - V_s) /1.2k$ $V_{amp} / V_s = 1.2k / 400 + 1 = 4$. Therefore $V_{out} / V_s = (V_{amp} / V_s)\ \ (V_{out} / V_{amp}) = 2.5$.

(c) Note that since no current goes into the non-inverting terminal of the op-amp, the voltage at that node is $-V_s$. KCL at the inverting terminal, $-V_s / 4k = (V_{out} + V_s)/\ 20k$ $V_{out} / V_s = -6$.

SOLUTION 4.3. Write KCL for both terminals,

$(V_- - V_i)/1k = (V_o - V_-) / 2k$

$V_- /1k = (V_o - V_-)/\ 3k$

Solving and doing the appropriate substitutions, $V_o / V_i = -8$.

SOLUTION 4.4. This is essentially the basic inverting configuration, which is defined as $V_o / V_i = -2k / 1k = -2$.

SOLUTION 4.5. (a) By voltage division $V_L = 1V\ \frac{100}{200} = 0.5V$. Using Ohm's law

$I_s = I_L = \frac{1}{100+100} = 5mA$.

(b) No current flows in the input terminal of an ideal op-amp, thus $I_s = 0A$ and $V_L = 1V$. From Ohm's law $I_a = I_L = V_L/100 = 10mA$.

SOLUTION 4.6. (a) Using voltage division,

$$V_1 = V_s\left(\frac{32||(8+24)}{[32||(8+24)]+8}\right) = \frac{2}{3}V_s$$

$$V_{out} = V_1\left(\frac{24}{24+8}\right) = 0.5V_s$$

(b) By voltage division,

$$V_1 = V_s\left(\frac{32}{32+40}\right) = 0.8V_s$$

$$V_{out} = V_1\left(\frac{24}{24+8}\right) = 0.6V_s$$

(c) Using voltage division, $V_1 = V_s\left(\frac{32}{32+8}\right) = 0.8V_s$, as no current enters the non-inverting terminal of the op-amp. Due to the virtual short property, $V_{out} = V_1\left(\frac{24}{24+8}\right) = 0.6V_1$. This is indeed the same results as (b), which should be expected because of the isolation provided by the ideal buffers.

SOLUTION 4.7. Write KCL at the inverting terminal,

$-V_{s1}/1k - V_{s2}/2k = V_{out}/4k \qquad V_{out} = -4V_{s1} - 2V_{s2} = 40mV$.

SOLUTION 4.8. (a) The voltage at the non-inverting terminal is $V_+ = 3/2V$, KCL at the inverting terminal gives $(1.5-2.5)/10k = (V_{out}-1.5)/30k \qquad V_{out} = -1.5V$. The power is

$P = V_{out}^2/500 = 4.5mW$.

(b) The voltage at the non-inverting terminal is 3V this time, thus KCL

$(3-2.5)/10k = (V_{out}-3)/30k \qquad V_{out} = 4.5V$. The power is $P = V_{out}^2/500 = 40.5mW$.

SOLUTION 4.9. (a) Define the point between the two op-amp as V_{int}. Observe that the first op-amp is in the basic inverting configuration, and the second the non-inverting configuration. By inspection,

$V_{\text{int}} / V_s = -R_1 / 1k$

$V_{out} / V_{\text{int}} = (1 + R_2 / 1k)$

Cascading the two stages, $(V_{\text{int}} / V_s)(V_{out} / V_{\text{int}}) = V_{out} / V_s = -R_1 / 1k(1 + R_2 / 1k)$. Solving for $R_1 = 20 \;\; 1k / (1 + R_2 / 1k) = 5k\Omega$. The power absorbed is $P = (20 \;\; 0.5)^2 / 8 = 12.5W$.

(b) Using the same equations as (a), solve for $R_2 = (20 \;\; 1k / 2k - 1)1k = 9k\Omega$.

(c) Rewriting the equation obtained in (a), $R_1^2 + 1kR_1 - 20M = 0$, and solving the quadratic equation yields $R_1 = R_2 = 4k\Omega$.

SOLUTION 4.10. This is a cascade of two non-inverting configuration op-amp of the form $V_o / V_s = (1 + 10k / 10k)$ for each. Therefore $2 \;\; 2 = 4$.

SOLUTION 4.11. This system is made up of a non-inverting stage with a gain of 1+10k/10k, a voltage divider of gain 8k/(2k+8k), and a second non-inverting stage of gain 1+10k/10k. The product of all three yields $V_{out} / V_{in} = (2)(0.8)(2) = 3.2$.

SOLUTION 4.12. (a) By inspection, the gain of the first stage is –1. Then write KCL for the second stage $V_{s1} / 2R - V_{s2} / R = V_{out} / 2R \qquad V_{out} = V_{s1} - 2V_{s2} = 10V$.

(b) The first stage gain is –0.5, thus $V_{out} = 2R(0.5V_{s1}) / 2R - 2R(V_{s2}) / \; 0.5R = -7.5V$, using the same procedure as in (a).

SOLUTION 4.13. (a) This is a cascade of a summing amplifier with the following transfer characteristic, $V_o = -4V_{s1} - 2V_{s2}$, and an inverting stage of gain –1.5. Thus $V_{out} = 1.5(4V_{s1} + 2V_{s2}) = 2.25V$.

(b) Notice that the only difference is the gain of the inverting stage, which is now –2. Therefore $V_{out} = 2(4V_{s1} + 2V_{s2}) = 3V$.

SOLUTION 4.14. This circuit is a cascade of two summing amplifier where the output of the first is an input of the second stage. The transfer function of the first stage is $V_o = -2RV_{s1} / 2R - 2RV_{s2} / R$, which is substituted in the transfer function of the second stage to obtain $V_{out} = -R[-2RV_{s1} / 2R - 2RV_{s2} / R] / \; R - RV_{s3} / R = V_{s1} + 2V_{s2} - V_{s3} = -2V$.

SOLUTION 4.15. Writing KCL at the inverting node, $-V_1 / R_1 - V_2 / R_2 - V_3 / R_3 = V_{out} / R_f$, and solving for $V_{out} = -\left(\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3\right)$.

SOLUTION 4.16. Referring figure P4.15, the value of the resistance must satisfy the following constraints: $R_1 = R_2 = R_3 = 3R$, $R_f = R$

These will yield the inverted average. If polarity is a concern, a second inverting stage should be added with a unity gain, i.e. both R's equal.

SOLUTION 4.17. Using the topology of 4.12 the following parameters are chosen,

$G_{a1} = 3,\ G_{a2} = 5,\ G_{b1} = 2,\ G_{b2} = 4$

For the time being assume $G_f = 1$. Now we calculate $\delta = (1+3+5) - (2+4) = 3$, this sets $G_g = 3$.

(a) The requirement for $G_f = 10\mu S$ sets the scaling factor $K = 10\mu / 1 = 10\mu$. This then yields the following set of parameters,

$G_{a1} = 30\mu S,\ G_{a2} = 50\,\mu S,\ G_{b1} = 20\mu S,\ G_{b2} = 40\mu S,\ G_f = 10\mu S,\ G_g = 30\mu S$

(b) The requirement for $G_f = 2\mu S$, sets the scaling constant to 2uS. So the following parameters are obtained:

$G_{a1} = 6\mu S,\ G_{a2} = 10\,\mu S,\ G_{b1} = 4\,\mu S,\ G_{b2} = 8\mu S$

Furthermore for $G_g = 12\mu S$, $\Delta G = 6\mu S$ in order to make the incident conductance equal at both terminal.

(c) Using the starting values from (a), one could choose a scaling constant of 5 μS. This will yield the following resistances:

$R_{a1} = 66.67k\Omega,\ R_{a2} = 40k\Omega,\ R_{b1} = 100k\Omega,\ R_{b2} = 50k\Omega,\ R_f = 200k\Omega,\ R_g = 66.67k\Omega$

These are all reasonable values for circuit implementation.

SOLUTION 4.18. (a) Choosing the following initial values:

$G_{a1} = 3S,\ G_{a2} = 5S,\ G_{b1} = 11S,\ G_{b2} = 4S,\ G_f = 1S$

then calculate $\delta = (1+3+5)-(11+4) = -6$. Thus $G_g = 1S$, and $\Delta G = 1+6 = 7S$. Scaling everything by 1μS, yield this final set of parameters, which meet the requirements.

$$G_{a1} = 3\mu S,\ G_{a2} = 5\mu S,\ G_{b1} = 11\mu S,\ G_{b2} = 4\mu S,\ G_f = 1\mu S,\ G_g = 1\mu S,\ \Delta G = 7uS$$

(b) The set of parameters remains unchanged, except for ΔG which now becomes 6uS in order to maintain the equal termination conductance requirement due to $G_g = 0S$.

(c) Scale the initial parameters of (a) by 5uS, and get the following set of resistances:

$$R_{a1} = 66.67k\Omega,\ R_{a2} = 40k\Omega,\ R_{b1} = 18.18k\Omega,\ R_{b2} = 50k\Omega,\ R_f = 200k\Omega,\ R_g = 200k\Omega,\ \Delta R = 28.57k\Omega$$

SOLUTION 4.19. (a) Choosing the following initial set of parameters:

$$R_{a1} = 1/(4S) = 0.25\Omega,\ R_{a2} = 1/(2S) = 0.5\Omega,\ R_{b1} = 1/(5S) = 1/5\Omega,\ R_{b2} = 1/(4S) = 0.25\Omega,\ R_f = 1\Omega$$

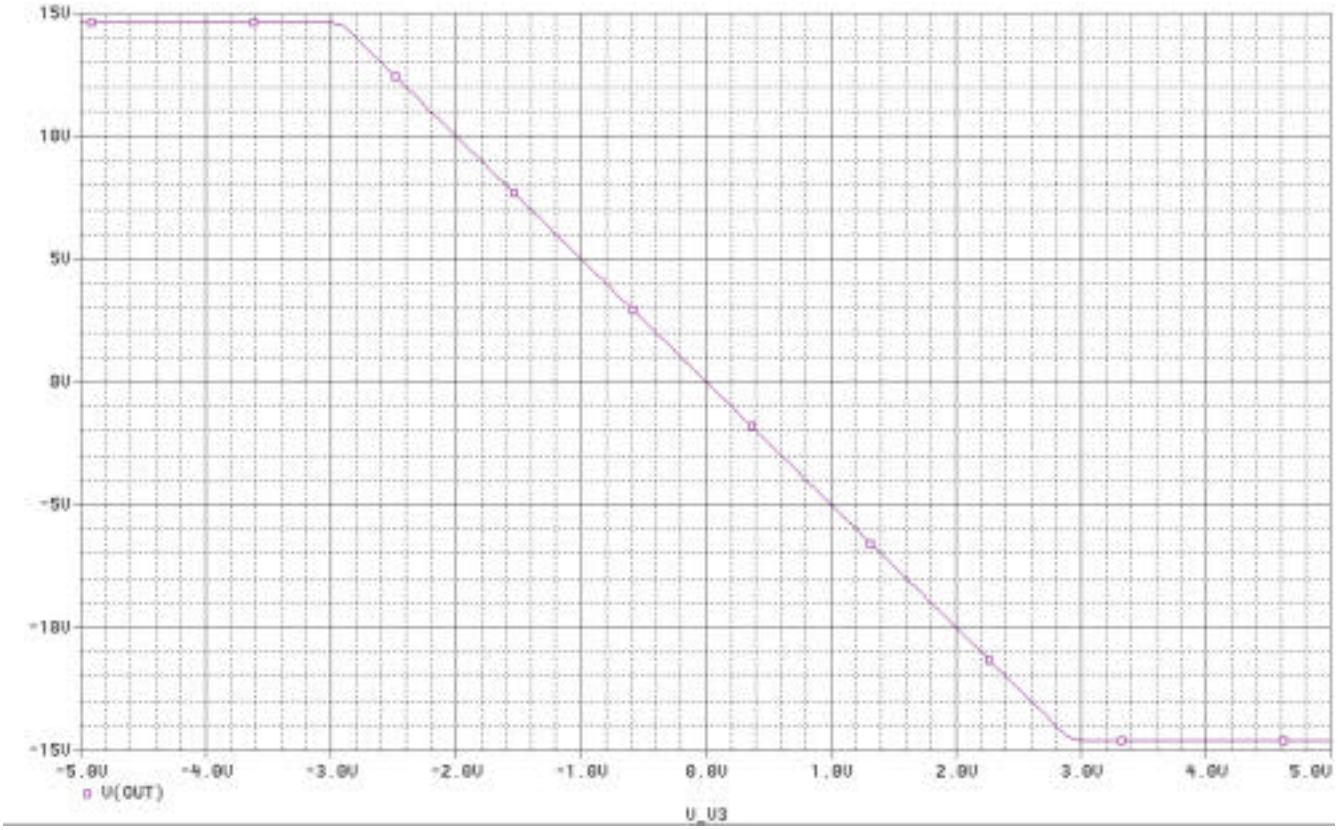
and $\delta = (1+4+2)-(5+4) = -2$, thus choose $R_g = 1/(1S) = 1\Omega$ and $\Delta R = 1/(1+2) = 1/3\Omega$. To meet the $R_f = 50k\Omega$ requirement, all the parameters must be scaled by 50k, which gives

$$R_{a1} = 12.5k\Omega,\ R_{a2} = 25k\Omega,\ R_{b1} = 10k\Omega,\ R_{b2} = 12.5k\Omega,\ R_f = 50k\Omega,\ R_g = 50k\Omega,\ \Delta R = 16.67k\Omega$$

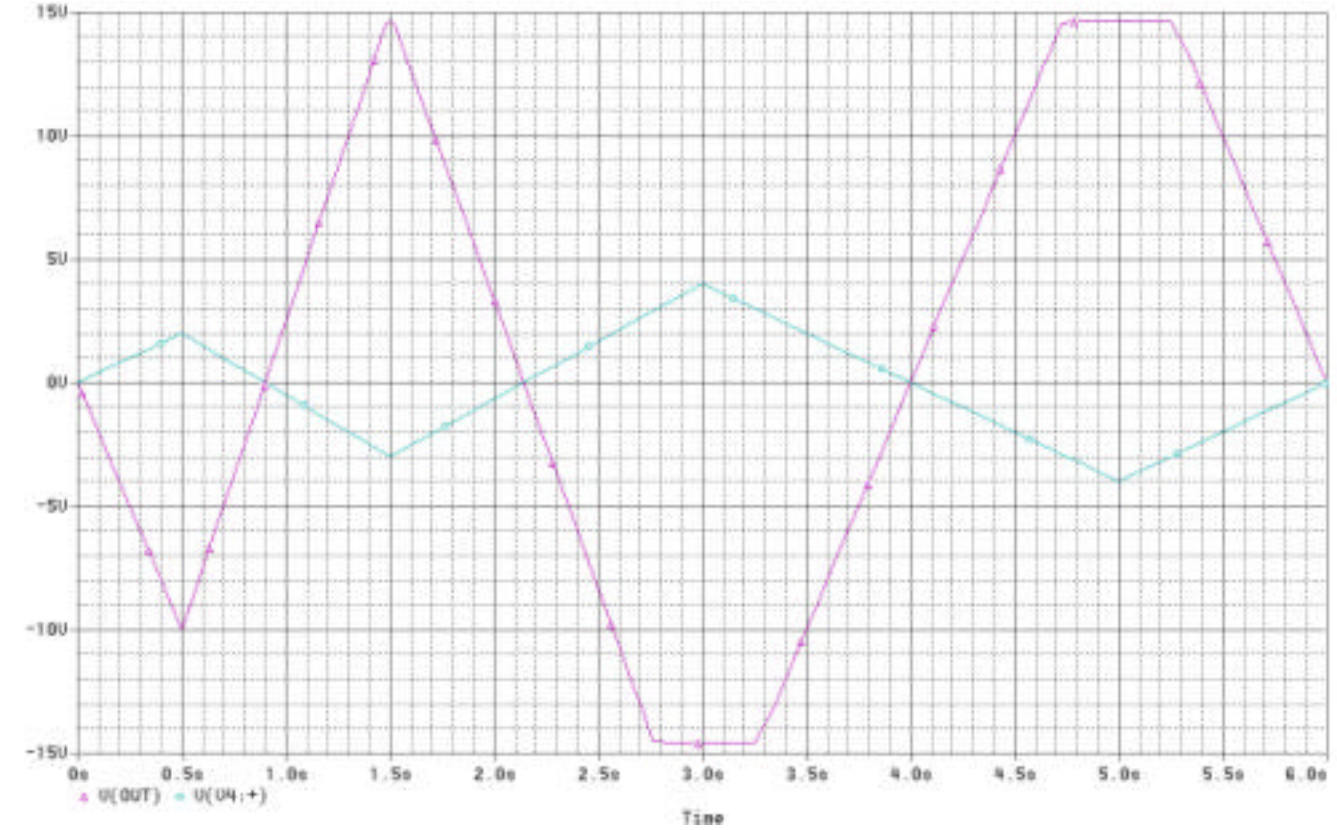
(b) Same as (a) with a 100k scaling constant:

$$R_{a1} = 25k\Omega,\ R_{a2} = 50k\Omega,\ R_{b1} = 20k\Omega,\ R_{b2} = 25k\Omega,\ R_f = 100k\Omega,\ R_g = 100k\Omega,\ \Delta R = 33.33k\Omega$$

SOLUTION 4.20. (a) When the op-amp is in its active region $v_{out}/v_s = -5$. Thus it will operate in its active region when $-3 \le v_s \le 3$, and will saturate at 15V when $v_s \le -3$, and at –15V when $v_s \ge 3$. SPICE yield the following plot:

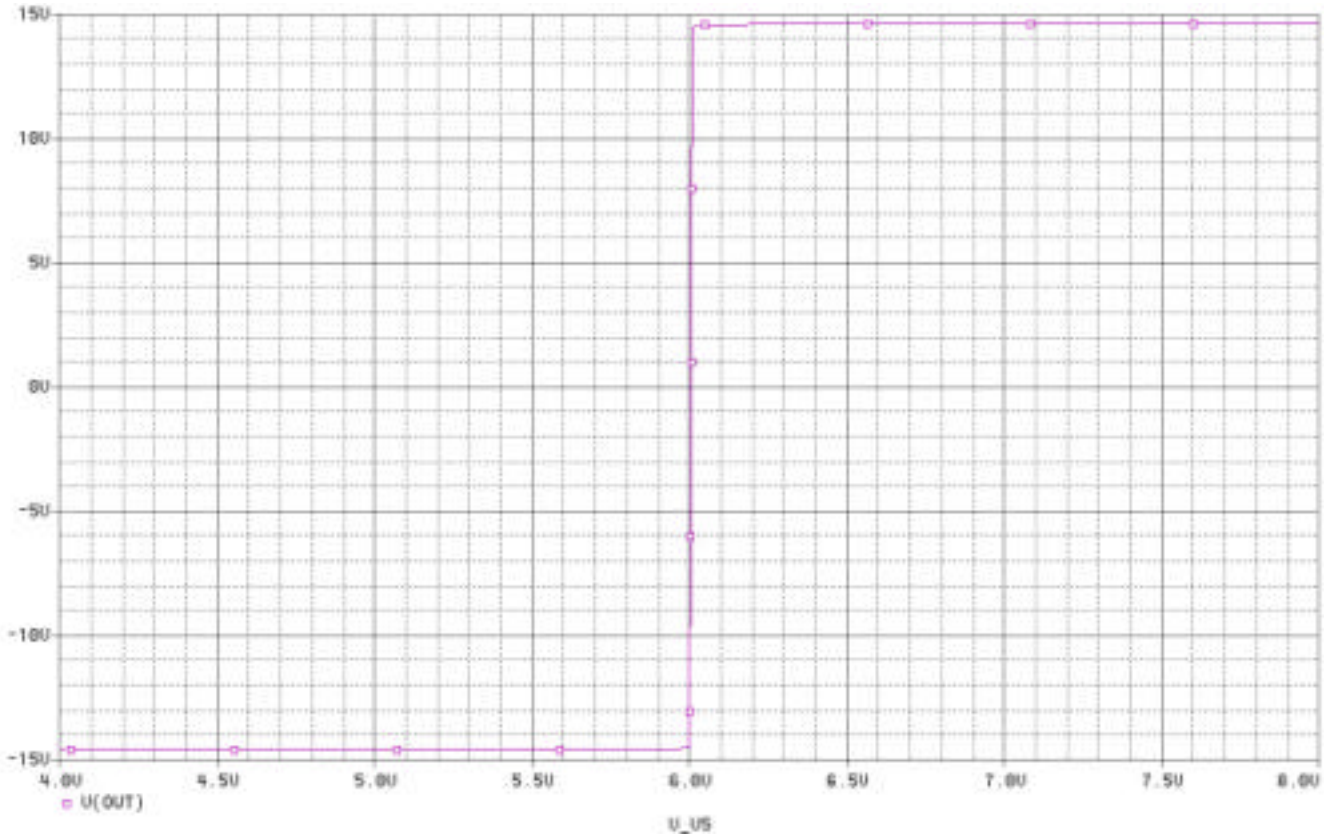


(b) Using SPICE the following plot is obtained:

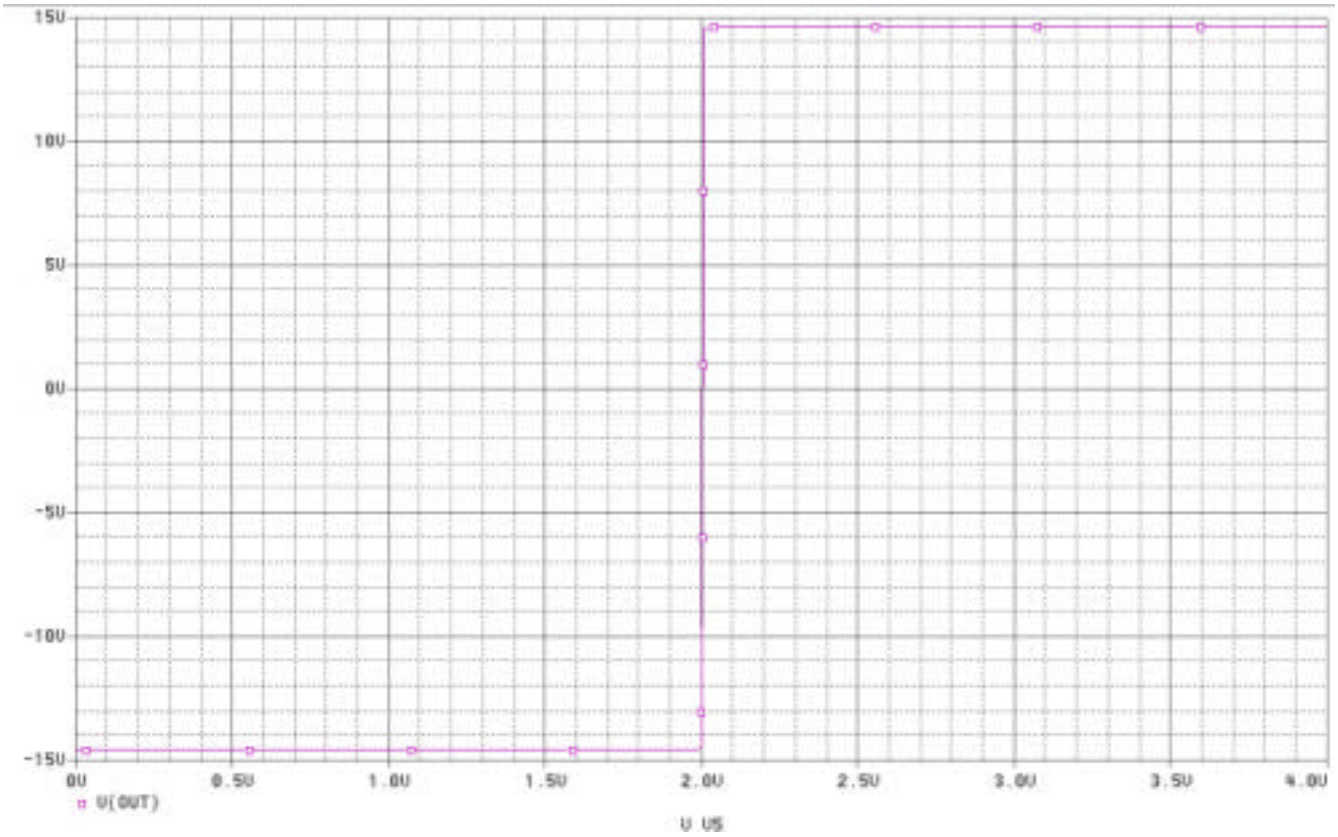


SOLUTION 4.21. The first stage is in a summing configuration, thus its output is, assuming it's in the active region of operation, -15 V which means it is just about to saturate. The second stage is in the inverting configuration with a gain of -1.5, which means that the overall output will be saturated at 15V.

SOLUTION 4.22. When $v_{in} - 80k\left(\frac{v_{in}+1.5}{100k}\right) > 0$, or $v_{in} > 6$ the output of the comparator saturates at –15 V, when it is $v_{in} < 6$, it will saturate at 15 V. The following plot is obtained from SPICE.



SOLUTION 4.23. When $v_{in} - 10k\left(\frac{v_{in}+20}{110k}\right) > 0$, or $v_{in} > 2$ the output of the comparator will be saturated at -15V. Otherwise when it is < 2V the output saturates at 15V. In SPICE:

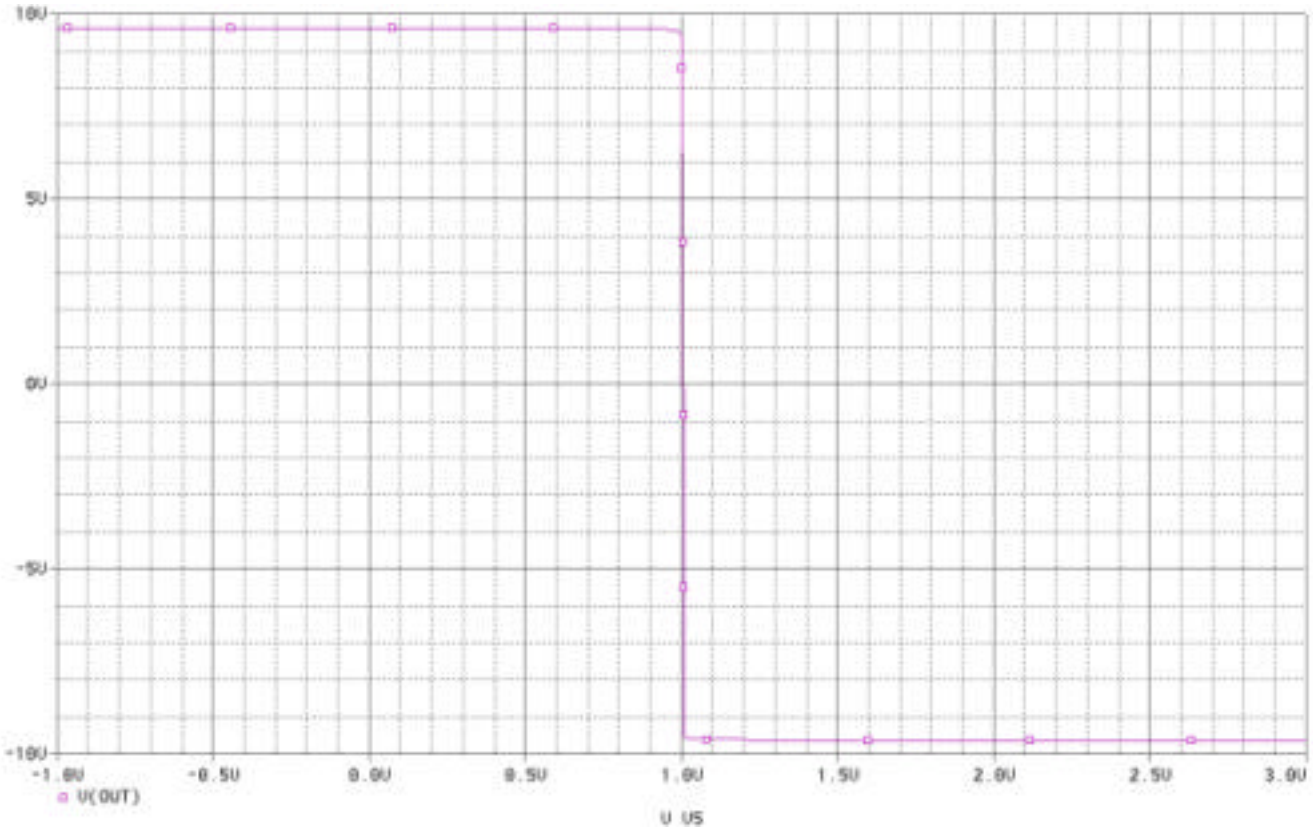


SOLUTION 4.24. Based on the same reasoning as the previous questions,

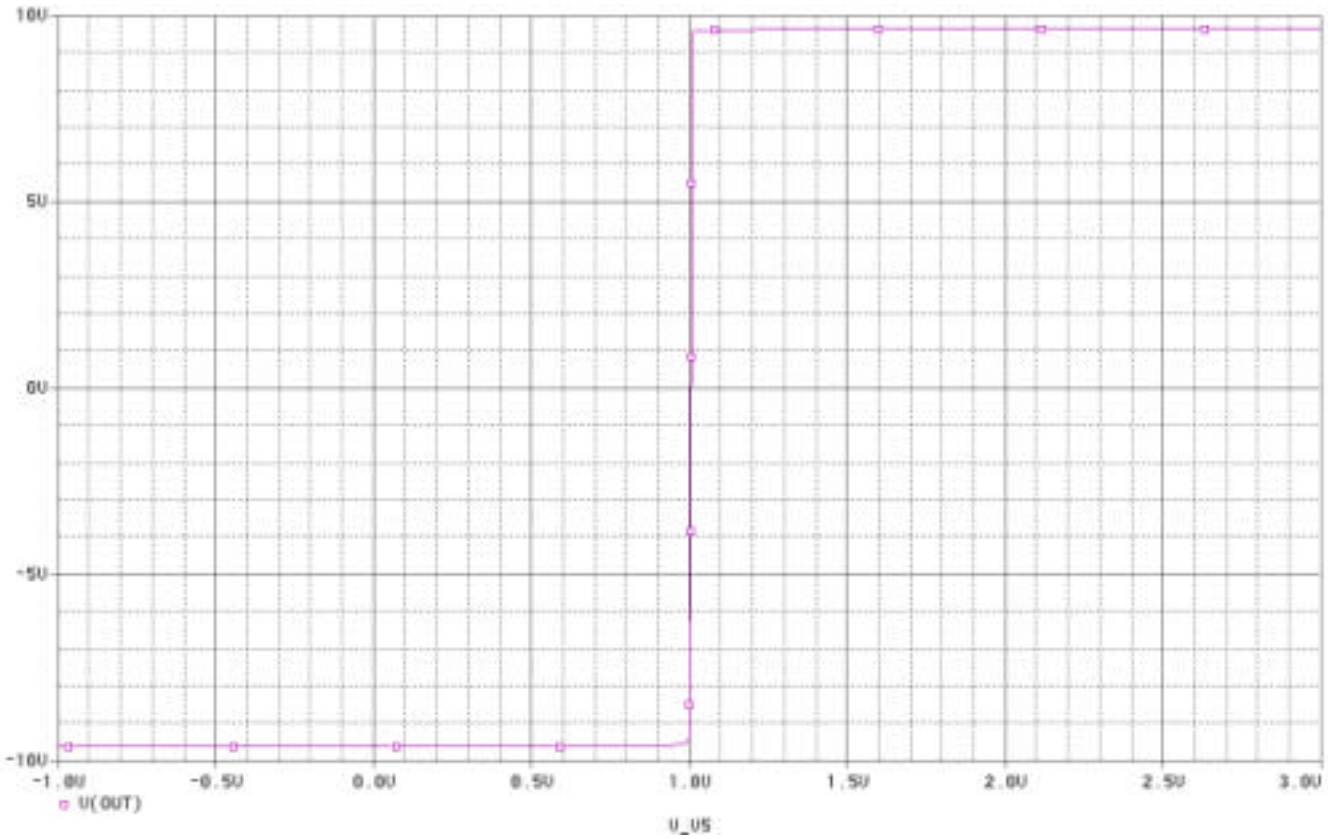
The output will be $+V_{sat}$, when $v_{in} < v_{ref}\left(1-\frac{R_1+R_2}{R_2}\right) = -\frac{R_1}{R_2}v_{ref}$, and $-V_{sat}$ for

$v_{in} > v_{ref}\left(1-\frac{R_1+R_2}{R_2}\right) = -\frac{R_1}{R_2}v_{ref}$.

SOLUTION 4.25. Using the previously derived relationship, and the topology of figure P4.24, set $v_{ref} = -1.5V$, and $R_1 = 2k\Omega$ and $R_2 = 3k\Omega$. Set the power supplies to the Op-amp to +/– 10V to satisfy the V_{sat} requirement. Also the input to the inverting and non-inverting terminal are reversed for fig. P4.24. Verifying in SPICE we obtain the following,

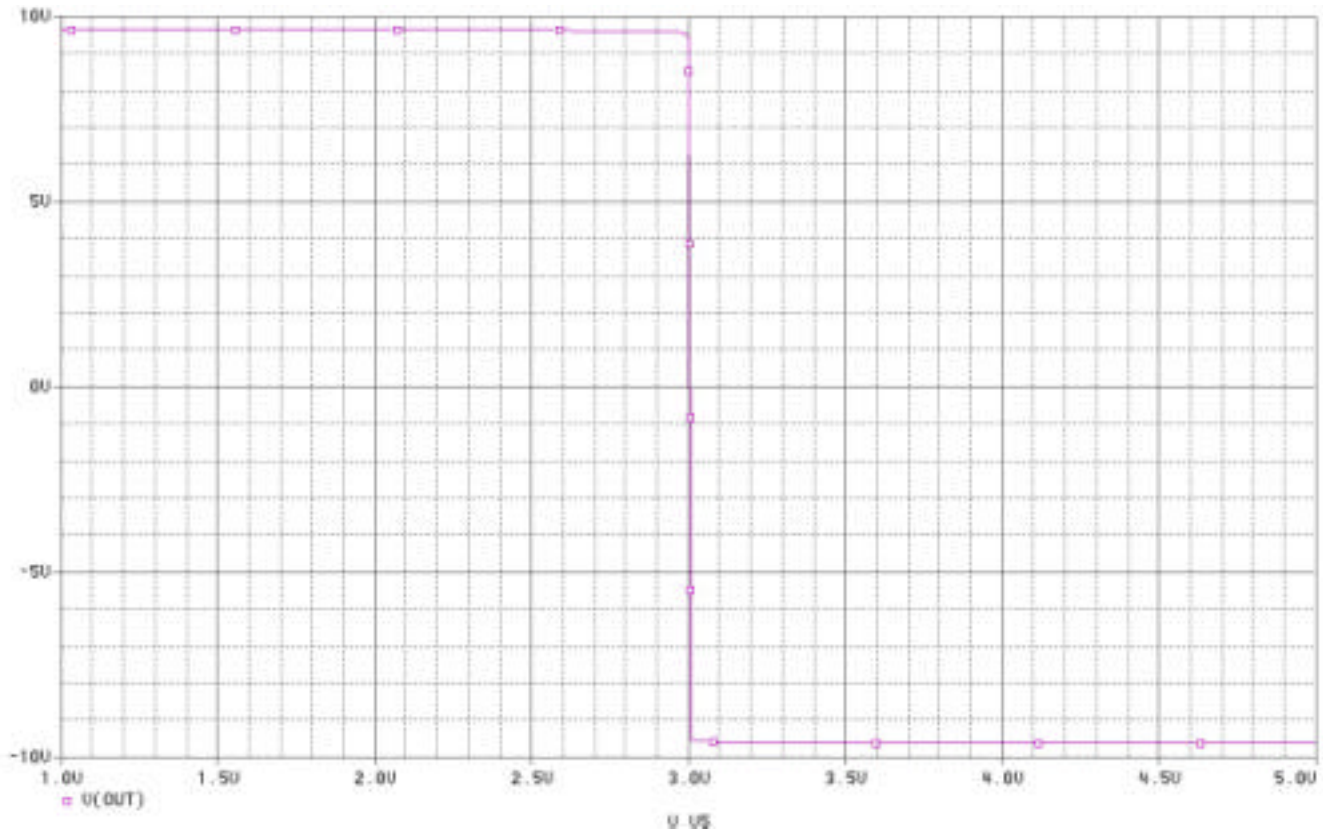


SOLUTION 4.26. The design that fulfills the requirement is the same as for P4.25, with the input to the op amp reversed. The following is obtained from SPICE,



SOLUTION 4.27. First, for the comparator to give +Vsat for the lower voltages, the inputs to the op amp in the topology of P4.24 must be interchanged. Then the components are chosen to satisfy the following relationship, $v_{switch} = v_{ref}\left(1 - \frac{R_1 + R_2}{R_2}\right) = -\frac{R_1}{R_2} v_{ref}$. Choose $v_{ref} = -1.5V$, and R_1 = 2k and R_2 = 1k.

Verifying in SPICE,



SOLUTION 4.28. Write KCL at the inverting terminal, noting that the no current flows into it: $(V_- - v_{in})/\ R = (v_{out} - V_-)/\ R$. Use the following relationship $v_{out} = A(V_+ - V_-) = -AV_-$. Solving using the previous two equations yields $v_{out}\ /\ v_{in} = -\dfrac{A}{A+2}$.

SOLUTION 4.29. (a) By inspection the voltage gain for the ideal case is –1. When A=1000, the gain becomes –0.998, thus 0.2%.

(b) Repeating the method of P4.28, and setting $v_{out}\ /\ v_{in} = -\dfrac{AR_f}{R_f + R_1 + AR_1}$ to –1 and solving for

$R_f = 10.417k\Omega$.

(c) Solving the previous equation when the gain is –1, $R_f\ /\ R_1 = (A+1)/\ (A-1)$.

SOLUTION 4.30. (a)The first part was obtained in P4.29. Rearranging the equation yields

$$v_{out}\ /\ v_{in} = -\frac{R_f}{R_1}\left[\frac{1}{1+\left(1+R_f\ /\ R_1\right)/\ A}\right].$$

(b) The error is caused by $(1+R_f/R_1)/A$ in the denominator, and may be defined, in percent, as $100-\left[\frac{1}{1+\left(1+R_f/R_1\right)/A}\right]100$. Thus for the conditions listed in the problem, it will always be less than 2.05%. With A = 10000 it will be less than 0.21%.

SOLUTION 4.31. (a) Substituting the non-ideal model, and writing KCL at the inverting terminal, $(V_- - v_{in})/R_1 + V_-/R_{in} = (v_{out}-V_-)/R_f$ is obtained. Now observe the following dependencies, $i_{out} = v_{out}/R_L$, and $v_{out} = -AV_- - (i_{out}+(v_{out}-V_-)/R_f)R_{out}$. Using these three equations, substitute the second into the third and then solve for v_{out}/v_{in} using the last two. This yields

$$V_- = v_{out} + v_{in}\frac{R_f}{R_1}1/\left(\frac{R_f}{R_1}+\frac{R_f}{R_{in}}+1\right) = v_{out}\left(\frac{-1-\frac{R_{out}}{R_L}-\frac{R_{out}}{R_f}}{A-\frac{R_{out}}{R_f}}\right)$$

and

$$v_{out}/v_{in} = -\frac{R_f}{R_1}\left(\frac{1}{1+\left(\frac{1+\frac{R_{out}}{R_f}+\frac{R_{out}}{R_L}}{A-\frac{R_{out}}{R_f}}\right)\left(1+\frac{R_f}{R_1}+\frac{R_f}{R_{in}}\right)}\right)$$

A gain of –9.988

(b) For an ideal op-amp the gain is $-R_f/R_1$=-10.

(c) The error is about 0.1175%.

SOLUTION 4.32. The gain is –9.883, and the error 1.16%

SOLUTION 4.33. This derivation was performed in P4.31.

SOLUTION 4.34. Assume that the sliding contact is at the bottom of R_p. Then, writing KCL at the inverting terminal yields $v_{in} / R_o = (v_{out} - v_{in}) / R_p$. This implies $v_{out} / v_{in} = 1 + R_p / R_o$. When the slider is at the top, it is evident that $v_{out} = v_{in}$. Therefore $1 \le v_{out} / v_{in} \le 1 + \frac{R_p}{R_o}$.

SOLUTION 4.35. Writing KCL at inverting input, and making use of voltage division, $-v_{in} / R_1 = \left[\beta v_{out} / R_f\right]$ where β is the fraction of v_{out} that appears across R_f. Hence, $\frac{v_{out}}{v_{in}} = -\frac{R_f}{\beta R_1}$.

When the slider is at the top $\beta = 1$ and $\frac{v_{out}}{v_{in}} = -\frac{R_f}{R_1}$. When the slider is at the bottom, the fraction of vout appearing across R_f is $\beta = \frac{R_f // R_0}{R_f // R_0 + R_p} = \frac{R_f R_0}{R_f + R_0} \times \frac{1}{\frac{R_f R_0}{R_f + R_0} + R_p} = \frac{R_f R_0}{R_f R_0 + R_p (R_f + R_0)}$. Hence

$\frac{1}{\beta} = \frac{R_f R_0 + R_p (R_f + R_0)}{R_f R_0} = 1 + \frac{R_p}{R_0} + \frac{R_p}{R_f}$. It follows that $\frac{v_{out}}{v_{in}} = -\frac{R_f}{\beta R_1} = -\frac{R_f}{R_1}\left(1 + \frac{R_p}{R_0} + \frac{R_p}{R_f}\right)$.

Therefore the range of achievable voltage gain is

$$-\frac{R_f}{R_1} \ge \frac{v_{out}}{v_{in}} \ge -\frac{R_f}{R_1}\left(1 + \frac{R_p}{R_0} + \frac{R_p}{R_f}\right)$$

SOLUTION 4.36. Using the basic non-inverting configuration of figure 4.10 characterized by $v_{out} / v_{in} = \left(1 + \frac{R_f}{R_1}\right)$, i.e., $\mu = \left(1 + \frac{R_f}{R_1}\right)$.

SOLUTION 4.37. At first glance, one might use two inverting configurations, figure 4.5, in cascade. However, such would not have infinite input resistance. To circumvent this problem we add a buffer amplifier as per figure 4.7 at the front end of a cascade of two inverting configurations. The resulting overall gain is $\mu = \left(\frac{R_{f1}}{R_{11}}\right)\left(\frac{R_{f2}}{R_{12}}\right)$. Indeed, such a configuration can achieve theoretically any gain greater than zero.

SOLUTION 4.38. Using a single inverting amplifier configuration, figure 4.5, preceded by a buffer stage of figure 4.7. The gain is $\mu = -\frac{R_f}{R_1}$.

SOLUTION 4.39. By KVL for figure P4.39a, $V_o = -i_1 R_f$. Thus to achieve $V_o = -i_1 r_m$ in figure P4.39b, we set $R_f = r_m$.

SOLUTION 4.40. Writing KCL at the inverting node of the ideal op amp yields $I_L = V_i / R_a$, which is indeed independent of the load resistor which has no effect on the load current.

SOLUTION 4.41. The current through the LED is $I_L = 10\left(\frac{R_1}{10k}\right) / 3.8k$, so for (a) it is 1.32mA and for (b) 2.11mA.

SOLUTION 4.42. Applying KCL at the inverting terminal, $I_L = v_{in} / R_1$. Again, ideally, R_L does not affect I_L.

SOLUTION 4.43. (a) Defining a temporary voltage V_o at the output of the op-amp, we can write KCL at the inverting and non-inverting terminal:

$$(V_- - 2)/ 1k = (V_o - V_-) / 2k$$
$$V_- /100 + (V_- - V_o) / 200 = I_{out}$$

Substituting the first equation into the second and simplifying causes V_o to drop out and $I_{out} = 20mA$. (b) The answer remains the same as the value of the load resistance was not used for finding the load current.

SOLUTION 4.44. Using the same approach as for the previous question, but with resistor labels instead, the following equations are obtained from KCL:

$$V_- = \frac{R_2 V_s + R_1 V_o}{R_2 + R_1}$$

$$I_{out} = V_-\left(\frac{R_2 + R_1}{R_1 R_2}\right) - \frac{V_o}{R_2}$$

Substituting the first into the second yields $I_{out} = V_s / R_1$.

SOLUTION 4.45. (a) $V_s = 5$ V, (b) $I_{out} = 10mA$ sets $R_1 = V_s / I_{out} = 500\,\Omega$. (c) From KVL and Ohm's law, $I_s = (V_s + R_L I_{out}) / \alpha R_1$. We require $I_s < 0.5$ mA. This means that in the worst case, $R_L = 500\ \Omega$,

$$\frac{(V_s + R_L I_{out})}{0.5 \times 10^{-3} R_1} = \frac{5 + 500 \times 0.01}{0.25} = 40 < \alpha .$$

(d) From KVL and Ohm's,

$$V_o = -R_L I_{out} - (I_{out} + (R_L I_{out})/\ R_1) R_2 \geq -20\ \text{V}$$

Hence

$$R_2 \leq \frac{20 - R_L I_{out}}{(I_{out} + (R_L I_{out}) / R_1)} = \frac{20 - 5}{0.01 + 5/\ 500} = 750$$

Hence one design is to pick $R_2 = 750\,\Omega$ and $\alpha = 40$ which implies $\alpha R_2 = 30$ kΩ.

SOLUTION 4.46. The exact same design as P4.45 can be used with the isolation buffer of figure 4.7 placed at the input of it in order to provide the infinite input resistance needed by P4.46b.

SOLUTION 4.47. The general expression for this summing circuit is

$$V_{out} = -\frac{R_f}{R_o} V_o - \frac{R_f}{R_1} V_1 - \frac{R_f}{R_2} V_2 - \frac{R_f}{R_3} .$$

(a) Using the expression above $|V_{out}| = |-1 - 0 - 0 - 8|\ E = 9E$.

(b) $|V_{out}| = |-0 - 2 - 4 - 0|\ E = 6E$.

(c) It has to be a linear combination of 8, 4, 2, 1, thus [1 1 0 1] would yield 13E.

(d) With the same approach, [0 1 1 1].

SOLUTION 4.48. For this implementation we add an extra R-2R branch along with an extra summing input to the op amp. From the theory developed in Example 4.9 the total resistance seen by the source is 2R. For the total power supplied by the source to be less than 0.02 W, we require $R \geq \frac{E^2}{2(0.02)} = 2.5$ kΩ.

SOLUTION 4.49. The same steps as in the previous questions are repeated. Because the resistance seen by the source is unchanged no matter how many branches are added to the R-2R network,

$$R \geq \frac{E^2}{2(0.01)} = 5\ \text{k}\Omega.$$

SOLUTION 4.50. (a) If the input is $3v_{\max}/8$, then the first comparator will give $-V_{sat}$, keeping S_2 down. The next comparator will output $+V_{sat}$, causing S_1 to go up. After subtraction, the input to the last comparator is $v_{\max}/8$ yielding $+V_{sat}$ at its output since its input is slightly above the reference input level. Thus the logic output values are [0 1 1].

(b) Putting in $6v_{\max}/8$, will cause $+V_{sat}$ and S_2 to go up. The input to the second comparator will be $2v_{\max}/8$, which will cause $+V_{sat}$ and S_1 to go up. The input to the last comparator will be 0, thus it will output $-V_{sat}$. The corresponding logic output is [1 1 0].

SOLUTION 4.51. Simply add a subtractor and switch to the last comparator, followed by an additional comparator. The reference level to the new (additional) comparator will be $v_{\max}/16$, and its output will be the new least significant bit.

SOLUTION 4.52. (a) Writing the node equation for figure P4.52c,

$$\frac{V_{out}}{R_L'} + \frac{(V_{out} - V_1)}{10k} = \frac{A(0 - V_1) - V_{out}}{R_{out}}$$

which implies that

$$V_{out}/V_1 = \frac{\left(\frac{1}{10k} - \frac{A}{R_{out}}\right)}{\left(\frac{1}{R_L'} + \frac{1}{10k} + \frac{1}{R_{out}}\right)}$$

For figure P4.52a, the corresponding node equation is

$$\frac{V_{out}}{R_L} = \frac{A(0 - V_{in}) - V_{out}}{R_{out}}$$

which leads to

$$V_{out} / V_{in} = \frac{\left(-\frac{A}{R_{out}}\right)}{\left(\frac{1}{R_L} + \frac{1}{R_{out}}\right)}$$

Note that $\frac{1}{R_L} = \frac{1}{R_L^1} + \frac{1}{10k}$, which when substituted into the later equation make both of them approximately the same since the 1/10k term in the numerator of V_{out} / V_1 has a negligible contribution.

(b) Writing the node equation for figure P4.52d, yields

$$\frac{V_{out}}{R_L'} + \frac{(V_{out} - V_2)}{10k} = \frac{A(0 - V_1) - V_{out}}{R_{out}}$$

Hence

$$V_1 = V_2\left(\frac{100 || R_{in}}{(100 || R_{in}) + 10k}\right) \approx \frac{V_2}{101}$$

Solving produces $V_{out} / V_2 = \frac{\left(\frac{1}{10k} - \frac{A}{101R_{out}}\right)}{\left(\frac{1}{R_L^1} + \frac{1}{10k} + \frac{1}{R_{out}}\right)}$. Note that as in (a) the 1/10k term in the numerator is negligible; after eliminating this negligible term, one sees that $\frac{V_{out}}{V_2}$ is 101 time smaller than $\frac{V_{out}}{V_{in}}$.

SOLUTION 4.53. (a) Using the equation just derived, after substituting in the values, the gain is –980.392

(b) From the previous equation, $V_{out} / V_1 = -980.382$; write KCL at the non-inverting terminal to obtain, $\frac{V_{in} - V_1}{10k} = \frac{V_1}{R_{in}} + \frac{V_1 - V_{out}}{10k}$; substitute $V_{out} = -980.382V_1$; solve for V_1 / V_{in}, and then multiply both gains to obtain $(V_{out} / V_1)(V_1 / V_{in}) = V_{out} / V_{in} = -0.9979$.

(c) They only differ by about 0.01%, thus they are very similar.

SOLUTION 4.54. Writing out the transfer equation, $V_{out} = \frac{R_2}{R_1} V_{s2} - \frac{R_2}{R_1} V_{s1}$, thus $R_2 / R_1 = 4$. Using $R_2 = 100k\Omega$, $R_1 = 25k\Omega$. As expected SPICE shows to noticeable difference in outputs when the source resistances are varied.

SOLUTION 4.55. Due to the ideal nature of the op-amp, the voltage $V_{R_b} = V_{s2} - V_{s1}$. By KVL

$$V_2 = V_{s2} + R_a(V_{s2} - V_{s1})/\ R_b$$
$$V_1 = V_{s1} - R_a(V_{s2} - V_{s1})\ /\ R_b$$

Next, $V_1 - V_2 = (V_{s1} - V_{s2})(1 + 2R_a\ /\ R_b)$.

SOLUTION 4.56. (a) Noticing that the final stage is a summing op-amp in which $V_{out} = \frac{R_2}{R_1} V_1 - \frac{R_2}{R_1} V_2$.

From the previous question, $V_{out} = \frac{R_2}{R_1}(V_1 - V_2) = \frac{R_2}{R_1}(1 + 2R_a\ /\ R_b)(V_{s1} - V_{s2})$. Thus

$\alpha = \frac{R_2}{R_1}(1 + 2R_a\ /\ R_b)$. The gain α can be varied by adjusting the single resistance R_b.

(b) Picking the set of values below will satisfy the requirement:

$$R_2 = 100\text{k}\Omega,\ \ R_1 = 100\text{k}\Omega,\ \ R_a = 20\text{k}\Omega,\ \ R_b = 10\text{k}\Omega.$$

(c) Doing the SPICE simulation using the parameters from (b) yield 5 V at the output for $V_{s1} - V_{s2} = 2 - 1$ V. Setting R_b arbitrarily to 20 kΩ, the output now becomes 3 V, which agrees with the relationships developed earlier.