# EE 2209
# Electronics-II
# Field Effect Transistor

**Dr. Mostafa Zaman Chowdhury**

# EE 2209 Electronics-I
# Credit: 4, Contact Hours: 4 Hrs/Week

- **Syllabus**
  - ***Transistor circuit analyses:*** **Different transistor equivalent circuits, r-parameters and h-parameters; Analysis at low, medium and high frequencies; Transistor amplifier circuits and their cascading; analysis of RC coupled transistor amplifier circuits at LF, MF, and HF ranges, effect of input output impedances; Darlington pair; Emitter follower.**
  - ***Feedback Amplifiers:*** **Basic concept, Amplifiers: voltage and current, negative feedback amplifiers, effect of negative feedback upon output and input resistances, different types of feedback amplifiers; stability.**
  - ***FET:*** **Introduction, Construction and characteristics, transfer characteristics, MOSFET: depletion type and enhancement type, biasing, FET amplifier, VVR, CMOS, VMOS, FET small signal model and analysis.**
  - ***Power Amplifiers*****: Untuned Class A, AB and B amplifiers, tuned class B and C amplifiers, neutralization, push-pull Class B and C amplifiers and their design, transistor amplifier with complimentary symmetry, Tuned potential amplifiers: single, double and Cascaded.**
  - ***P-AMP*****: Different types of operational amplifiers and their applications in: Differentiator, integrator and comparator circuits. Analog computer and its application in differential equation solution, active filter.**

# FETs vs. BJTs

## Similarities:

- **Amplifiers**
- **Switching devices**
- **Impedance matching circuits**

## Few Differences:

- **FETs are voltage controlled devices. BJTs are current controlled devices.**
- **FETs have a higher input impedance. BJTs have higher gains.**
- **FETs are less sensitive to temperature variations and are more easily integrated on ICs.**
- **FETs are generally more static sensitive than BJTs.**

# FET Types

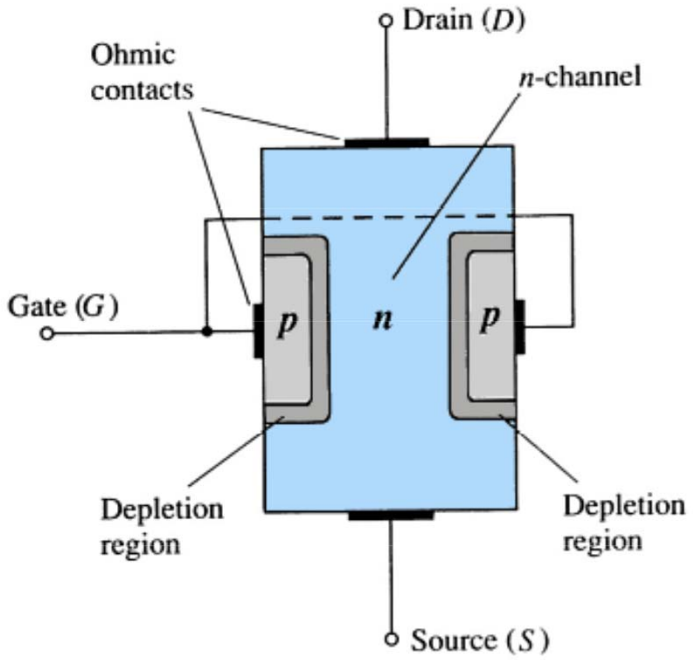
- **JFET:** **Junction FET**
- **MOSFET:** **Metal–Oxide–Semiconductor FET**
  - **D-MOSFET:** **Depletion MOSFET**
  - **E-MOSFET:** **Enhancement MOSFET**

# JFET Construction

**There are two types of JFETs**

- ***n*-channel**
- ***p*-channel**

**The n-channel is more widely used.**




**There are three terminals:**

- **Drain (D) and Source (S) are connected to the *n*-channel**
- **Gate (G) is connected to the *p*-type material**

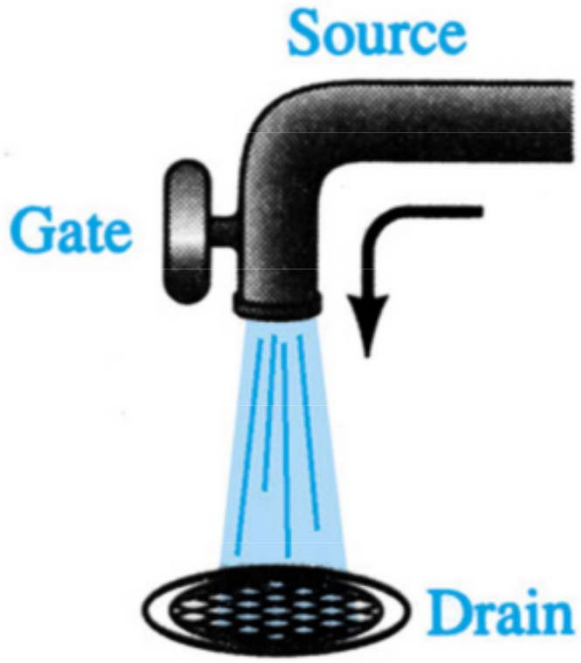
# JFET Operation: The Basic Idea

JFET operation can be compared to a water spigot.

**The source** of water pressure is the accumulation of electrons at the negative pole of the drain-source voltage.

The drain of water is the electron deficiency (or holes) at the positive pole of the applied voltage.

**The control** of flow of water is the gate voltage that controls the width of the n-channel and, therefore, the flow of charges from source to drain.



# JFET Operating Characteristics

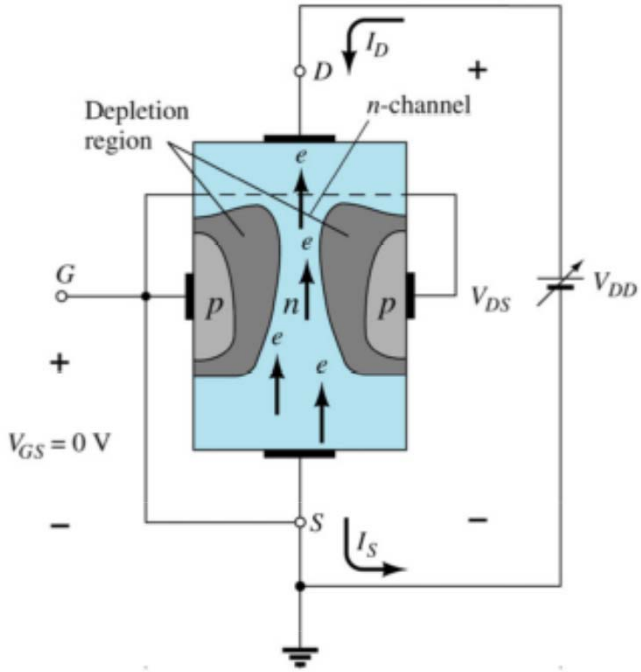
**There are three basic operating conditions for a JFET:**

- **$V_{GS} = 0$, $V_{DS}$ increasing to some positive value**
- **$V_{GS} < 0$, $V_{DS}$ at some positive value**
- **Voltage-controlled resistor**

# JFET Operating Characteristics: $V_{GS} = 0$ V

**Three things happen when $V_{GS} = 0$ and $V_{DS}$ is increased from 0 to a more positive voltage**

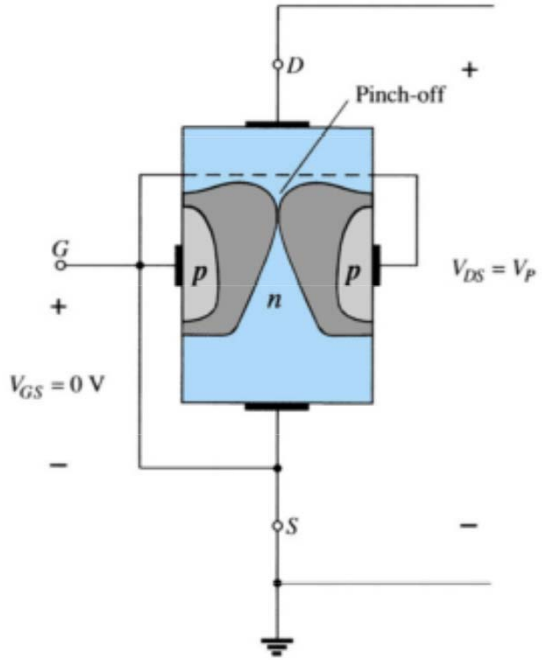
- **The depletion region between p-gate and n-channel increases as electrons from n-channel combine with holes from p-gate.**
- **Increasing the depletion region, decreases the size of the n-channel which increases the resistance of the n-channel.**
- **Even though the n-channel resistance is increasing, the current ($I_D$) from source to drain through the n-channel is increasing. This is because $V_{DS}$ is increasing.**



# JFET Operating Characteristics: Pinch Off

**If $V_{GS}$ = 0 and $V_{DS}$ is further increased to a more positive voltage, then the depletion zone gets so large that it pinches off the n-channel.**

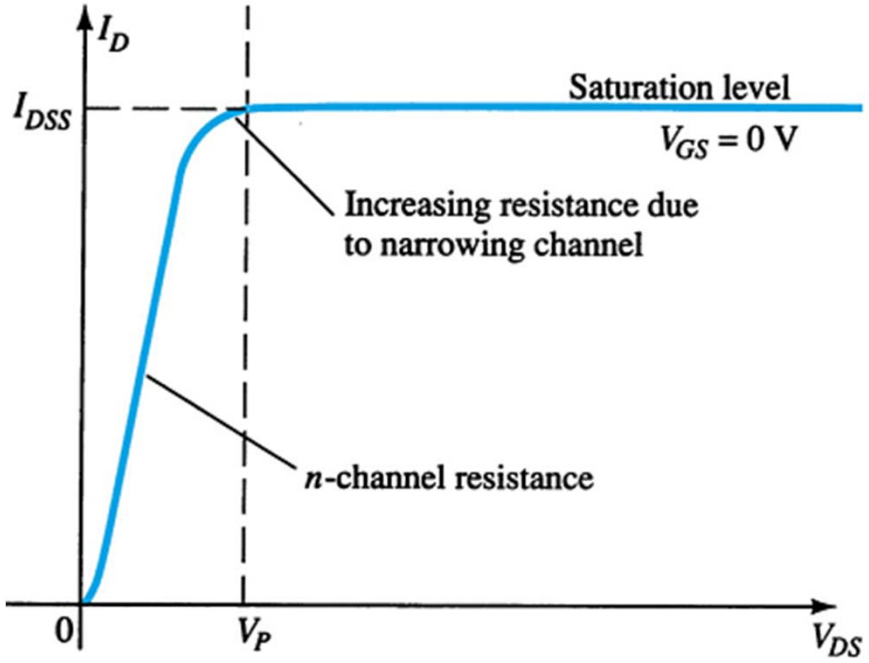
**This suggests that the current in the n-channel ($I_D$) would drop to 0A, but it does just the opposite–as $V_{DS}$ increases, so does $I_D$.**



# JFET Operating Characteristics: Saturation

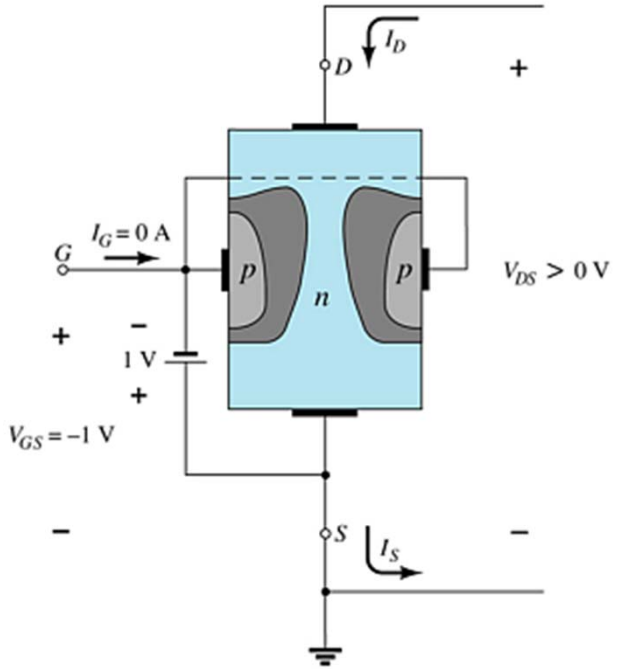
**At the pinch-off point:**

- **Any further increase in $V_{GS}$ does not produce any increase in $I_D$. $V_{GS}$ at pinch-off is denoted as $V_p$.**
- **$I_D$ is at saturation or maximum. It is referred to as $I_{DSS}$.**
- **The ohmic value of the channel is maximum.**



# JFET Operating Characteristics

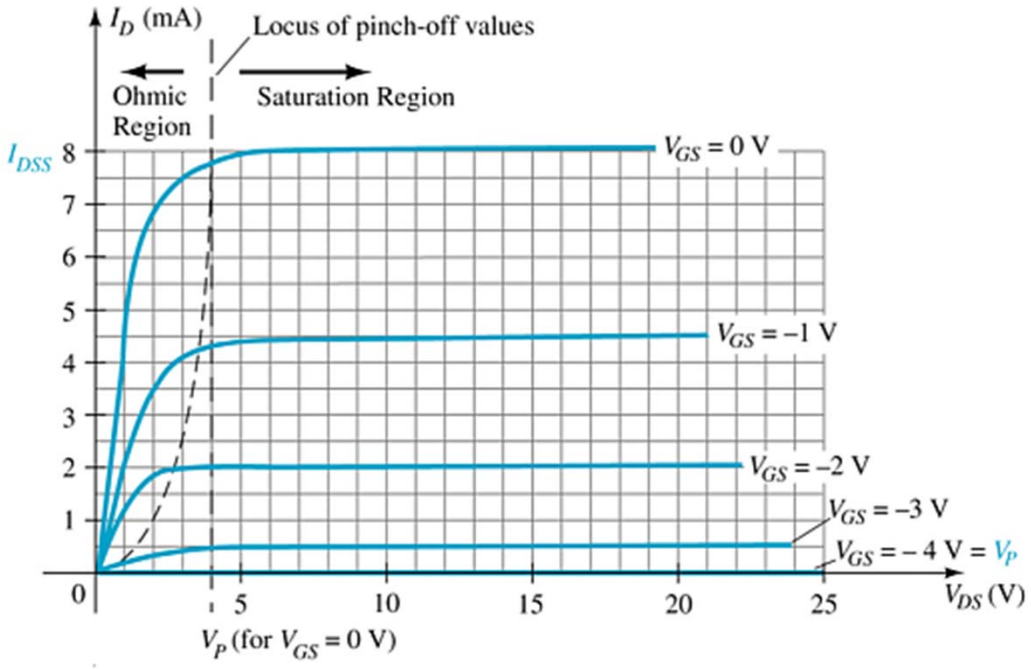
**As $V_{GS}$ becomes more negative, the depletion region increases.**



# JFET Operating Characteristics

**As $V_{GS}$ becomes more negative:**

- **The JFET experiences pinch-off at a lower voltage ($V_P$).**
- **$I_D$ decreases ($I_D < I_{DSS}$) even though $V_{DS}$ is increased.**
- **Eventually $I_D$ reaches 0 A. $V_{GS}$ at this point is called $V_p$ or $V_{GS(off)}$..**



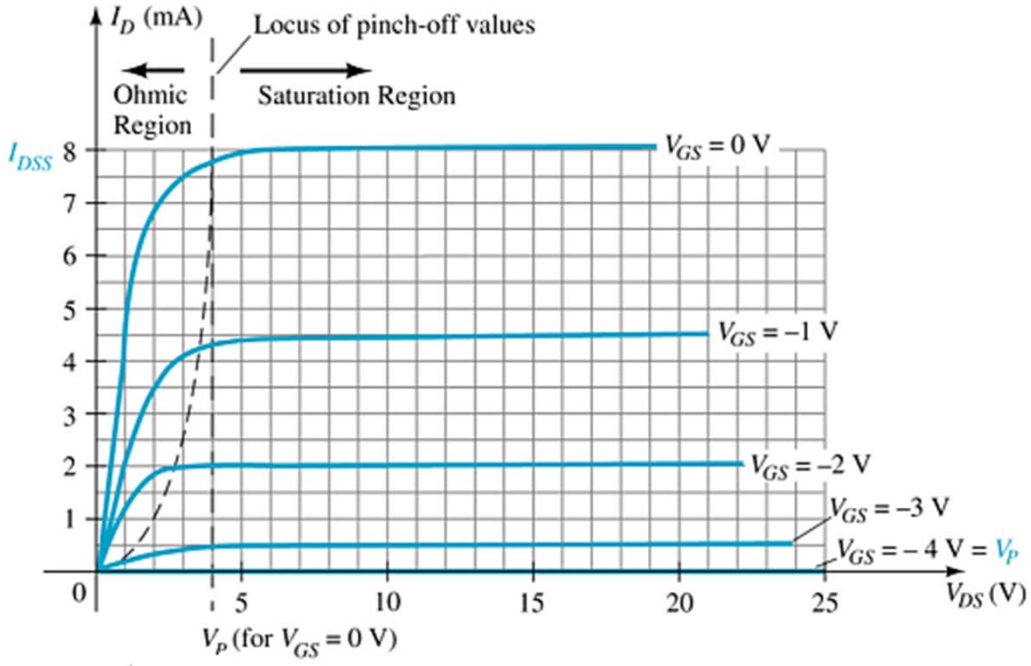

**Also note that at high levels of $V_{DS}$ the JFET reaches a breakdown situation. $I_D$ increases uncontrollably if $V_{DS} > V_{DSmax}$.**

# JFET Operating Characteristics: Voltage-Controlled Resistor

**The region to the left of the pinch-off point is called the ohmic region.**

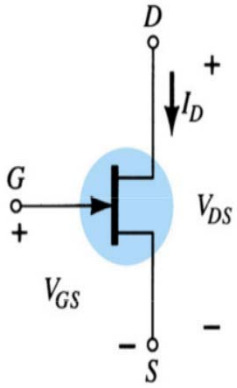
**The JFET can be used as a variable resistor, where $V_{GS}$ controls the drain-source resistance ($r_d$). As $V_{GS}$ becomes more negative, the resistance ($r_d$) increases.**

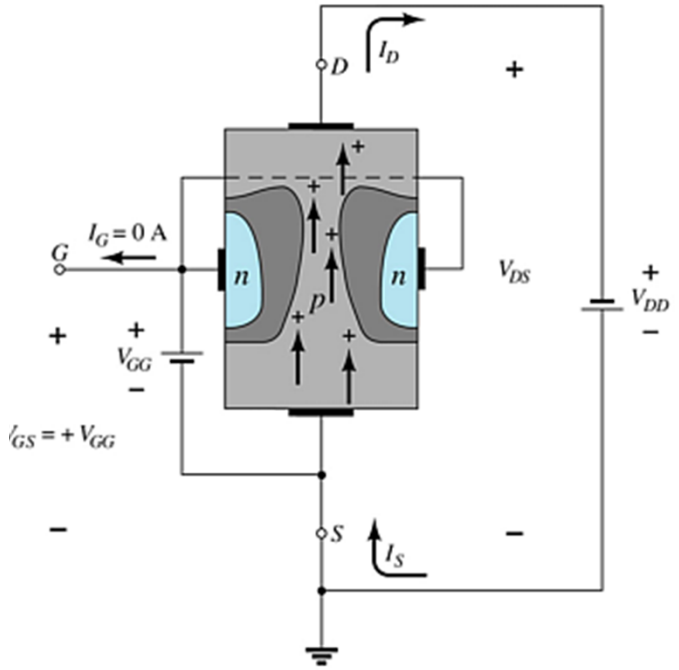
$$r_d = \frac{r_o}{\left(1 - \frac{V_{GS}}{V_P}\right)^2}$$



# p-Channel JFETS

**The *p*-channel JFET behaves the same as the *n*-channel JFET, except the voltage polarities and current directions are reversed.**

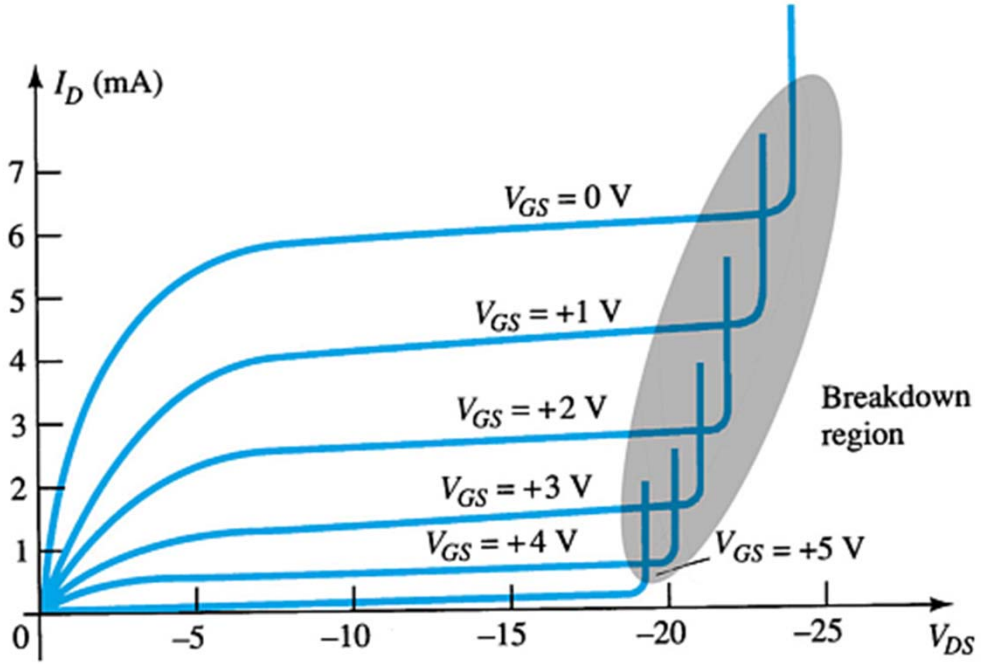


# p-Channel JFET Characteristics

**As $V_{GS}$ increases more positively**

- **The depletion zone increases**
- **$I_D$ decreases ($I_D < I_{DSS}$)**
- **Eventually $I_D = 0$ A**




**Also note that at high levels of $V_{DS}$ the JFET reaches a breakdown situation: $I_D$ increases uncontrollably if $V_{DS} > V_{DSmax}$.**

# JFET Transfer Characteristics

**The transfer characteristic of input-to-output is not as straightforward in a JFET as it is in a BJT.**

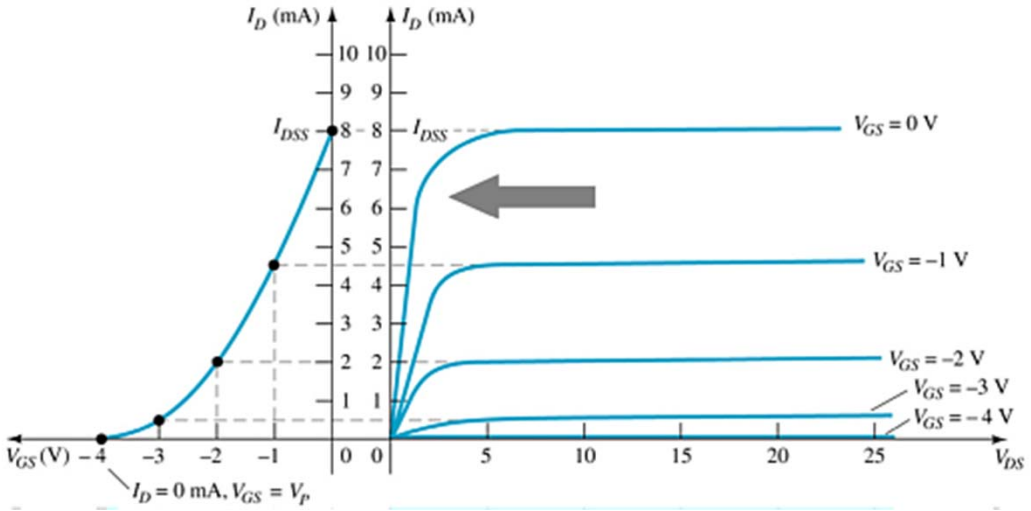
**In a BJT, $\beta$ indicates the relationship between $I_B$ (input) and $I_C$ (output).**

**In a JFET, the relationship of $V_{GS}$ (input) and $I_D$ (output) is a little more complicated:**

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$$

# JFET Transfer Curve

**This graph shows the value of $I_D$ for a given value of $V_{GS}$.**



# Plotting the JFET Transfer Curve

**Using $I_{DSS}$ and Vp ($V_{GS(off)}$) values found in a specification sheet, the transfer curve can be plotted according to these three steps:**

**Step 1**

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

**Solving for $V_{GS}$ = 0V** $\quad I_D = I_{DSS}$

**Step 2**

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

**Solving for $V_{GS} = V_p$ ($V_{GS(off)}$)** $\quad I_D = 0A$

**Step 3**

**Solving for $V_{GS}$ = 0V to $V_p$** $\quad I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

# MOSFETs

**MOSFETs have characteristics similar to JFETs and additional characteristics that make then very useful.**

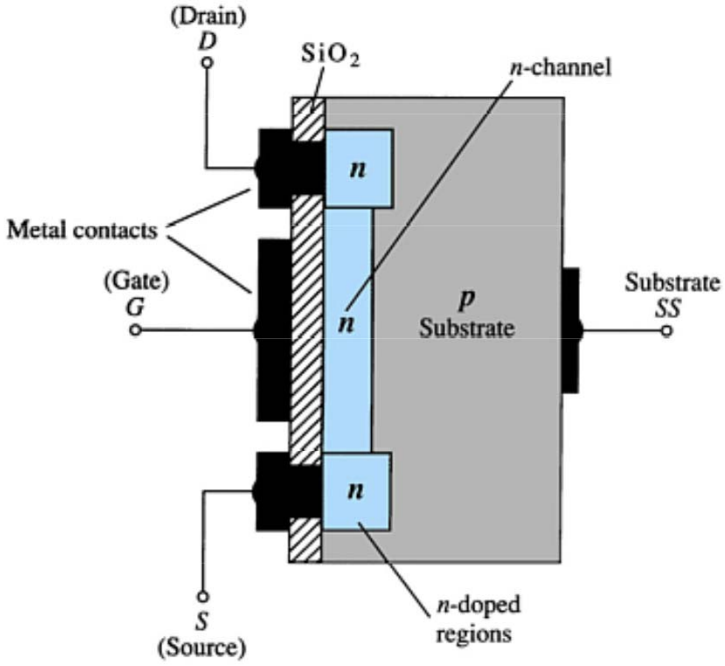
**There are two types of MOSFETs:**

- **Depletion-Type**
- **Enhancement-Type**

# Depletion-Type MOSFET Construction

**The Drain (D) and Source (S) connect to the to *n*-doped regions. These *n*-doped regions are connected via an *n*-channel. This *n*-channel is connected to the Gate (G) via a thin insulating layer of $SiO_2$.**

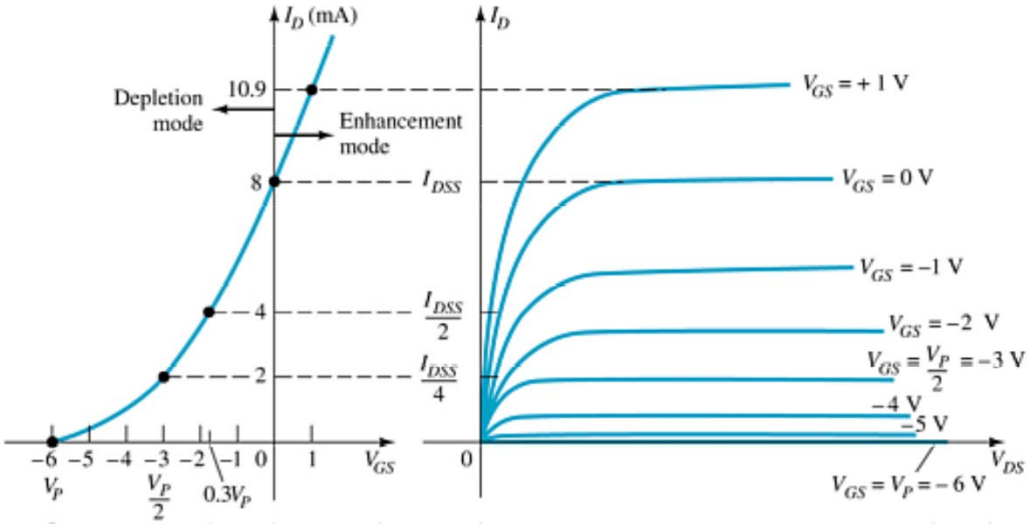
**The *n*-doped material lies on a *p*-doped substrate that may have an additional terminal connection called Substrate (SS).**



# Basic MOSFET Operation

**A depletion-type MOSFET can operate in two modes:**

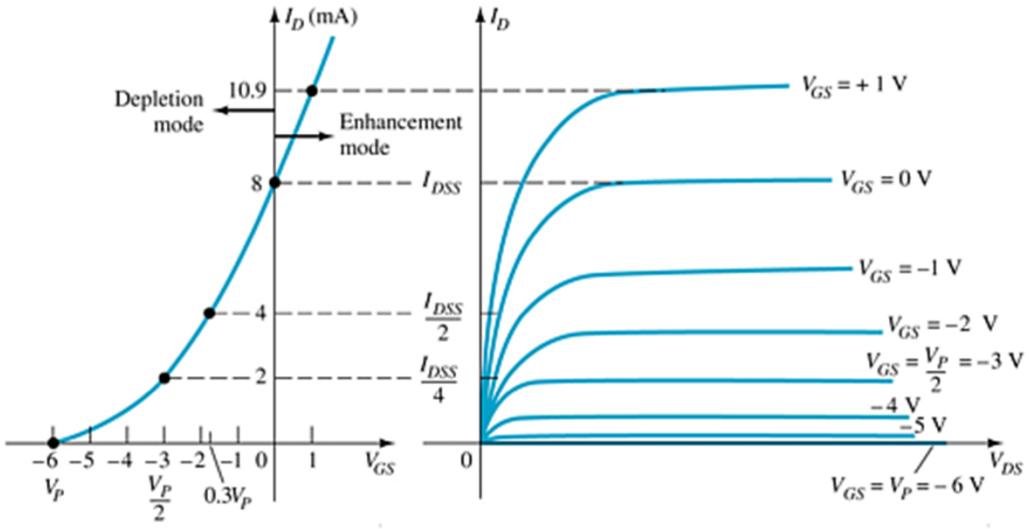
- **Depletion mode**
- **Enhancement mode**



# D-Type MOSFET in Depletion Mode

## Depletion Mode

**The characteristics are similar to a JFET.**




- **When $V_{GS} = 0$ V, $I_D = I_{DSS}$**
- **When $V_{GS} < 0$ V, $I_D < I_{DSS}$**
- **The formula used to plot the transfer curve still applies:**

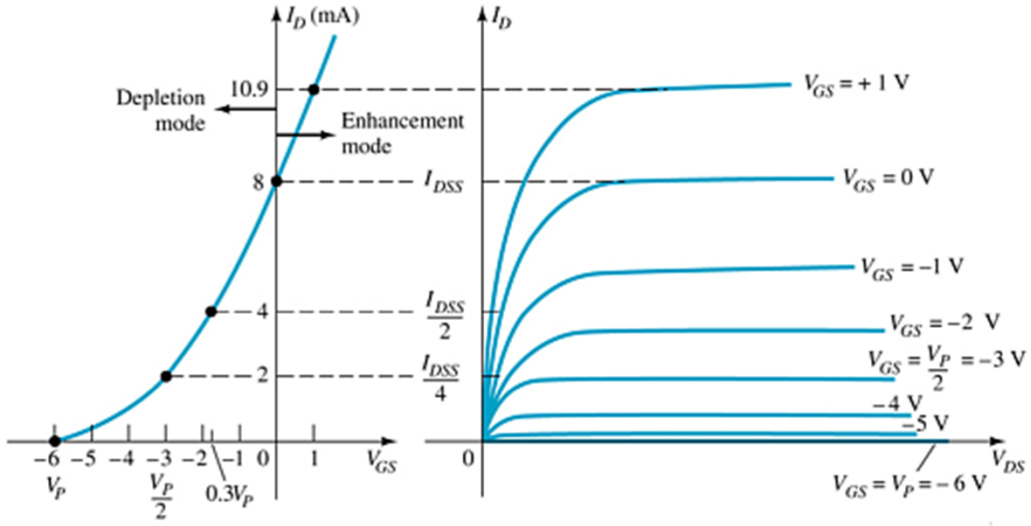
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

# D-Type MOSFET in Enhancement Mode

## Enhancement Mode

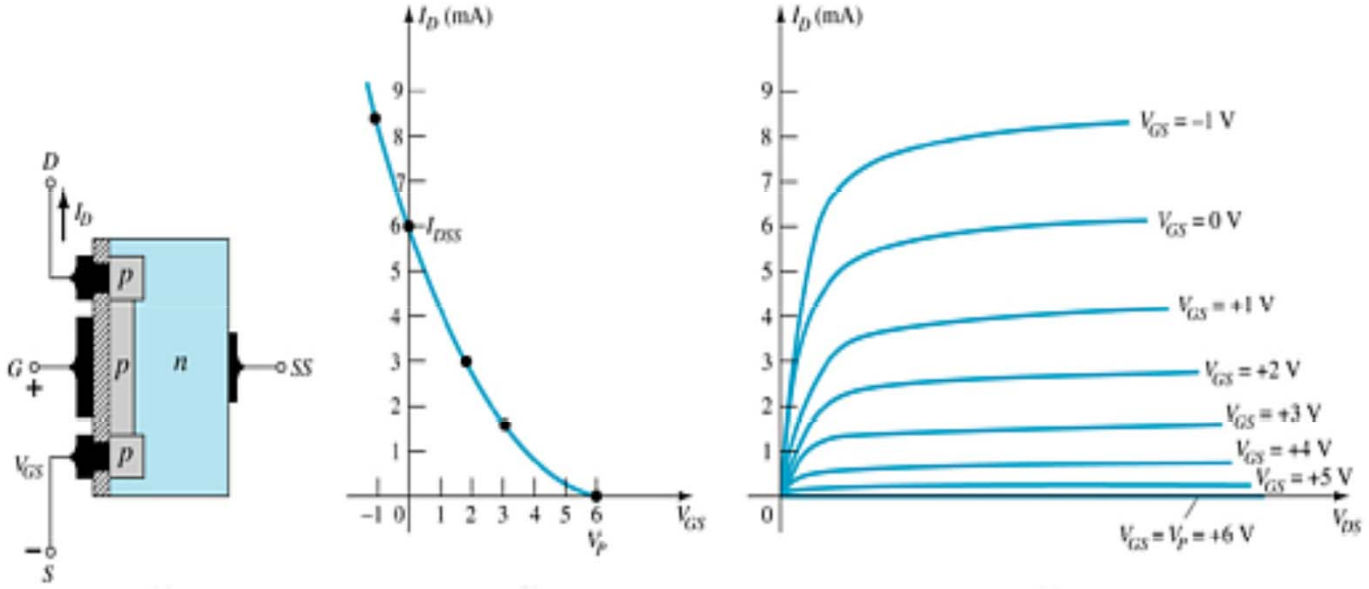
- $V_{GS} > 0$ V
- $I_D$ increases above $I_{DSS}$
- The formula used to plot the transfer curve still applies:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

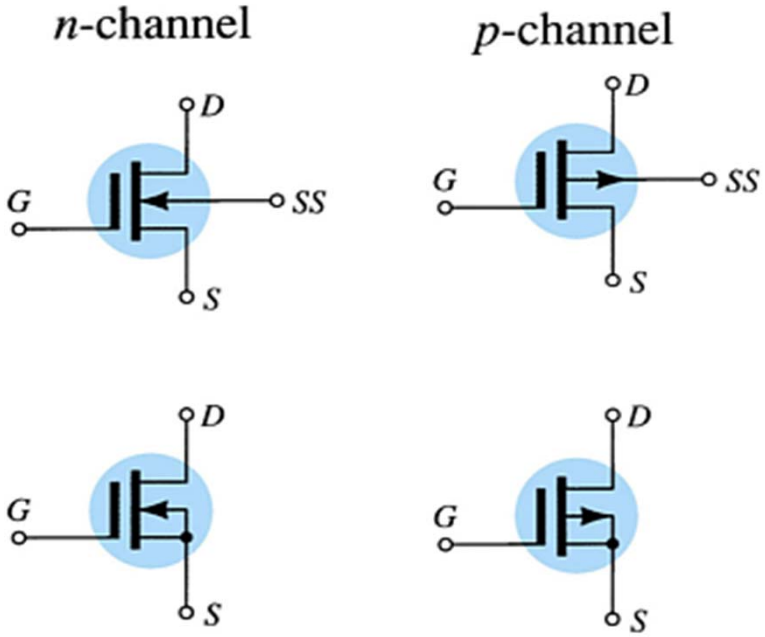



**Note that $V_{GS}$ is now a positive polarity**

# p-Channel D-Type MOSFET

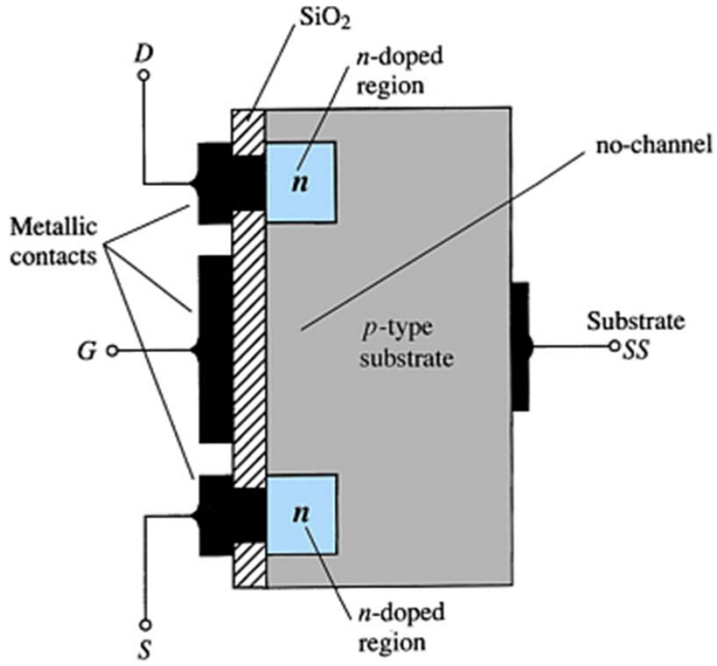


# D-Type MOSFET Symbols



# E-Type MOSFET Construction

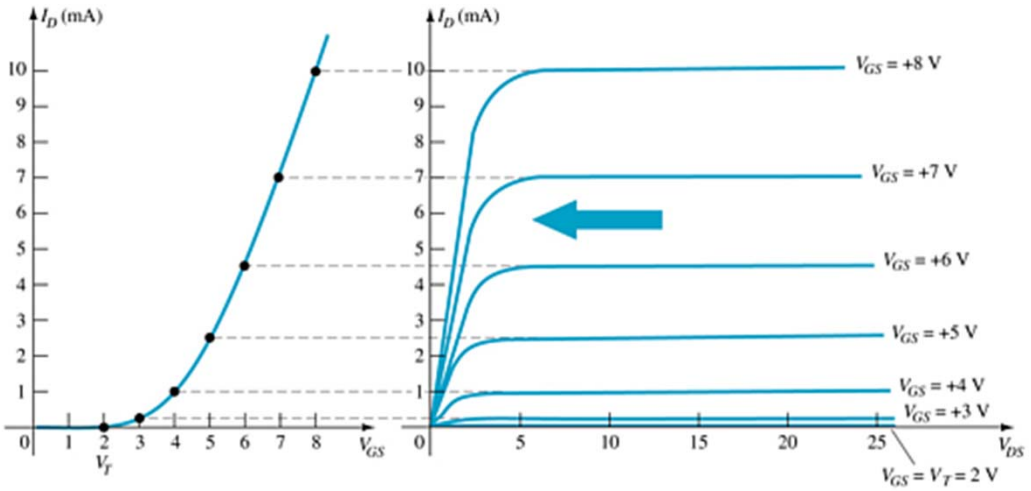
- **The Drain (D) and Source (S) connect to the to *n*-doped regions. These *n*-doped regions are connected via an *n*-channel**
- **The Gate (G) connects to the *p*-doped substrate via a thin insulating layer of $SiO_2$**
- **There is no channel**
- **The *n*-doped material lies on a *p*-doped substrate that may have an additional terminal connection called the Substrate (SS)**



# Basic Operation of the E-Type MOSFET

**The enhancement-type MOSFET operates only in the enhancement mode.**

- **$V_{GS}$ is always positive**
- **As $V_{GS}$ increases, $I_D$ increases**
- **As $V_{GS}$ is kept constant and $V_{DS}$ is increased, then $I_D$ saturates ($I_{DSS}$) and the saturation level, $V_{DSsat}$ is reached**



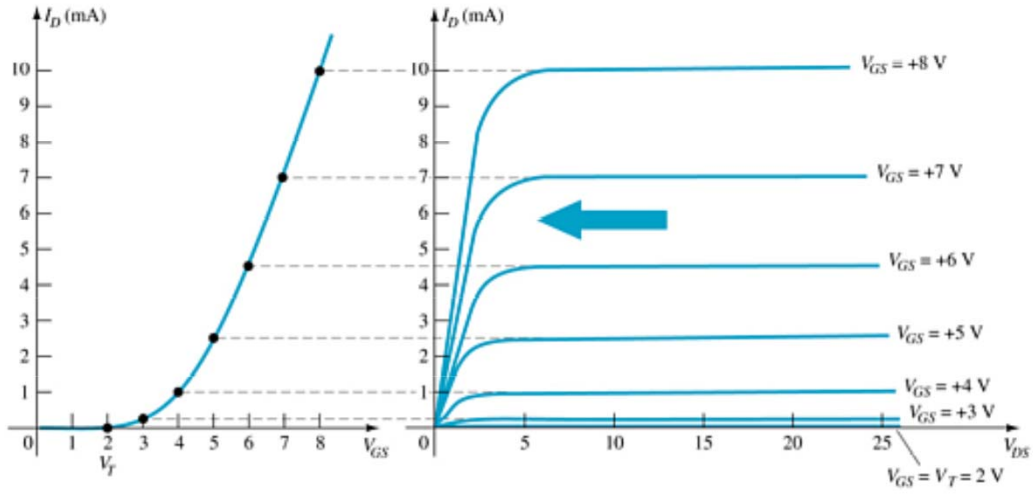
# E-Type MOSFET Transfer Curve

**To determine $I_D$ given $V_{GS}$:**

$$I_D = k(V_{GS} - V_T)^2$$

**Where:**

**$V_T$ = threshold voltage or voltage at which the MOSFET turns on**



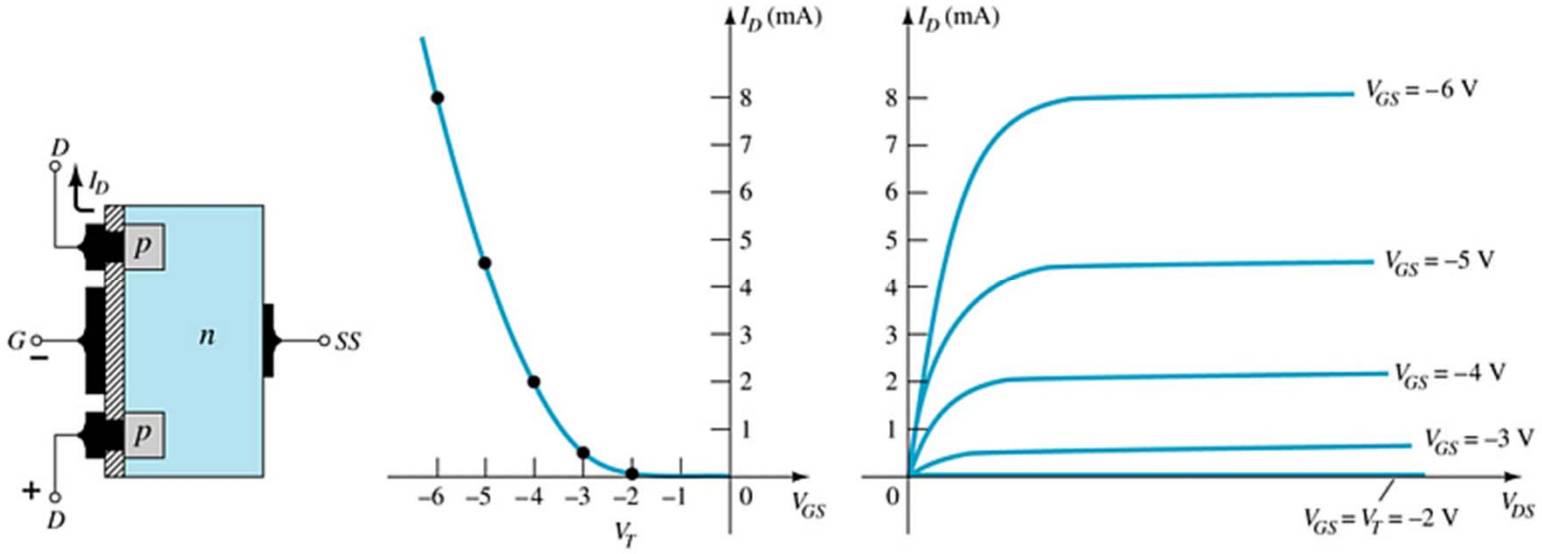

***k*, a constant, can be determined by using values at a specific point and the formula:**

$$k = \frac{I_{D(ON)}}{(V_{GS(ON)} - V_T)^2}$$

**$V_{DSsat}$ can be calculated by:**

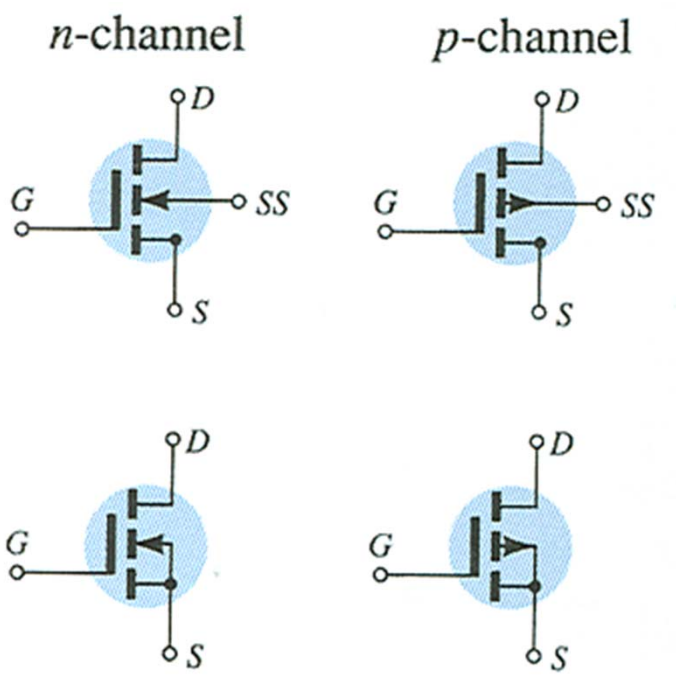
$$V_{Dsat} = V_{GS} - V_T$$

# p-Channel E-Type MOSFETs




**The *p*-channel enhancement-type MOSFET is similar to the *n*-channel, except that the voltage polarities and current directions are reversed.**

# MOSFET Symbols



# Handling MOSFETs

**MOSFETs are very sensitive to static electricity. Because of the very thin $SiO_2$ layer between the external terminals and the layers of the device, any small electrical discharge can create an unwanted conduction.**

## Protection

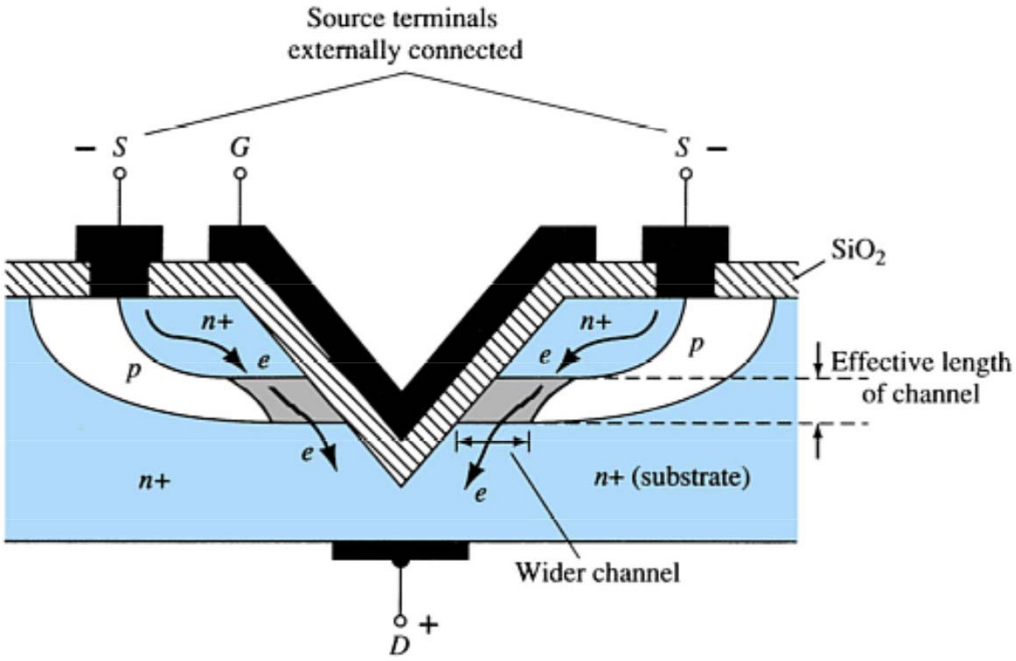
- **Always transport in a static sensitive bag**
- **Always wear a static strap when handling MOSFETS**
- 
- **Apply voltage limiting devices between the gate and source, such as back-to-back Zeners to limit any transient voltage.**

# VMOS Devices

**VMOS (vertical MOSFET) increases the surface area of the device.**

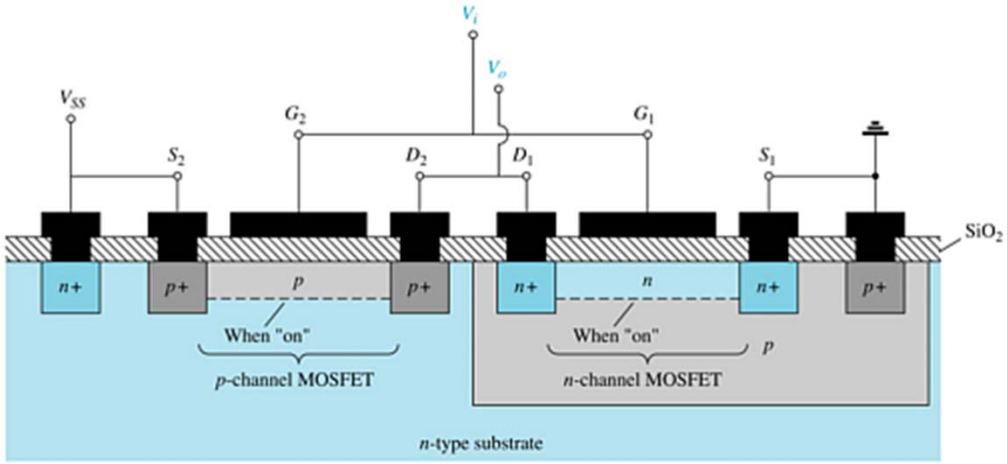
## Advantages

- **VMOS devices handle higher currents by providing more surface area to dissipate the heat.**
- **VMOS devices also have faster switching times.**



# CMOS Devices

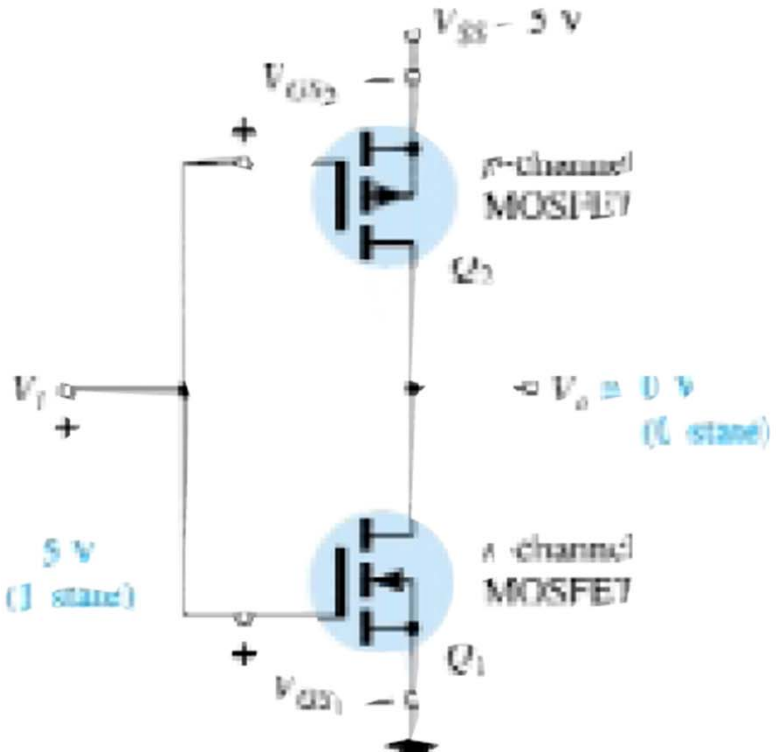
**CMOS (complementary MOSFET) uses a *p*-channel and *n*-channel MOSFET; often on the same substrate as shown here.**

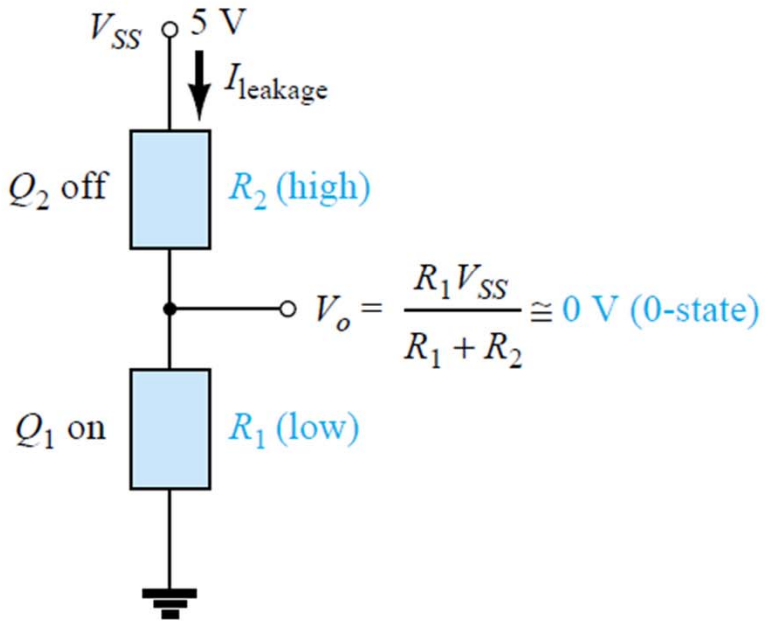



## Advantages

- **Useful in logic circuit designs**
- **Higher input impedance**
- **Faster switching speeds**
- **Lower operating power levels**

# CMOC Inverter



# Thank You!