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ACKNOWLEDGMENTS

Our sincerest appreciation must be extended to the instructors who have used the text and sent in comments, corrections, and suggestions. We also want to thank Rex Davidson and Kate Linsner at Prentice Hall for their editorial support of the ninth edition of this text.

We thank Penny Walker at GTS/Techbooks for her production coordination.

We wish to thank the countless individuals who have shared their suggestions and evaluations of this text throughout its many editions. Their comments and support have enabled us to present *Electronic Devices and Circuit Theory* in this new edition. In particular, we want to acknowledge the following reviewers for their valuable assistance in the preparation of this ninth edition:

Joseph Booker	DeVry University—DuPage Campus
Charles F. Bunting	Old Dominion University
Mauro J. Caputi	Hofstra University
Denton Dailey	Butler Community College
Kevin Ford	Alvin Community College
David Krispinsky	Rochester Institute of Technology
William Mack	Harrisburg Area Community College
John Sherrick	Rochester Institute of Technology

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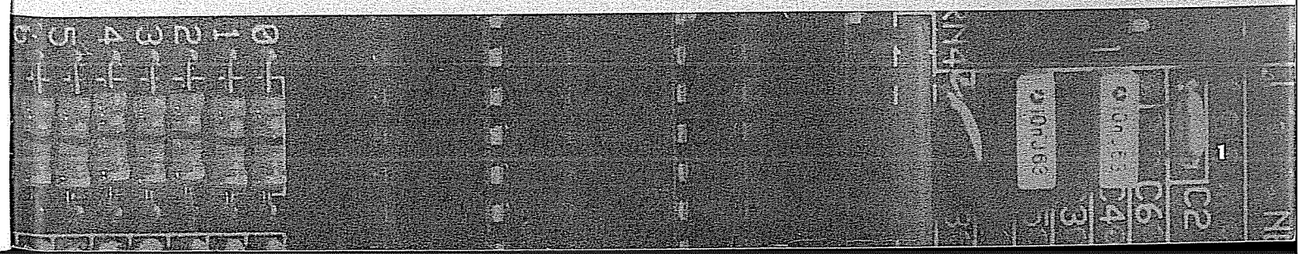
1 Semiconductor Diodes

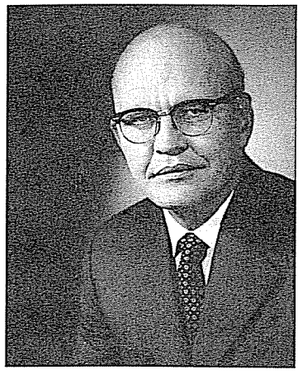
CHAPTER OUTLINE

1.1 Introduction
1.2 Semiconductor Materials: Ge, Si, and GaAs
1.3 Covalent Bonding and Intrinsic Materials
1.4 Energy Levels
1.5 Extrinsic Materials: *n*-Type and *p*-Type Materials
1.6 Semiconductor Diode
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1.1 INTRODUCTION

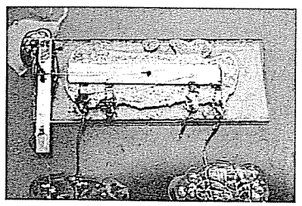
One of the noteworthy things about this field, as in many other areas of technology, is how little the fundamental principles change over time. Systems are incredibly smaller, current speeds of operation are truly remarkable, and new gadgets surface every day, leaving us to wonder where technology is taking us. However, if we take a moment to consider that the majority of all the devices in use were invented decades ago and that design techniques appearing in texts as far back as the 1930s are still in use, we realize that most of what we see is primarily a steady improvement in construction techniques and application of those devices rather than the development of new elements and fundamentally new designs. The result is that most of the devices discussed in this text have been around for some time, and that texts on the subject written a decade ago are still good references with content that has not changed very much. The major changes have been in the understanding of how these devices work and their full range of capabilities, and in improved methods of teaching the fundamentals associated with them. The benefit of all this to the new student of the subject





Jack St. Clair Kilby, inventor of the integrated circuit and co-inventor of the electronic handheld calculator. (Courtesy of Texas Instruments.)

Born: Jefferson City, Missouri, 1923. MS, University of Wisconsin. Director of Engineering and Technology, Components Group, Texas Instruments. Fellow of the IEEE. Holds more than 60 U.S. patents.



The first integrated circuit, a phase-shift oscillator, invented by Jack S. Kilby in 1958. (Courtesy of Texas Instruments.)

FIG. 1.1
Jack St. Clair Kilby.

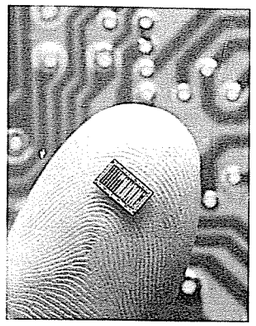


FIG. 1.2
Computer chip. (© Stock Photo/CORBIS.)

is that the material in this text will, we hope, have reached a level where it is relatively easy to grasp and the information will have application for years to come.

The miniaturization that has occurred in recent years leaves us to wonder about its limits. Complete systems now appear on wafers thousands of times smaller than the single element of earlier networks. The first integrated circuit (IC) was developed by Jack Kilby while working at Texas Instruments in 1958 (Fig. 1.1). Today, the Intel® Pentium® 4 processor shown in Fig. 1.2 has more than 42 million transistors and a host of other components. Recent advances suggest that 1 billion transistors will soon be placed on a sliver of silicon smaller than a fingernail. We have obviously reached a point where the primary purpose of the container is simply to provide some means for handling the device or system and to provide a mechanism for attachment to the remainder of the network. Further miniaturization appears to be limited by three factors: the quality of the semiconductor material, the network design technique, and the limits of the manufacturing and processing equipment.

The first device to be introduced here is the simplest of all electronic devices, yet has a range of applications that seems endless. We devote two chapters to the device to introduce the materials commonly used in solid-state devices and review some fundamental laws of electric circuits.

1.2 SEMICONDUCTOR MATERIALS: Ge, Si, and GaAs

The construction of every discrete (individual) solid-state (hard crystal structure) electronic device or integrated circuit begins with a semiconductor material of the highest quality.

Semiconductors are a special class of elements having a conductivity between that of a good conductor and that of an insulator.

In general, semiconductor materials fall into one of two classes: *single-crystal* and *compound*. Single-crystal semiconductors such as germanium (Ge) and silicon (Si) have a repetitive crystal structure, whereas compound semiconductors such as gallium arsenide (GaAs), cadmium sulfide (CdS), gallium nitride (GaN), and gallium arsenide phosphide (GaAsP) are constructed of two or more semiconductor materials of different atomic structures.

The three semiconductors used most frequently in the construction of electronic devices are Ge, Si, and GaAs.

In the first few decades following the discovery of the diode in 1939 and the transistor in 1947 germanium was used almost exclusively because it was relatively easy to find and was available in fairly large quantities. It was also relatively easy to refine to obtain very high levels of purity, an important aspect in the fabrication process. However, it was discovered in the early years that diodes and transistors constructed using germanium as the base material suffered from low levels of reliability due primarily to its sensitivity to changes in temperature. At the time, scientists were aware that another material, silicon, had improved temperature sensitivities, but the refining process for manufacturing silicon of very high levels of purity was still in the development stages. Finally, however, in 1954 the first silicon transistor was introduced, and silicon quickly became the semiconductor material of choice. Not only is silicon less temperature sensitive, but it is one of the most abundant materials on earth, removing any concerns about availability. The flood gates now opened to this new material, and the manufacturing and design technology improved steadily through the following years to the current high level of sophistication.

As time moved on, however, the field of electronics became increasingly sensitive to issues of speed. Computers were operating at higher and higher speeds, and communication systems were operating at higher levels of performance. A semiconductor material capable of meeting these new needs had to be found. The result was the development of the first GaAs transistor in the early 1970s. This new transistor had speeds of operation up to five times that of Si. The problem, however, was that because of the years of intense design efforts and manufacturing improvements using Si, Si transistor networks for most applications were cheaper to manufacture and had the advantage of highly efficient design strategies. GaAs was more difficult to manufacture at high levels of purity, was more expensive, and had little design support in the early years of development. However, in time the demand for increased speed resulted in more funding for GaAs research, to the point that today it is consistently used as the base material for new high-speed, very large scale integrated (VLSI) circuit designs.

This brief review of the history of semiconductor materials is not meant to imply that GaAs will soon be the only material appropriate for solid-state construction. Germanium devices are still being manufactured, although for a limited range of applications. Even though it is a temperature-sensitive semiconductor, it does have characteristics that find application in a limited number of areas. Given its availability and low manufacturing costs, it will continue to find its place in product catalogs. As noted earlier, Si has the benefit of years of development, and is the leading semiconductor material for electronic components and ICs. GaAs is more expensive, but as manufacturing processes improve and demands for higher speeds increase, it will begin to challenge Si as the dominant semiconductor material.

1.3 COVALENT BONDING AND INTRINSIC MATERIALS

To fully appreciate why Si, Ge, and GaAs are the semiconductors of choice for the electronics industry requires some understanding of the atomic structure of each and how the atoms are bound together to form a crystalline structure. Every atom is composed of three basic particles: the electron, the proton, and the neutron. In the lattice structure, neutrons and protons form the nucleus and electrons appear in fixed orbits around the nucleus. The Bohr model for the three materials is provided in Fig. 1.3.

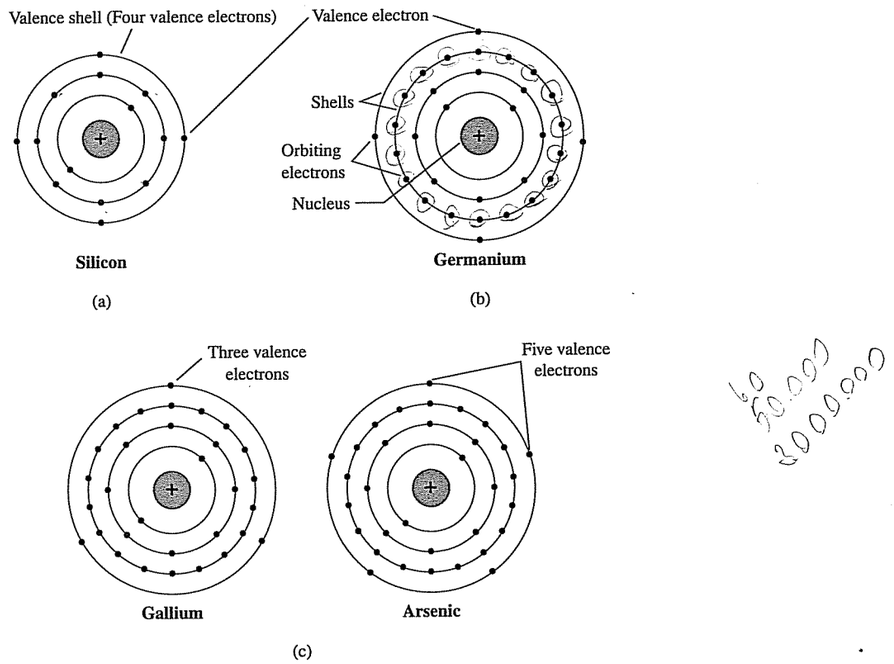


FIG. 1.3
Atomic structure of (a) silicon; (b) germanium; and (c) gallium and arsenic.

As indicated in Fig. 1.3, silicon has 14 orbiting electrons, germanium has 32 electrons, gallium has 31 electrons, and arsenic has 33 orbiting electrons (the same arsenic that is a very poisonous chemical agent). For germanium and silicon there are four electrons in the outermost shell, which are referred to as *valence electrons*. Gallium has three valence electrons and arsenic has five valence electrons. Atoms that have four valence electrons are called *tetravalent*, those with three are called *trivalent*, and those with five are called *pentavalent*. The term *valence* is used to indicate that the potential (ionization potential) required to remove any one of these electrons from the atomic structure is significantly lower than that required for any other electron in the structure.

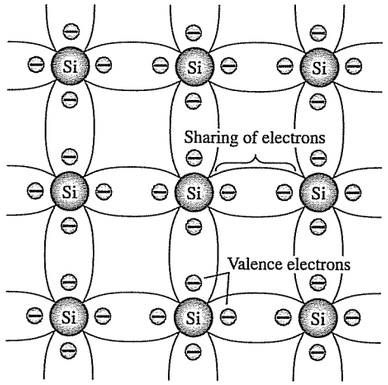


FIG. 1.4
Covalent bonding of the silicon atom.

In a pure silicon or germanium crystal the four valence electrons of one atom form a bonding arrangement with four adjoining atoms, as shown in Fig. 1.4.

This bonding of atoms, strengthened by the sharing of electrons, is called covalent bonding.

Because GaAs is a compound semiconductor, there is sharing between the two different atoms, as shown in Fig. 1.5. Each atom is surrounded by atoms of the complementary type. There is still a sharing of electrons similar in structure to that of Ge and Si, but now five electrons are provided by the As atom and three by the Ga atom.

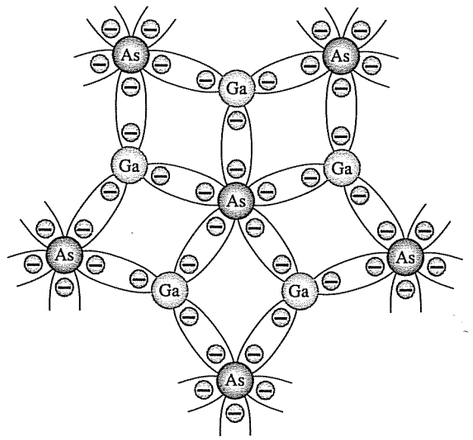


FIG. 1.5
Covalent bonding of the GaAs crystal.

Although the covalent bond will result in a stronger bond between the valence electrons and their parent atom, it is still possible for the valence electrons to absorb sufficient kinetic energy from external natural causes to break the covalent bond and assume the "free" state. The term *free* is applied to any electron that has separated from the fixed lattice structure and is very sensitive to any applied electric fields such as established by voltage sources or any difference in potential. *The external causes include effects such as light energy in the form of photons and thermal energy (heat) from the surrounding medium.* At room temperature there are approximately 1.5×10^{10} free carriers in 1 cm^3 of *intrinsic* silicon material, that is, 15,000,000,000 (15 billion) electrons in a space smaller than a small sugar cube—an enormous number.

The term intrinsic is applied to any semiconductor material that has been carefully refined to reduce the number of impurities to a very low level—essentially as pure as can be made available through modern technology.

The free electrons in a material due only to external causes are referred to as *intrinsic carriers*. Table 1.1 compares the number of intrinsic carriers per cubic centimeter for Ge, Si, and GaAs. It is interesting to note that Ge has the highest number and GaAs the lowest. In fact, Ge has more than twice the number as GaAs. The number of carriers in the intrinsic form is important, but other characteristics of the material are more significant in determining its use in the field. One such factor is the *relative mobility* (μ_n) of the free carriers in the material, that is, the ability of the free carriers to move throughout the material. Table 1.2 clearly reveals that the free carriers in GaAs have more than five times the mobility of free carriers in Si, a factor that results in response times using GaAs electronic devices that can be up to five times those of the same devices made from Si. Note also that free carriers in Ge have more than twice the mobility of electrons in Si, a factor that results in the continued use of Ge in high-speed radio frequency applications.

TABLE 1.1
Intrinsic Carriers

Semiconductor	Intrinsic Carriers (per cubic centimeter)
GaAs	1.7×10^6
Si	1.5×10^{10}
Ge	2.5×10^{13}

TABLE 1.2
Relative Mobility Factor μ_n

Semiconductor	μ_n (cm^2/V-s)
Si	1500
Ge	3900
GaAs	8500

One of the most important technological advances of recent decades has been the ability to produce semiconductor materials of very high purity. Recall that this was one of the problems encountered in the early use of silicon—it was easier to produce germanium of the required purity levels. Impurity levels of 1 part in 10 billion are common today, with higher levels attainable for large-scale integrated circuits. One might ask whether these extremely high levels of purity are necessary. They certainly are if one considers that the addition of one part of impurity (of the proper type) per million in a wafer of silicon material can change that material from a relatively poor conductor to a good conductor of electricity. We obviously have to deal with a whole new level of comparison when we deal with the semiconductor medium. The ability to change the characteristics of a material through this process is called *doping*, something that germanium, silicon, and gallium arsenide readily and easily accept. The doping process is discussed in detail in Sections 1.5 and 1.6.

One important and interesting difference between semiconductors and conductors is their reaction to the application of heat. For conductors, the resistance increases with an increase in heat. This is because the numbers of carriers in a conductor do not increase significantly with temperature, but their vibration pattern about a relatively fixed location makes it increasingly difficult for a sustained flow of carriers through the material. Materials that react in this manner are said to have a *positive temperature coefficient*. Semiconductor materials, however, exhibit an increased level of conductivity with the application of heat. As the temperature rises, an increasing number of valence electrons absorb sufficient thermal energy to break the covalent bond and to contribute to the number of free carriers. Therefore:

Semiconductor materials have a negative temperature coefficient.

1.4 ENERGY LEVELS

Within the atomic structure of each and every *isolated* atom there are specific energy levels associated with each shell and orbiting electron, as shown in Fig. 1.6. The energy levels associated with each shell will be different for every element. However, in general:

The farther an electron is from the nucleus, the higher is the energy state, and any electron that has left its parent atom has a higher energy state than any electron in the atomic structure.

Note in Fig. 1.6a that only specific energy levels can exist for the electrons in the atomic structure of an isolated atom. The result is a series of gaps between allowed energy levels

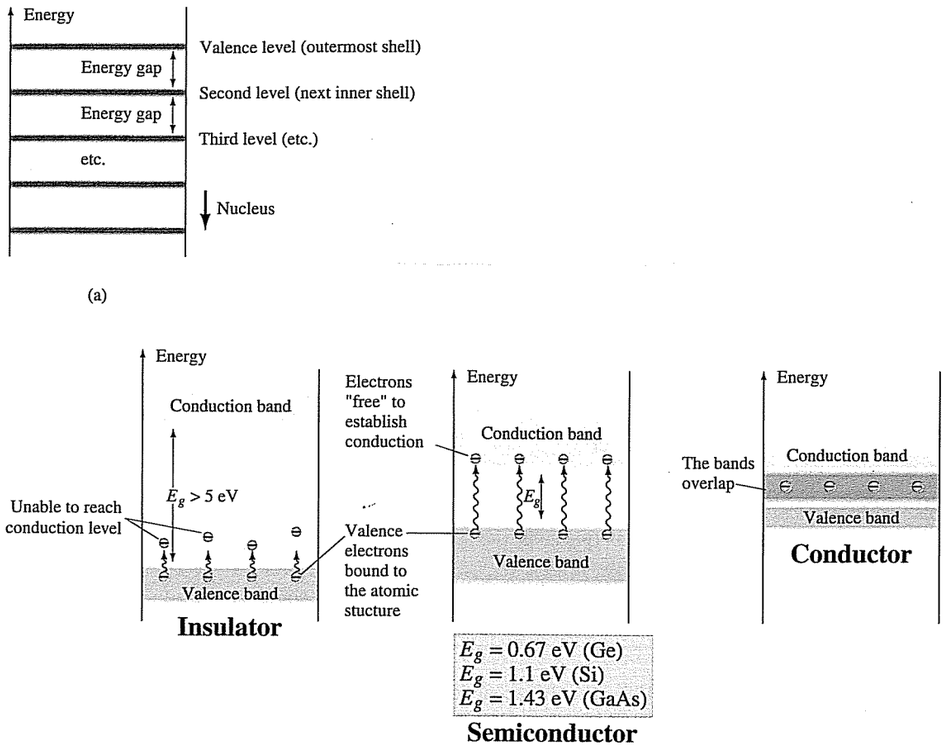


FIG. 1.6

Energy levels: (a) discrete levels in isolated atomic structures; (b) conduction and valence bands of an insulator, a semiconductor, and a conductor.

where carriers are not permitted. However, as the atoms of a material are brought closer together to form the crystal lattice structure, there is an interaction between atoms, which will result in the electrons of a particular shell of an atom having slightly different energy levels from electrons in the same orbit of an adjoining atom. The result is an expansion of the fixed, discrete energy levels of the valence electrons of Fig. 1.6a to bands as shown in Fig. 1.6b. In other words, the valence electrons in a silicon material can have varying energy levels as long as they fall within the band of Fig. 1.6b. Figure 1.6b clearly reveals that there is a minimum energy level associated with electrons in the conduction band and a maximum energy level of electrons bound to the valence shell of the atom. Between the two is an energy gap that the electron in the valence band must overcome to become a free carrier. That energy gap is different for Ge, Si, and GaAs; Ge has the smallest gap and GaAs the largest gap. In total, this simply means that:

An electron in the valence band of silicon must absorb more energy than one in the valence band of germanium to become a free carrier. Similarly, an electron in the valence band of gallium arsenide must gain more energy than one in silicon or germanium to enter the conduction band.

This difference in energy gap requirements reveals the sensitivity of each type of semiconductor to changes in temperature. For instance, as the temperature of a Ge sample increases, the number of electrons that can pick up thermal energy and enter the conduction band will increase quite rapidly because the energy gap is quite small. However, the number of electrons entering the conduction band for Si, or GaAs would be a great deal less. This sensitivity to changes in energy level can have positive and negative affects. The design of photodetectors sensitive to light and security systems sensitive to heat would appear to be an excellent area of application for Ge devices. However, for transistor networks, where stability is a high priority, this sensitivity to temperature or light can be a detrimental factor.

The energy gap also reveals which elements are useful in the construction of light-emitting devices such as light-emitting diodes (LEDs), which will be introduced shortly. The wider the energy gap, the greater is the possibility of energy being released in the form of visible or invisible (infrared) light waves. For conductors, the overlapping of valence and conduction bands essentially results in all the additional energy picked up by the electrons being dissipated in the form of heat. Similarly, for Ge and Si, because the energy gap is so small, most of the electrons that pick up sufficient energy to leave the valence band end up in the conduction band, and the energy is dissipated in the form of heat. However, for GaAs the gap is sufficiently large to result in significant light radiation. For LEDs (Section 1.9) the level of doping and the materials chosen determine the resulting color.

Before we leave this subject, it is important to underscore the importance of understanding the units used for a quantity. In Fig. 1.6 the units of measurement are *electron volts* (eV). The unit of measure is appropriate because W (energy) $= QV$ (as derived from the defining equation for voltage: $V = W/Q$). Substituting the charge of one electron and a potential difference of 1 V results in an energy level referred to as one *electron volt*.

1.5 EXTRINSIC MATERIALS: *n*-TYPE AND *p*-TYPE MATERIALS

Because Si is the material used most frequently as the base (substrate) material in the construction of solid-state electronic devices, the discussion to follow in this and the next few sections deals solely with Si semiconductors. Because Ge, Si, and GaAs share a similar covalent bonding, the discussion can easily be extended to include the use of the other materials in the manufacturing process.

As indicated earlier, the characteristics of a semiconductor material can be altered significantly by the addition of specific impurity atoms to the relatively pure semiconductor material. These impurities, although only added at 1 part in 10 million, can alter the band structure sufficiently to totally change the electrical properties of the material.

A semiconductor material that has been subjected to the doping process is called an extrinsic material.

There are two extrinsic materials of immeasureable importance to semiconductor device fabrication: *n*-type and *p*-type materials. Each is described in some detail in the following subsections.

n-Type Material

Both *n*-type and *p*-type materials are formed by adding a predetermined number of impurity atoms to a silicon base. An *n*-type material is created by introducing impurity elements that have *five* valence electrons (*pentavalent*), such as *antimony*, *arsenic*, and *phosphorus*. The effect of such impurity elements is indicated in Fig. 1.7 (using antimony as the impurity in a silicon base). Note that the four covalent bonds are still present. There

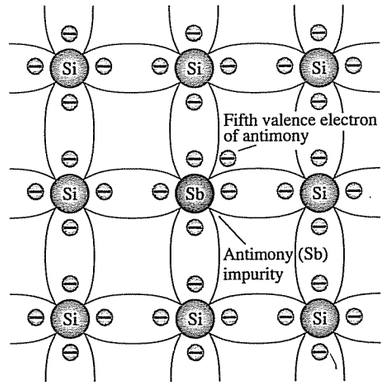


FIG. 1.7

Antimony impurity in n-type material.

is, however, an additional fifth electron due to the impurity atom, which is *unassociated* with any particular covalent bond. This remaining electron, loosely bound to its parent (antimony) atom, is relatively free to move within the newly formed *n*-type material. Since the inserted impurity atom has donated a relatively "free" electron to the structure:

Diffused impurities with five valence electrons are called donor atoms.

It is important to realize that even though a large number of free carriers have been established in the *n*-type material, it is still electrically *neutral* since ideally the number of positively charged protons in the nuclei is still equal to the number of free and orbiting negatively charged electrons in the structure.

The effect of this doping process on the relative conductivity can best be described through the use of the energy-band diagram of Fig. 1.8. Note that a discrete energy level (called the *donor level*) appears in the forbidden band with an E_g significantly less than that of the intrinsic material. Those free electrons due to the added impurity sit at this energy level and have less difficulty absorbing a sufficient measure of thermal energy to move into the conduction band at room temperature. The result is that at room temperature, there are a large number of carriers (electrons) in the conduction level, and the conductivity of the material increases significantly. At room temperature in an intrinsic Si material there is about one free electron for every 10^{12} atoms. If the dosage level is 1 in 10 million (10^7), the ratio $10^{12}/10^7 = 10^5$ indicates that the carrier concentration has increased by a ratio of 100,000:1.

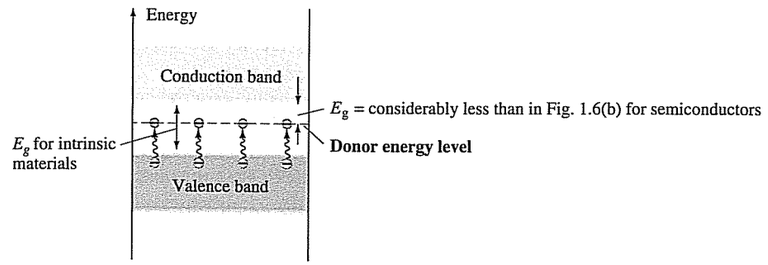


FIG. 1.8
Effect of donor impurities on the energy band structure.

p-Type Material

The *p*-type material is formed by doping a pure germanium or silicon crystal with impurity atoms having *three* valence electrons. The elements most frequently used for this purpose are *boron*, *gallium*, and *indium*. The effect of one of these elements, boron, on a base of silicon is indicated in Fig. 1.9.

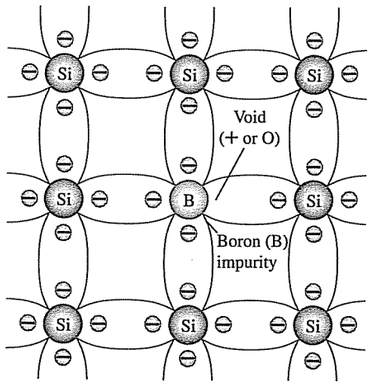


FIG. 1.9
Boron impurity in p-type material.

Note that there is now an insufficient number of electrons to complete the covalent bonds of the newly formed lattice. The resulting vacancy is called a *hole* and is represented by a small circle or a plus sign, indicating the absence of a negative charge. Since the resulting vacancy will readily *accept* a free electron:

The diffused impurities with three valence electrons are called acceptor atoms.

The resulting *p*-type material is electrically neutral, for the same reasons described for the *n*-type material.

Electron versus Hole Flow

The effect of the hole on conduction is shown in Fig. 1.10. If a valence electron acquires sufficient kinetic energy to break its covalent bond and fills the void created by a hole, then a vacancy, or hole, will be created in the covalent bond that released the electron. There is, therefore, a transfer of holes to the left and electrons to the right, as shown in Fig. 1.10. The direction to be used in this text is that of *conventional flow*, which is indicated by the direction of hole flow.

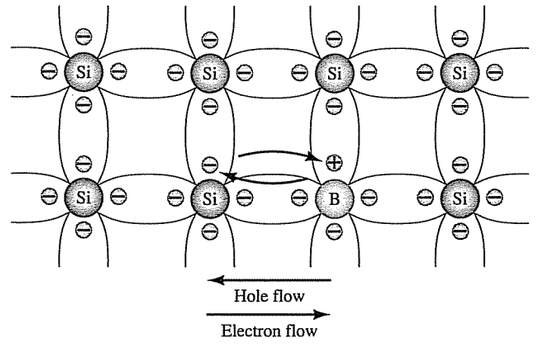


FIG. 1.10
Electron versus hole flow.

Majority and Minority Carriers

In the intrinsic state, the number of free electrons in Ge or Si is due only to those few electrons in the valence band that have acquired sufficient energy from thermal or light sources to break the covalent bond or to the few impurities that could not be removed. The vacancies left behind in the covalent bonding structure represent our very limited supply of holes. In an *n*-type material, the number of holes has not changed significantly from this intrinsic level. The net result, therefore, is that the number of electrons far outweighs the number of holes. For this reason:

In an n-type material (Fig. 1.11a) the electron is called the majority carrier and the hole the minority carrier.

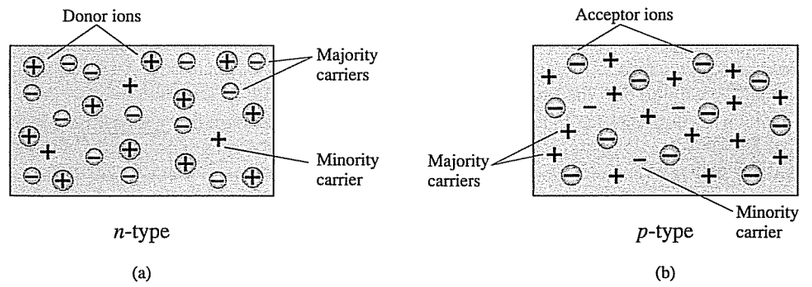


FIG. 1.11
(a) n-type material; (b) p-type material.

For the *p*-type material the number of holes far outweighs the number of electrons, as shown in Fig. 1.11b. Therefore:

In a p-type material the hole is the majority carrier and the electron is the minority carrier.

When the fifth electron of a donor atom leaves the parent atom, the atom remaining acquires a net positive charge: hence the plus sign in the donor-ion representation. For similar reasons, the minus sign appears in the acceptor ion.

The *n*- and *p*-type materials represent the basic building blocks of semiconductor devices. We will find in the next section that the "joining" of a single *n*-type material with a *p*-type material will result in a semiconductor element of considerable importance in electronic systems.

1.6 SEMICONDUCTOR DIODE

Now that both *n*- and *p*-type materials are available, we can construct our first solid-state electronic device. The *semiconductor diode*, with applications too numerous to mention, is created by simply joining an *n*-type and a *p*-type material together, nothing more, just the joining of one material with a majority carrier of electrons to one with a majority carrier of holes. The basic simplicity of its construction simply reinforces the importance of the development of this solid-state era.

No Applied Bias ($V = 0$ V)

At the instant the two materials are "joined" the electrons and the holes in the region of the junction will combine, resulting in a lack of free carriers in the region near the junction, as shown in Fig. 1.12a. Note in Fig. 1.12a that the only particles displayed in this region are the positive and the negative ions remaining once the free carriers have been absorbed.

This region of uncovered positive and negative ions is called the depletion region due to the "depletion" of free carriers in the region.

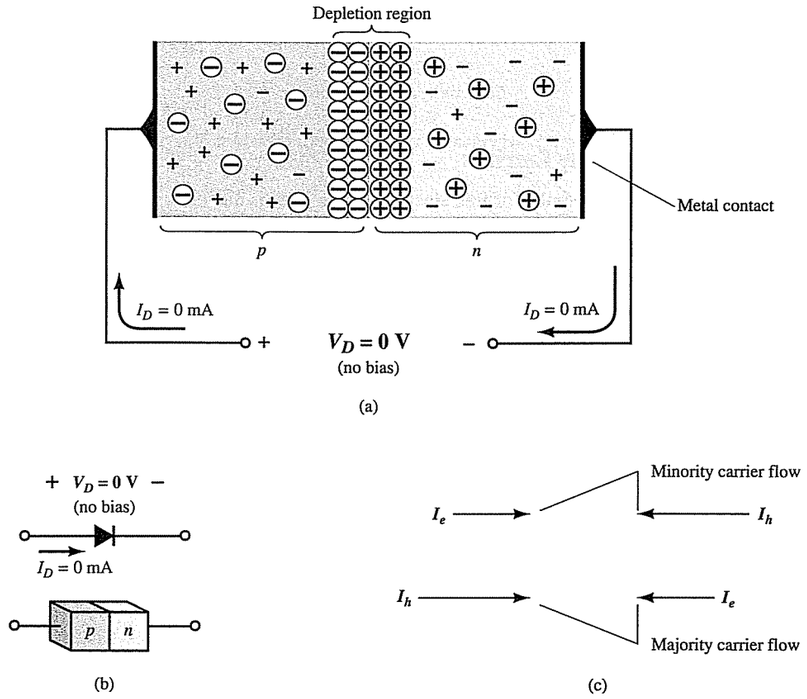


FIG. 1.12

A p–n junction with no external bias. (a) An internal distribution of charge; (b) a diode symbol, with the defined polarity and the current direction; (c) demonstration that the net carrier flow is zero at the external terminal of the device when $V_D = 0$ V.

If leads are connected to the ends of each material, a *two-terminal device* results, as shown in Figs. 1.12a and 1.12b. Three options then become available: *no bias*, *forward bias*, and *reverse bias*. The term *bias* refers to the application of an external voltage across the two terminals of the device to extract a response. The condition shown in Figs. 1.12a and 1.12b is the no-bias situation because there is no external voltage applied. It is simply a diode with two leads sitting isolated on a laboratory bench. In Fig. 1.12b the symbol for a semiconductor diode is provided to show its correspondence with the *p–n* junction. In each figure it is clear that the applied voltage is 0 V (no bias) and the resulting current is 0 A, much like an isolated resistor. The absence of a voltage across a resistor results in zero current through it. Even at this early point in the discussion it is important to note the polarity of the voltage across the diode in Fig. 1.12b and the direction given to the current. Those polarities will be recognized as the *defined polarities* for the semiconductor diode. If a voltage applied across the diode has the same polarity across the diode as in Fig. 1.12b, it will be considered a positive voltage. If the reverse, it is a negative voltage. The same standards can be applied to the defined direction of current in Fig. 1.12b.

Under no-bias conditions, any minority carriers (holes) in the *n*-type material that find themselves within the depletion region for any reason whatsoever will pass quickly into the *p*-type material. The closer the minority carrier is to the junction, the greater is the attraction for the layer of negative ions and the less is the opposition offered by the positive ions in the depletion region of the *n*-type material. We will conclude, therefore, for future discussions, that any minority carriers of the *n*-type material that find themselves in the depletion region will pass directly into the *p*-type material. This carrier flow is indicated at the top of Fig. 1.12c for the minority carriers of each material.

The majority carriers (electrons) of the *n*-type material must overcome the attractive forces of the layer of positive ions in the *n*-type material and the shield of negative ions in the *p*-type material to migrate into the area beyond the depletion region of the *p*-type material. However, the number of majority carriers is so large in the *n*-type material that there will invariably be a small number of majority carriers with sufficient kinetic energy to pass through the depletion region into the *p*-type material. Again, the same type of discussion can be applied to the majority carriers (holes) of the *p*-type material. The resulting flow due to the majority carriers is shown at the bottom of Fig. 1.12c.

A close examination of Fig. 1.12c will reveal that the relative magnitudes of the flow vectors are such that the net flow in either direction is zero. This cancellation of vectors for each type of carrier flow is indicated by the crossed lines. The length of the vector representing hole flow is drawn longer than that of electron flow to demonstrate that the two magnitudes need not be the same for cancellation and that the doping levels for each material may result in an unequal carrier flow of holes and electrons. In summary, therefore:

In the absence of an applied bias across a semiconductor diode, the net flow of charge in one direction is zero.

In other words, the current under no-bias conditions is zero, as shown in Figs. 1.12a and 1.12b.

Reverse-Bias Condition ($V_D < 0$ V)

If an external potential of V volts is applied across the *p–n* junction such that the positive terminal is connected to the *n*-type material and the negative terminal is connected to the *p*-type material as shown in Fig. 1.13, the number of uncovered positive ions in the depletion region of the *n*-type material will increase due to the large number of free electrons drawn to the positive potential of the applied voltage. For similar reasons, the number of uncovered negative ions will increase in the *p*-type material. The net effect, therefore, is a widening of the depletion region. This widening of the depletion region will establish too great a barrier for the majority carriers to overcome, effectively reducing the majority carrier flow to zero, as shown in Fig. 1.13a.

The number of minority carriers, however, entering the depletion region will not change, resulting in minority-carrier flow vectors of the same magnitude indicated in Fig. 1.12c with no applied voltage.

The current that exists under reverse-bias conditions is called the reverse saturation current and is represented by I_s.

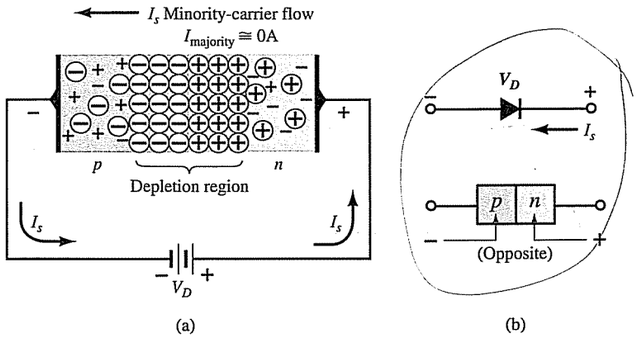


FIG. 1.13

Reverse-biased p–n junction. (a) Internal distribution of charge under reverse-bias conditions; (b) reverse-bias polarity and direction of reverse saturation current.

The reverse saturation current is seldom more than a few microamperes, except for high-power devices. In fact, in recent years its level is typically in the nanoampere range for silicon devices. The term *saturation* comes from the fact that it reaches its maximum level quickly and does not change significantly with increases in the reverse-bias potential, as shown on the diode characteristics of Fig. 1.15 for $V_D < 0$ V. The reverse-biased conditions are depicted in Fig. 1.13b for the diode symbol and *p–n* junction. Note, in particular, that the direction of I_s is against the arrow of the symbol. Note also that the negative side of the applied voltage is connected to the *p*-type material and the positive side to the *n*-type material, the difference in underlined letters for each region revealing a reverse-bias condition.

Forward-Bias Condition ($V_D > 0$ V)

A *forward-bias* or "on" condition is established by applying the positive potential to the *p*-type material and the negative potential to the *n*-type material as shown in Fig. 1.14.

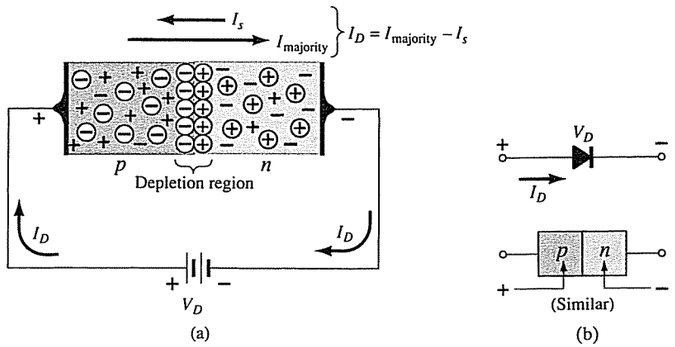


FIG. 1.14

Forward-biased p–n junction. (a) Internal distribution of charge under forward-bias conditions; (b) forward-bias polarity and direction of resulting current.

The application of a forward-bias potential V_D will "pressure" electrons in the *n*-type material and holes in the *p*-type material to recombine with the ions near the boundary and reduce the width of the depletion region as shown in Fig. 1.14a. The resulting minority-carrier flow of electrons from the *p*-type material to the *n*-type material (and of holes from the *n*-type material to the *p*-type material) has not changed in magnitude (since the conduction level is controlled primarily by the limited number of impurities in the material), but the reduction in the width of the depletion region has resulted in a heavy majority flow

across the junction. An electron of the *n*-type material now "sees" a reduced barrier at the junction due to the reduced depletion region and a strong attraction for the positive potential applied to the *p*-type material. As the applied bias increases in magnitude, the depletion region will continue to decrease in width until a flood of electrons can pass through the junction, resulting in an exponential rise in current as shown in the forward-bias region of the characteristics of Fig. 1.15. Note that the vertical scale of Fig. 1.15 is measured in milliamperes (although some semiconductor diodes have a vertical scale measured in amperes), and the horizontal scale in the forward-bias region has a maximum of 1 V. Typically, therefore, the voltage across a forward-biased diode will be less than 1 V. Note also how quickly the current rises beyond the knee of the curve.

It can be demonstrated through the use of solid-state physics that the general characteristics of a semiconductor diode can be defined by the following equation, referred to as Shockley's equation, for the forward- and reverse-bias regions:

$$\boxed{I_D = I_s(e^{V_D/nV_T} - 1)} \quad \text{(A)} \tag{1.1}$$

where I_s is the reverse saturation current
V_D is the applied forward-bias voltage across the diode
n is an ideality factor, which is a function of the operating conditions and physical construction; it has a range between 1 and 2 depending a wide variety of factors ($n = 1$ will be assumed throughout this text unless otherwise noted).

The voltage V_T in Eq. (1.1) is called the *thermal voltage* and is determined by

$$\boxed{V_T = \frac{kT}{q}} \quad \text{(V)} \tag{1.2}$$

where k is Boltzmann's constant $= 1.38 \times 10^{-23}$ J/K
T is the absolute temperature in kelvins $= 273 +$ the temperature in °C
q is the magnitude of electronic charge $= 1.6 \times 10^{-19}$ C

EXAMPLE 1.1 At a temperature of 27°C (common temperature for components in an enclosed operating system), determine the thermal voltage V_T.

Solution: Substituting into Eq. (1.2), we obtain

$$T = 273 + °C = 273 + 27 = 300\,K$$

$$V_T = \frac{kT}{q} = \frac{(1.38 \times 10^{-23}\,J/K)(300)}{1.6 \times 10^{-19}\,C}$$

$$= \mathbf{25.875\,mV \cong 26\,mV}$$

The thermal voltage will become an important parameter in the analysis to follow in this chapter and a number of those to follow.

Initially, Eq. (1.1) with all its defined quantities may appear somewhat complex. However, it will not be used extensively in the analysis to follow. It is simply important at this point to understand the source of the diode characteristics and which factors affect its shape.

A plot of Eq. (1.1) with $I_s = 10$ pA is provided in Fig. 1.15 as the dashed line. If we expand Eq. (1.1) into the following form, the contributing component for each region of Fig. 1.15 can be described with increased clarity:

$$I_D = I_s e^{V_D/nV_T} - I_s$$

For positive values of V_D the first term of the above equation will grow very quickly and totally overpower the effect of the second term. The result is the following equation, which only has positive values and takes on the exponential format e^x appearing in Fig. 1.16:

$$I_D \cong I_s e^{V_D/nV_T} \qquad (V_D \text{ positive})$$

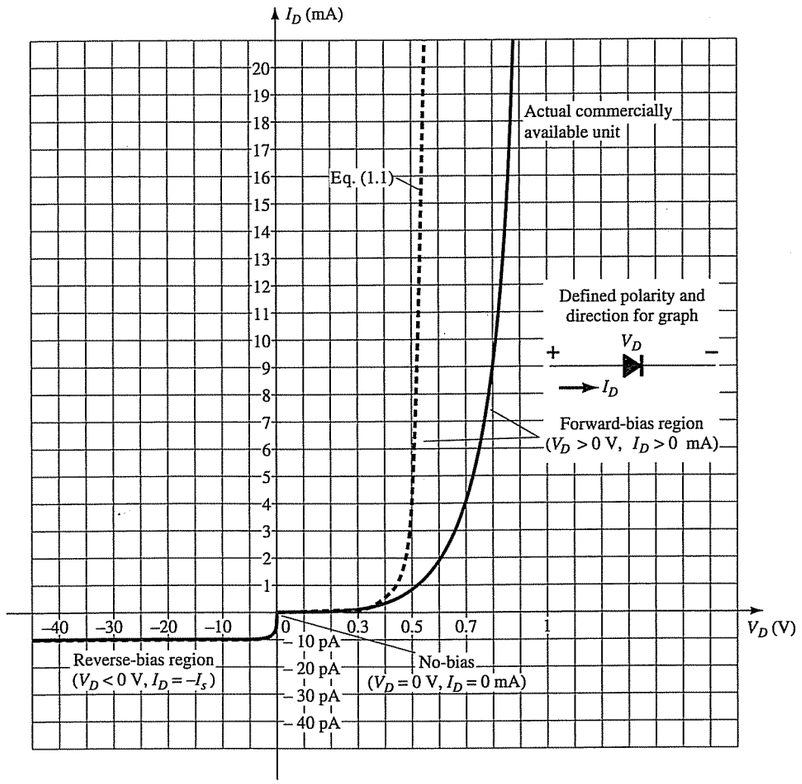


FIG. 1.15
Silicon semiconductor diode characteristics.

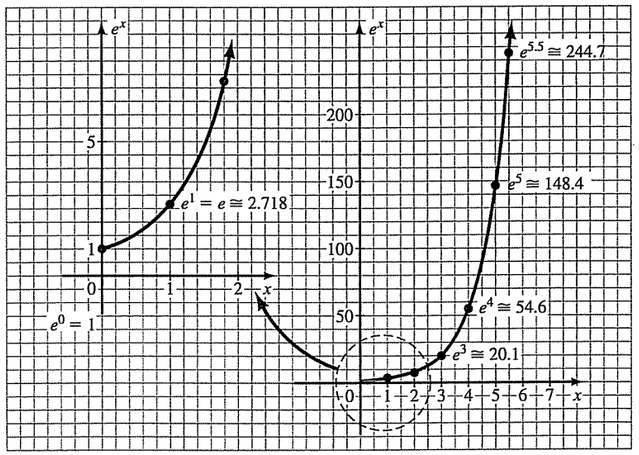


FIG. 1.16
Plot of e^x.

The exponential curve of Fig. 1.16 increases very rapidly with increasing values of x. At $x = 0$, $e^0 = 1$, whereas at $x = 5$, it jumps to greater than 148. If we continued to $x = 10$, the curve jumps to greater than 22,000. Clearly, therefore, as the value of x increases, the curve becomes almost vertical, an important conclusion to keep in mind when we examine the change in current with increasing values of applied voltage.

For negative values of V_D the exponential term drops very quickly below the level of I, and the resulting equation for I_D is simply

$$I_D \cong -I_s \qquad (V_D \text{ negative})$$

Note in Fig. 1.15 that for negative values of V_D the current is essentially horizontal at the level of $-I_s$.

At $V = 0$ V, Eq. (1.1) becomes

$$I_D = I_s(e^0 - 1) = I_s(1 - 1) = 0 \text{ mA}$$

as confirmed by Fig. 1.15.

The sharp change in direction of the curve at $V_D = 0$ V is simply due to the change in current scales from above the axis to below the axis. Note that above the axis the scale is in milliamperes (mA), whereas below the axis it is in picoamperes (pA).

Theoretically, with all things perfect, the characteristics of a silicon diode should appear as shown by the dashed line of Fig. 1.15. However, commercially available silicon diodes deviate from the ideal for a variety of reasons including the internal "body" resistance and the external "contact" resistance of a diode. Each contributes to an additional voltage at the same current level, as determined by Ohm's law, causing the shift to the right witnessed in Fig. 1.15.

The change in current scales between the upper and lower regions of the graph was noted earlier. For the voltage V_D there is also a measurable change in scale between the right-hand region of the graph and the left-hand region. For positive values of V_D the scale is in tenths of volts, and for the negative region it is in tens of volts.

It is important to note in Fig. 1.14b how:

The defined direction of conventional current for the positive voltage region matches the arrowhead in the diode symbol.

This will always be the case for a forward-biased diode. It may also help to note that the forward-bias condition is established when the bar representing the negative side of the applied voltage matches the side of the symbol with the vertical bar.

Going back a step further by looking at Fig. 1.14b, we find a forward-bias condition is established across a p–n junction when the positive side of the applied voltage is applied to the p-type material (noting the correspondence in the letter p) and the negative side of the applied voltage is applied to the n-type material (noting the same correspondence).

It is particularly interesting to note that the reverse saturation current of the commercial unit is significantly larger than that of I_s in Shockley's equation. This is due to effects not included in Shockley's equation, such as the generation of carriers in the depletion region and surface leakage currents, which are sensitive to the contact area at the junction. In other words:

The actual reverse saturation current of a commercially available diode will normally be measurably larger than that appearing as the reverse saturation current in Shockley's equation.

It is important to keep in mind, however, that even if the actual reverse saturation current is 1,000 times greater, if $I_s = 10$ pA, the reverse saturation current will simply increase to only 10 nA, which can still be ignored for most applications.

Another factor that has a strong effect on the magnitude of the reverse saturation current is the contact area at the junction:

There is a direct correspondence between the area at the junction and the level of reverse saturation current.

For example, if we assume that the contact area necessary to handle a high-current diode of 1 A is 1000 times that of a diode with a maximum rated forward current of 1 mA (with $I_s = 1$ nA), then, according to the above statement, the reverse saturation current of the 1-A diode will be 1000 times that of the 1-mA diode, or 1 μA (a level that could cause some concern for some applications).

We will find in the discussions to follow that the ideal situation is for I_s to be 0 A in the reverse-bias region. The fact that it is typically in the range of 0.01 pA to 10 pA today as compared to 0.1 μA to 1 μA a few decades ago is a credit to the manufacturing industry. Comparing the common value of 10 pA to the 1-μA level of years past shows an improvement factor of 100,000.

Zener Region

Even though the scale of Fig. 1.15 is in tens of volts in the negative region, there is a point where the application of too negative a voltage will result in a sharp change in the characteristics, as shown in Fig. 1.17. The current increases at a very rapid rate in a direction opposite to that of the positive voltage region. The reverse-bias potential that results in this dramatic change in characteristics is called the *Zener potential* and is given the symbol V_Z.

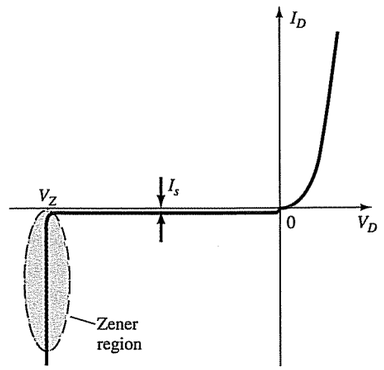


FIG. 1.17
Zener region.

As the voltage across the diode increases in the reverse-bias region, the velocity of the minority carriers responsible for the reverse saturation current I_s will also increase. Eventually, their velocity and associated kinetic energy ($W_K = \frac{1}{2}mv^2$) will be sufficient to release additional carriers through collisions with otherwise stable atomic structures. That is, an *ionization* process will result whereby valence electrons absorb sufficient energy to leave the parent atom. These additional carriers can then aid the ionization process to the point where a high *avalanche* current is established and the *avalanche breakdown* region determined.

The avalanche region (V_Z) can be brought closer to the vertical axis by increasing the doping levels in the *p*- and *n*-type materials. However, as V_Z decreases to very low levels, such as -5 V, another mechanism, called *Zener breakdown*, will contribute to the sharp change in the characteristic. It occurs because there is a strong electric field in the region of the junction that can disrupt the bonding forces within the atom and "generate" carriers. Although the Zener breakdown mechanism is a significant contributor only at lower levels of V_Z, this sharp change in the characteristic at any level is called the *Zener region*, and diodes employing this unique portion of the characteristic of a *p–n* junction are called *Zener diodes*. They are described in detail in Section 1.15.

The Zener region of the semiconductor diode described must be avoided if the response of a system is not to be completely altered by the sharp change in characteristics in this reverse-voltage region.

The maximum reverse-bias potential that can be applied before entering the Zener region is called the peak inverse voltage (referred to simply as the PIV rating) or the peak reverse voltage (denoted the PRV rating).

If an application requires a PIV rating greater than that of a single unit, a number of diodes of the same characteristics can be connected in series. Diodes are also connected in parallel to increase the current-carrying capacity.

It will be shown in Section 1.12 when we review the specification sheets provided with commercially available diodes that:

At a fixed temperature, the reverse saturation current of a diode increases with an increase in the applied reverse bias.

For instance, the diode described in Section 1.12 has a reverse saturation current of 1 nA at 20 V at room temperature but a reverse saturation current of 5 nA at 100 V at the same temperature.

Ge, Si, and GaAs

The discussion thus far has solely used Si as the base semiconductor material. It is now important to compare it to the other two materials of primary importance: GaAs and Ge. A plot comparing the characteristics of commercially available Si, GaAs, and Ge diodes is provided in Fig. 1.18. It is immediately obvious that the point of vertical rise in the characteristics is different for each material, although the general shape of each characteristic is quite similar. Germanium is closest to the vertical axis and GaAs is the most distant. As noted on the curves, the center of the knee of the curve is about 0.3 V for Ge, 0.7 V for Si, and 1.2 V for GaAs (see Table 1.3).

TABLE 1.3
Knee Voltages V_K

Semiconductor	V_K(V)
Ge	0.3
Si	0.7
GaAs	1.2

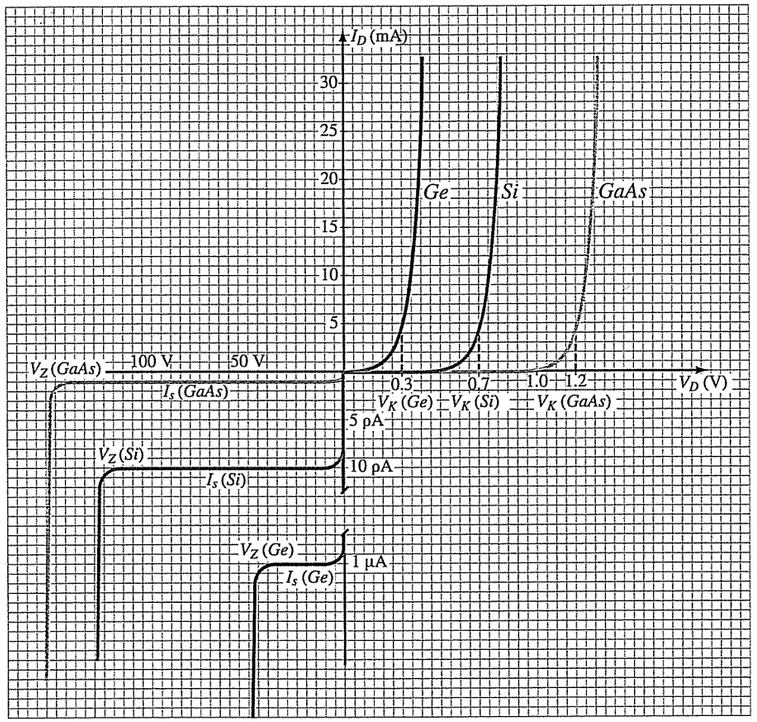


FIG. 1.18
Comparison of Ge, Si, and GaAs diodes.

The shape of the curve in the reverse-bias region is also quite similar for each material, but notice the measurable difference in the magnitudes of the typical reverse saturation currents. For GaAs, the reverse saturation current is typically about 1 pA, compared to 10 pA for Si and 1 μA for Ge, a significant difference in levels.

Also note the relative magnitudes of the reverse breakdown voltages for each material. GaAs typically has maximum breakdown levels that exceed those of Si devices of the same power level by about 10%, with both having breakdown voltages that typically extend between 50 V and 1 kV. There are Si power diodes with breakdown voltages as high as 20 kV. Germanium typically has breakdown voltages of less than 100 V, with maximums around 400 V. The curves of Fig. 1.18 are simply designed to reflect relative breakdown voltages for the three materials. When one considers the levels of reverse

saturation currents and breakdown voltages, Ge certainly sticks out as having the least desirable characteristics.

Temperature Effects

Temperature can have a marked effect on the characteristics of a semiconductor diode, as demonstrated by the characteristics of a silicon diode shown in Fig. 1.19:

In the forward-bias region the characteristics of a silicon diode shift to the left at a rate of 2.5 mV per centigrade degree increase in temperature.

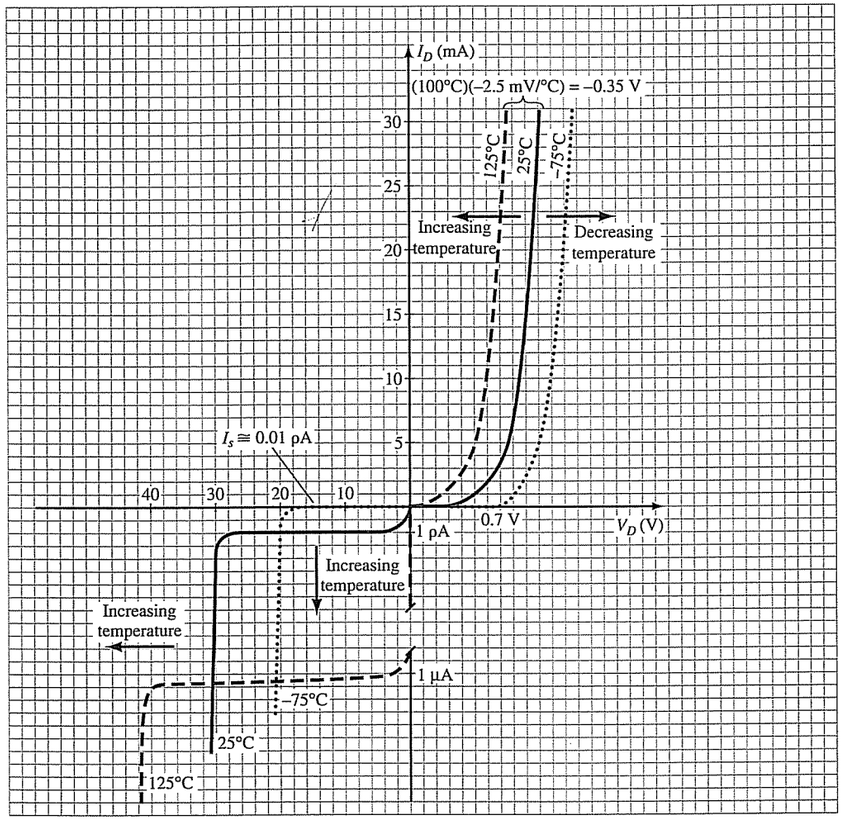


FIG. 1.19
Variation in Si diode characteristics with temperature change.

A increase from room temperature (20°C) to 100°C (the boiling point of water) results in a drop of 80(2.5 mV) = 200 mV, or 0.2 V, which is significant on a graph scaled in tenths of volts. A decrease in temperature has the reverse effect, as also shown in the figure:

In the reverse-bias region the reverse saturation current of a silicon diode doubles for every 10°C rise in temperature.

For a change from 20°C to 100°C, the level of I_s increases from 10 nA to a value of 2.56 μA, which is a significant, 256-fold increase. Continuing to 200°C would result in a monstrous reverse saturation current of 2.62 mA. For high-temperature applications one would therefore look for Si diodes with room-temperature I_s closer to 10 pA, a level commonly available today, which would limit the current to 2.62 μA. It is indeed fortunate that both Si and GaAs have relatively small reverse saturation currents at room temperature. GaAs devices are available that work very well in the −200°C to +200°C temperature range, with some having maximum temperatures approaching 400°C. Consider, for a moment, how huge the reverse saturation current would be if we started with a Ge diode with a saturation current of 1 μA and applied the same doubling factor.

Finally, it is important to note from Fig. 1.19 that:

The reverse breakdown voltage of a semiconductor diode will increase or decrease with temperature depending on the Zener potential.

Although Fig. 1.19 reveals that the breakdown voltage will increase with temperature, if the initial breakdown voltage is less than 5 V, the breakdown voltage may actually decrease with temperature. The sensitivity of the Zener potential to changes of temperature will be examined in more detail in Section 1.15.

Summary

A great deal has been introduced in the foregoing paragraphs about the construction of a semiconductor diode and the materials employed. The characteristics have now been presented and the important differences between the response of the materials discussed. It is now time to compare the *p–n* junction response to the desired response and reveal the primary functions of a semiconductor diode.

Table 1.4 provides a synopsis of material regarding the three most frequently used semiconductor materials. Figure 1.20 includes a short biography of the first research scientist to discover the *p–n* junction in a semiconductor material.

TABLE 1.4
The Current Commercial Use of Ge, Si, and GaAs

Ge:	Germanium is in limited production due to its temperature sensitivity and high reverse saturation current. It is still commercially available but is limited to some high-speed applications (due to a relatively high mobility factor) and applications that use its sensitivity to light and heat such as photodetectors and security systems.
Si:	Without question the semiconductor used most frequently for the full range of electronic devices. It has the advantage of being readily available at low cost and has relatively low reverse saturation currents, good temperature characteristics, and excellent breakdown voltage levels. It also benefits from decades of enormous attention to the design of large-scale integrated circuits and processing technology.
GaAs:	Since the early 1990s the interest in GaAs has grown in leaps and bounds, and it will eventually take a good share of the development from silicon devices, especially in very large scale integrated circuits. Its high-speed characteristics are in more demand every day, with the added features of low reverse saturation currents, excellent temperature sensitivities, and high breakdown voltages. More than 80% of its applications are in optoelectronics with the development of light-emitting diodes, solar cells, and other photodetector devices, but that will probably change dramatically as its manufacturing costs drop and its use in integrated circuit design continues to grow; perhaps the semiconductor material of the future.



Russell Ohl (1898–1987)

American (Allentown, PA; Holmdel, NJ; Vista, CA)
Army Signal Corps, University of Colorado, Westinghouse, AT&T, Bell Labs Fellow, Institute of Radio Engineers—1955
(Courtesy Pennsylvania State University Archives, Pennsylvania State University Libraries.)

Although vacuum tubes were used in all forms of communication in the 1930s, Russell Ohl was determined to demonstrate that the future of the field was defined by semiconductor crystals. Germanium was not immediately available for his research, so he turned to silicon, and found a way to raise its level of purity to 99.8%, for which he received a patent. The actual discovery of the *p–n* junction, as often happens in scientific research, was the result of a set of circumstances that were not planned. On February 23, 1940, Ohl found that a silicon crystal with a crack down the middle would produce a significant rise in current when placed near a source of light. This discovery led to further research, which revealed that the purity levels on each side of the crack were different and that a barrier was formed at the junction that allowed the passage of current in only one direction—the first solid-state diode had been identified and explained. In addition, this sensitivity to light was the beginning of the development of solar cells. The results were quite instrumental in the development of the transistor in 1945 by three individuals also working at Bell Labs.

FIG. 1.20

1.7 IDEAL VERSUS PRACTICAL

In the previous section we found that a *p–n* junction will permit a generous flow of charge when forward-biased and a very small level of current when reverse-biased. Both conditions are reviewed in Fig. 1.21, with the heavy current vector in Fig. 1.21a matching the direction of the arrow in the diode symbol and the significantly smaller vector in the opposite direction in Fig. 1.21b representing the reverse saturation current.

An analogy often used to describe the behavior of a semiconductor diode is a mechanical switch. In Fig. 1.21a the diode is acting like a closed switch permitting a generous flow of charge in the direction indicated. In Fig. 1.21b the level of current is so small in most cases that it can be approximated as 0 A and represented by an open switch.

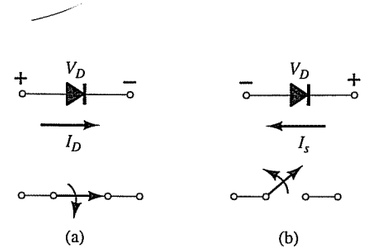


FIG. 1.21
Ideal semiconductor diode: (a) forward-biased; (b) reverse-biased.


Multisim

In other words:

The semiconductor diode behaves in a manner similar to a mechanical switch in that it can control whether current will flow between it's two terminals.

However, it is important to also be aware that:

The semiconductor diode is different from a mechanical switch in the sense that when the switch is closed it will only permit current to flow in one direction.

Ideally, if the semiconductor diode is to behave like a closed switch in the forward-bias region, the resistance of the diode should be 0 Ω. In the reverse-bias region its resistance should be ∞ Ω to represent the open-circuit equivalent. Such levels of resistance in the forward- and reverse-bias regions result in the characteristics of Fig. 1.22.

The characteristics have been superimposed to compare the ideal Si diode to a real-world Si diode. First impressions might suggest that the commercial unit is a poor impression of the ideal switch. However, when one considers that the only major difference is that the commercial diode rises at a level of 0.7 V rather than 0 V, there are a number of similarities between the two plots.

When a switch is closed the resistance between the contacts is assumed to be 0 Ω. At the plot point chosen on the vertical axis the diode current is 5 mA and the voltage across the diode is 0 V. Substituting into Ohm's law results in

$$R_F = \frac{V_D}{I_D} = \frac{0\text{ V}}{5\text{ mA}} = \mathbf{0\ \Omega} \qquad \text{(short-circuit equivalent)}$$

In fact:

At any current level on the vertical line, the voltage across the ideal diode is 0 V and the resistance is 0 Ω.

For the horizontal section, if we again apply Ohm's law, we find

$$R_R = \frac{V_D}{I_D} = \frac{20\text{ V}}{0\text{ mA}} \cong \infty\ \Omega \qquad \text{(open-circuit equivalent)}$$

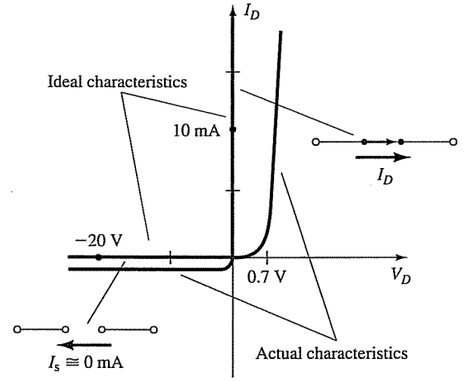


FIG. 1.22
Ideal versus actual semiconductor characteristics.

Again:

Because the current is 0 mA anywhere on the horizontal line, the resistance is ∞ Ω at any point on the axis.

Due to the shape and the location of the curve for the commercial unit in the forward-bias region there will be a resistance associated with the diode that is greater than 0 Ω. However, if that resistance is small enough compared to other resistors of the network in series with the diode, it is often a good approximation to simply assume the resistance of the commercial unit is 0 Ω. In the reverse-bias region, if we assume the reverse saturation current is so small it can be approximated as 0 mA, we have the same open-circuit equivalence provided by the open switch.

The result, therefore, is that there are sufficient similarities between the ideal switch and the semiconductor diode to make it an effective electronic device. In the next section the various resistance levels of importance are determined for use in the next chapter, where the response of diodes in an actual network is examined.

1.8 RESISTANCE LEVELS

As the operating point of a diode moves from one region to another the resistance of the diode will also change due to the nonlinear shape of the characteristic curve. It will be demonstrated in the next few paragraphs that the type of applied voltage or signal will define the resistance level of interest. Three different levels will be introduced in this section, which will appear again as we examine other devices. It is therefore paramount that their determination be clearly understood.

DC or Static Resistance

The application of a dc voltage to a circuit containing a semiconductor diode will result in an operating point on the characteristic curve that will not change with time. The resistance of the diode at the operating point can be found simply by finding the corresponding levels of V_D and I_D as shown in Fig. 1.23 and applying the following equation:

$$\boxed{R_D = \frac{V_D}{I_D}} \qquad \textbf{(1.3)}$$

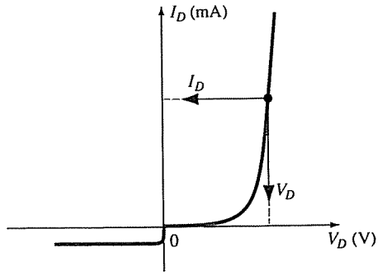


FIG. 1.23
Determining the dc resistance of a diode at a particular operating point.

The dc resistance levels at the knee and below will be greater than the resistance levels obtained for the vertical rise section of the characteristics. The resistance levels in the reverse-bias region will naturally be quite high. Since ohmmeters typically employ a relatively constant-current source, the resistance determined will be at a preset current level (typically, a few milliamperes).

In general, therefore, the higher the current through a diode, the lower is the dc resistance level.

EXAMPLE 1.2 Determine the dc resistance levels for the diode of Fig. 1.24 at

a. $I_D = 2$ mA (low level)
b. $I_D = 20$ mA (high level)
c. $V_D = -10$ V (reverse-biased)

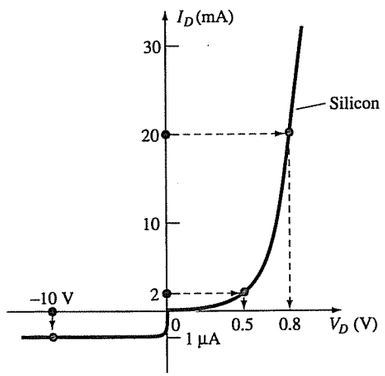


FIG. 1.24
Example 1.2.

Solution:

a. At $I_D = 2$ mA, $V_D = 0.5$ V (from the curve) and

$$R_D = \frac{V_D}{I_D} = \frac{0.5\text{ V}}{2\text{ mA}} = \mathbf{250\ \Omega}$$

b. At $I_D = 20$ mA, $V_D = 0.8$ V (from the curve) and

$$R_D = \frac{V_D}{I_D} = \frac{0.8\text{ V}}{20\text{ mA}} = \mathbf{40\ \Omega}$$

c. At $V_D = -10$ V, $I_D = -I_s = -1\ \mu$A (from the curve) and

$$R_D = \frac{V_D}{I_D} = \frac{10\text{ V}}{1\ \mu\text{A}} = \mathbf{10\ M\Omega}$$

clearly supporting some of the earlier comments regarding the dc resistance levels of a diode.

AC or Dynamic Resistance

It is obvious from Eq. (1.3) and Example 1.2 that the dc resistance of a diode is independent of the shape of the characteristic in the region surrounding the point of interest. If a sinusoidal rather than a dc input is applied, the situation will change completely. The varying input will move the instantaneous operating point up and down a region of the characteristics and thus defines a specific change in current and voltage as shown in Fig. 1.25. With no applied varying signal, the point of operation would be the *Q*-point appearing on Fig. 1.25, determined by the applied dc levels. The designation *Q-point* is derived from the word *quiescent*, which means "still or unvarying."

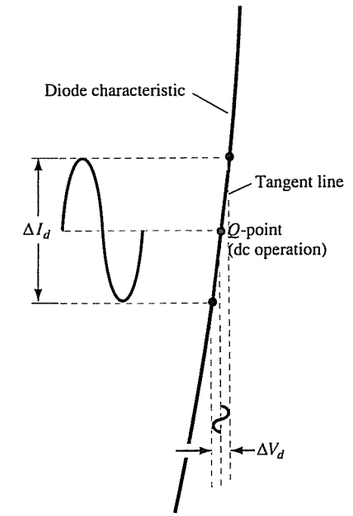


FIG. 1.25
Defining the dynamic or ac resistance.

A straight line drawn tangent to the curve through the *Q*-point as shown in Fig. 1.26 will define a particular change in voltage and current that can be used to determine the *ac* or *dynamic* resistance for this region of the diode characteristics. An effort should be made to keep the change in voltage and current as small as possible and equidistant to either side of the *Q*-point. In equation form,

$$r_d = \frac{\Delta V_d}{\Delta I_d} \tag{1.4}$$

where Δ signifies a finite change in the quantity.

The steeper the slope, the lower is the value of ΔV_d for the same change in ΔI_d and the lower is the resistance. The ac resistance in the vertical-rise region of the characteristic is therefore quite small, whereas the ac resistance is much higher at low current levels.

In general, therefore, the lower the Q-point of operation (smaller current or lower voltage), the higher is the ac resistance.

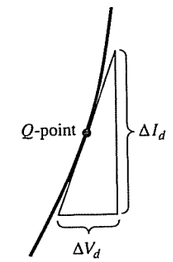


FIG. 1.26
Determining the ac resistance at a Q-point.

EXAMPLE 1.3 For the characteristics of Fig. 1.27:

a. Determine the ac resistance at $I_D = 2$ mA.
b. Determine the ac resistance at $I_D = 25$ mA.
c. Compare the results of parts (a) and (b) to the dc resistances at each current level.

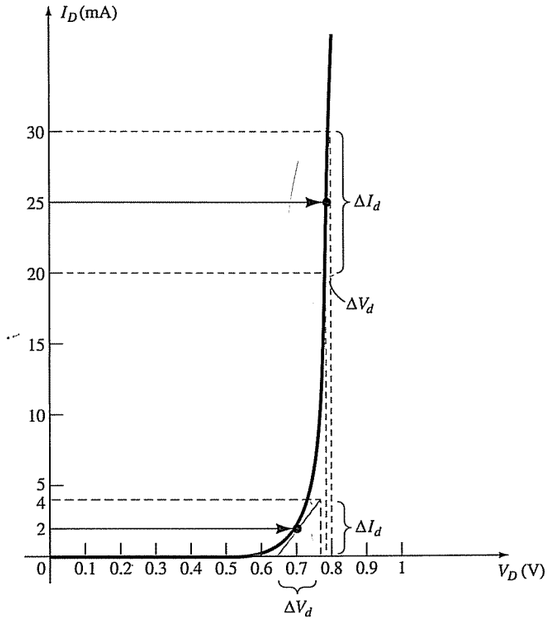


FIG. 1.27
Example 1.3.

Solution:

a. For $I_D = 2$ mA, the tangent line at $I_D = 2$ mA was drawn as shown in Fig. 1.27 and a swing of 2 mA above and below the specified diode current was chosen. At $I_D = 4$ mA, $V_D = 0.76$ V, and at $I_D = 0$ mA, $V_D = 0.65$ V. The resulting changes in current and voltage are, respectively,

$$\Delta I_d = 4\,\text{mA} - 0\,\text{mA} = 4\,\text{mA}$$

and

$$\Delta V_d = 0.76\,\text{V} - 0.65\,\text{V} = 0.11\,\text{V}$$

and the ac resistance is

$$r_d = \frac{\Delta V_d}{\Delta I_d} = \frac{0.11\,\text{V}}{4\,\text{mA}} = \mathbf{27.5\ \Omega}$$

b. For $I_D = 25$ mA, the tangent line at $I_D = 25$ mA was drawn as shown in Fig. 1.27 and a swing of 5 mA above and below the specified diode current was chosen. At $I_D = 30$ mA, $V_D = 0.8$ V, and at $I_D = 20$ mA, $V_D = 0.78$ V. The resulting changes in current and voltage are, respectively,

$$\Delta I_d = 30\,\text{mA} - 20\,\text{mA} = 10\,\text{mA}$$

and

$$\Delta V_d = 0.8\,\text{V} - 0.78\,\text{V} = 0.02\,\text{V}$$

and the ac resistance is

$$r_d = \frac{\Delta V_d}{\Delta I_d} = \frac{0.02\,\text{V}}{10\,\text{mA}} = \mathbf{2\ \Omega}$$

c. For $I_D = 2$ mA, $V_D = 0.7$ V and

$$R_D = \frac{V_D}{I_D} = \frac{0.7\,\text{V}}{2\,\text{mA}} = \mathbf{350\ \Omega}$$

which far exceeds the r_d of 27.5 Ω.

For $I_D = 25$ mA, $V_D = 0.79$ V and

$$R_D = \frac{V_D}{I_D} = \frac{0.79\,\text{V}}{25\,\text{mA}} = \mathbf{31.62\ \Omega}$$

which far exceeds the r_d of 2 Ω.

We have found the dynamic resistance graphically, but there is a basic definition in differential calculus that states:

The derivative of a function at a point is equal to the slope of the tangent line drawn at that point.

Equation (1.4), as defined by Fig. 1.26, is, therefore, essentially finding the derivative of the function at the *Q*-point of operation. If we find the derivative of the general equation (1.1) for the semiconductor diode with respect to the applied forward bias and then invert the result, we will have an equation for the dynamic or ac resistance in that region. That is, taking the derivative of Eq. (1.1) with respect to the applied bias will result in

$$\frac{d}{dV_D}(I_D) = \frac{d}{dV_D}\left[I_s\left(e^{V_D/nV_T} - 1\right)\right]$$

and

$$\frac{dI_D}{dV_D} = \frac{1}{nV_T}(I_D + I_s)$$

after we apply a few basic maneuvers of differential calculus. In general, $I_D \gg I_s$ in the vertical-slope section of the characteristics and

$$\frac{dI_D}{dV_D} \cong \frac{I_D}{nV_T}$$

Flipping the result to define a resistance ratio ($R = V/I$) gives

$$\frac{dV_D}{dI_D} = r_d = \frac{nV_T}{I_D}$$

Substituting $n = 1$ and $V_T \cong 26$ mV from Example 1.1 results in

$$\boxed{r_d = \frac{26\,\text{mV}}{I_D}} \qquad \textbf{(1.5)}$$

The significance of Eq. (1.5) must be clearly understood. It implies that *the dynamic resistance can be found simply by substituting the quiescent value of the diode current into the equation.* There is no need to have the characteristics available or to worry about sketching tangent lines as defined by Eq. (1.4). It is important to keep in mind, however, that Eq. (1.5) is accurate only for values of I_D in the vertical-rise section of the curve. For lesser values of I_D, $n = 2$ (silicon) and the value of r_d obtained must be multiplied by a factor of 2. For small values of I_D below the knee of the curve, Eq. (1.5) becomes inappropriate.

All the resistance levels determined thus far have been defined by the *p–n* junction and do not include the resistance of the semiconductor material itself (called *body* resistance) and the resistance introduced by the connection between the semiconductor material and the external metallic conductor (called *contact* resistance). These additional resistance levels can be included in Eq. (1.5) by adding a resistance denoted r_B:

$$\boxed{r'_d = \frac{26\,\text{mV}}{I_D} + r_B} \quad \text{ohms} \qquad \textbf{(1.6)}$$

The resistance r'_d, therefore, includes the dynamic resistance defined by Eq. (1.5) and the resistance r_B just introduced. The factor r_B can range from typically 0.1 Ω for high-power devices to 2 Ω for some low-power, general-purpose diodes. For Example 1.3 the ac resistance at 25 mA was calculated to be 2 Ω. Using Eq. (1.5), we have

$$r_d = \frac{26\,\text{mV}}{I_D} = \frac{26\,\text{mV}}{25\,\text{mA}} = \mathbf{1.04\ \Omega}$$

The difference of about 1 Ω could be treated as the contribution of r_B.

For Example 1.3 the ac resistance at 2 mA was calculated to be 27.5 Ω. Using Eq. (1.5) but multiplying by a factor of 2 for this region (in the knee of the curve $n = 2$),

$$r_d = 2\left(\frac{26\text{ mV}}{I_D}\right) = 2\left(\frac{26\text{ mV}}{2\text{ mA}}\right) = 2(13\ \Omega) = \mathbf{26\ \Omega}$$

The difference of 1.5 Ω could be treated as the contribution due to r_B.

In reality, determining r_d to a high degree of accuracy from a characteristic curve using Eq. (1.4) is a difficult process at best and the results have to be treated with a grain of salt. At low levels of diode current the factor r_B is normally small enough compared to r_d to permit ignoring its impact on the ac diode resistance. At high levels of current the level of r_B may approach that of r_d, but since there will frequently be other resistive elements of a much larger magnitude in series with the diode, we will assume in this book that the ac resistance is determined solely by r_d, and the impact of r_B will be ignored unless otherwise noted. Technological improvements of recent years suggest that the level of r_B will continue to decrease in magnitude and eventually become a factor that can certainly be ignored in comparison to r_d.

The discussion above centered solely on the forward-bias region. In the reverse-bias region we will assume that the change in current along the I_s line is nil from 0 V to the Zener region and the resulting ac resistance using Eq. (1.4) is sufficiently high to permit the open-circuit approximation.

Average AC Resistance

If the input signal is sufficiently large to produce a broad swing such as indicated in Fig. 1.28, the resistance associated with the device for this region is called the *average ac resistance.* The average ac resistance is, by definition, the resistance determined by a straight line drawn between the two intersections established by the maximum and minimum values of input voltage. In equation form (note Fig. 1.28),

$$\boxed{r_{av} = \left.\frac{\Delta V_d}{\Delta I_d}\right|_{\text{pt. to pt.}}} \tag{1.7}$$

For the situation indicated by Fig. 1.28,

$$\Delta I_d = 17\text{ mA} - 2\text{ mA} = 15\text{ mA}$$

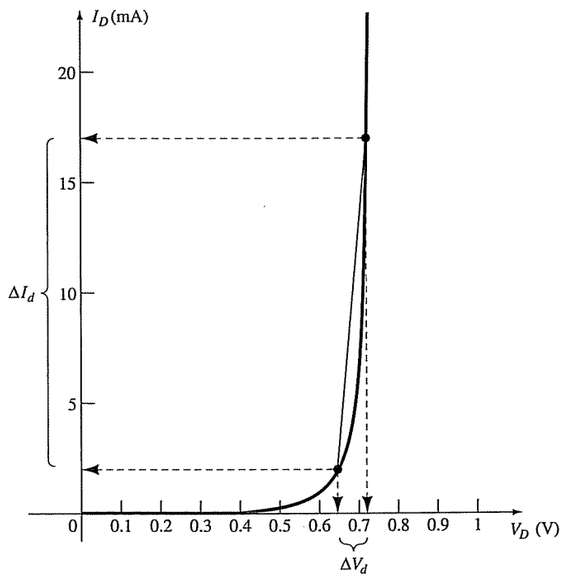


FIG. 1.28
Determining the average ac resistance between indicated limits.

and

$$\Delta V_d = 0.725\text{ V} - 0.65\text{ V} = 0.075\text{ V}$$

with

$$r_{av} = \frac{\Delta V_d}{\Delta I_d} = \frac{0.075\text{ V}}{15\text{ mA}} = \mathbf{5\ \Omega}$$

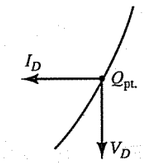
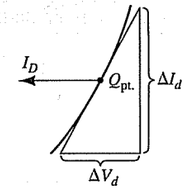
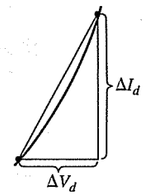
If the ac resistance (r_d) were determined at $I_D = 2$ mA, its value would be more than 5 Ω, and if determined at 17 mA, it would be less. In between, the ac resistance would make the transition from the high value at 2 mA to the lower value at 17 mA. Equation (1.7) defines a value that is considered the average of the ac values from 2 mA to 17 mA. The fact that one resistance level can be used for such a wide range of the characteristics will prove quite useful in the definition of equivalent circuits for a diode in a later section.

As with the dc and ac resistance levels, the lower the level of currents used to determine the average resistance, the higher is the resistance level.

Summary Table

Table 1.5 was developed to reinforce the important conclusions of the last few pages and to emphasize the differences among the various resistance levels. As indicated earlier, the content of this section is the foundation for a number of resistance calculations to be performed in later sections and chapters.

TABLE 1.5
Resistance Levels

Type	Equation	Special Characteristics	Graphical Determination
DC or static	$R_D = \frac{V_D}{I_D}$	Defined as a point on the characteristics	
AC or dynamic	$r_d = \frac{\Delta V_d}{\Delta I_d} = \frac{26\text{ mV}}{I_D}$	Defined by a tangent line at the Q-point	
Average ac	$r_{av} = \left.\frac{\Delta V_d}{\Delta I_d}\right\|_{\text{pt. to pt.}}$	Defined by a straight line between limits of operation	

1.9 DIODE EQUIVALENT CIRCUITS

An equivalent circuit is a combination of elements properly chosen to best represent the actual terminal characteristics of a device or system in a particular operating region.

In other words, once the equivalent circuit is defined, the device symbol can be removed from a schematic and the equivalent circuit inserted in its place without severely affecting the actual behavior of the system. The result is often a network that can be solved using traditional circuit analysis techniques.

Piecewise-Linear Equivalent Circuit

One technique for obtaining an equivalent circuit for a diode is to approximate the characteristics of the device by straight-line segments, as shown in Fig. 1.29. The resulting equivalent circuit is called a *piecewise-linear equivalent circuit.* It should be obvious from Fig. 1.29 that the straight-line segments do not result in an exact duplication of the actual characteristics, especially in the knee region. However, the resulting segments are sufficiently close to the actual curve to establish an equivalent circuit that will provide an excellent first approximation to the actual behavior of the device. For the sloping section of the equivalence the average ac resistance as introduced in Section 1.8 is the resistance level appearing in the equivalent circuit of Fig. 1.28 next to the actual device. In essence, it defines the resistance level of the device when it is in the "on" state. The ideal diode is included to establish that there is only one direction of conduction through the device, and a reverse-bias condition will result in the open-circuit state for the device. Since a silicon semiconductor diode does not reach the conduction state until V_D reaches 0.7 V with a forward bias (as shown in Fig. 1.29), a battery V_K opposing the conduction direction must appear in the equivalent circuit as shown in Fig. 1.30. The battery simply specifies that the voltage across the device must be greater than the threshold battery voltage before conduction through the device in the direction dictated by the ideal diode can be established. When conduction is established the resistance of the diode will be the specified value of r_{av}.

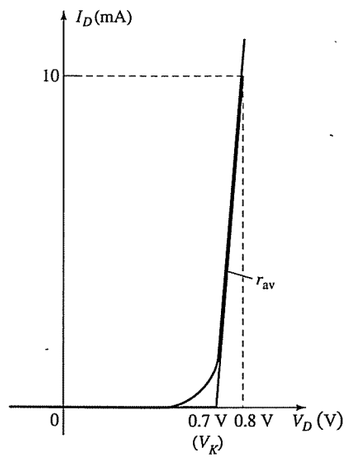


FIG. 1.29
Defining the piecewise-linear equivalent circuit using straight-line segments to approximate the characteristic curve.

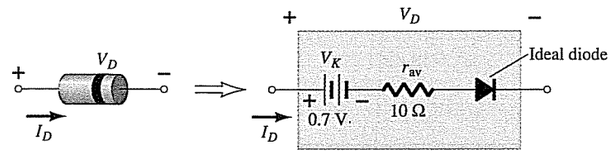


FIG. 1.30
Components of the piecewise-linear equivalent circuit.

Keep in mind, however, that V_K in the equivalent circuit is not an independent voltage source. If a voltmeter is placed across an isolated diode on the top of a lab bench, a reading of 0.7 V will not be obtained. The battery simply represents the horizontal offset of the characteristics that must be exceeded to establish conduction.

The approximate level of r_{av} can usually be determined from a specified operating point on the specification sheet (to be discussed in Section 1.10). For instance, for a silicon semiconductor diode, if $I_F = 10$ mA (a forward conduction current for the diode) at

$V_D = 0.8$ V, we know that for silicon a shift of 0.7 V is required before the characteristics rise, and we obtain

$$r_{av} = \left.\frac{\Delta V_d}{\Delta I_d}\right|_{\text{pt. to pt.}} = \frac{0.8\text{ V} - 0.7\text{ V}}{10\text{ mA} - 0\text{ mA}} = \frac{0.1\text{ V}}{10\text{ mA}} = \mathbf{10\ \Omega}$$

as obtained for Fig. 1.29.

Simplified Equivalent Circuit

For most applications, the resistance r_{av} is sufficiently small to be ignored in comparison to the other elements of the network. Removing r_{av} from the equivalent circuit is the same as implying that the characteristics of the diode appear as shown in Fig. 1.31. Indeed, this approximation is frequently employed in semiconductor circuit analysis as demonstrated in Chapter 2. The reduced equivalent circuit appears in the same figure. It states that a forward-biased silicon diode in an electronic system under dc conditions has a drop of 0.7 V across it in the conduction state at any level of diode current (within rated values, of course).

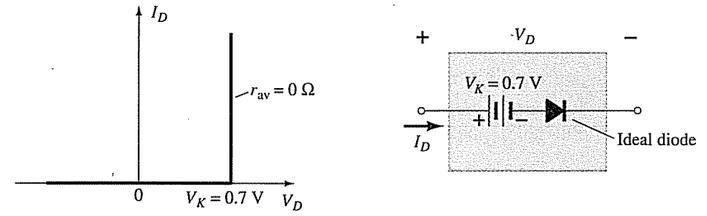


FIG. 1.31
Simplified equivalent circuit for the silicon semiconductor diode.

Ideal Equivalent Circuit

Now that r_{av} has been removed from the equivalent circuit, let us take the analysis a step further and establish that a 0.7-V level can often be ignored in comparison to the applied voltage level. In this case the equivalent circuit will be reduced to that of an ideal diode as shown in Fig. 1.32 with its characteristics. In Chapter 2 we will see that this approximation is often made without a serious loss in accuracy.

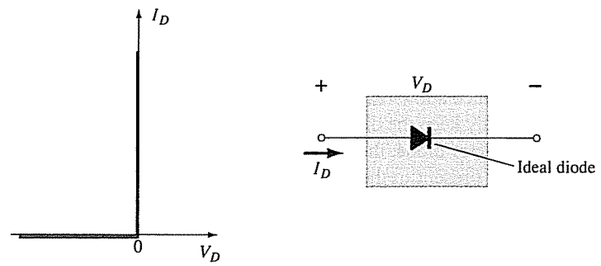


FIG. 1.32
Ideal diode and its characteristics.

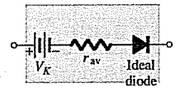
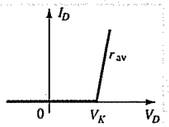
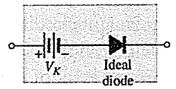
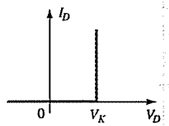
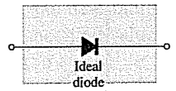
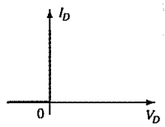
In industry a popular substitution for the phrase "diode equivalent circuit" is diode *model*—a model by definition being a representation of an existing device, object, system, and so on. In fact, this substitute terminology will be used almost exclusively in the chapters to follow.

Summary Table

For clarity, the diode models employed for the range of circuit parameters and applications are provided in Table 1.6 with their piecewise-linear characteristics. Each will be investigated in greater detail in Chapter 2. There are always exceptions to the general rule, but it is fairly safe to say that the simplified equivalent model will be employed most frequently

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TABLE 1.6
Diode Equivalent Circuits (Models)

Type	Conditions	Model	Characteristics
Piecewise-linear model			
Simplified model	$R_{network} \gg r_{av}$		
Ideal device	$R_{network} \gg r_{av}$ $E_{network} \gg V_K$		

in the analysis of electronic systems, whereas the ideal diode is frequently applied in the analysis of power supply systems where larger voltages are encountered.

1.10 TRANSITION AND DIFFUSION CAPACITANCE

It is important to realize that:

Every electronic or electrical device is frequency sensitive.

That is, the terminal characteristics of any device will change with frequency. Even the resistance of a basic resistor, as of any construction, will be sensitive to the applied frequency. At low to mid-frequencies most resistors can be considered fixed in value. However, as we approach high frequencies, stray capacitive and inductive effects start to play a role and will affect the total impedance level of the element.

For the diode it is the stray capacitance levels that have the greatest effect. At low frequencies and relatively small levels of capacitance the reactance of a capacitor, determined by $X_C = 1/2\pi fC$, is usually so high it can be considered infinite in magnitude, represented by an open circuit, and ignored. At high frequencies, however, the level of X_C can drop to the point where it will introduce a low-reactance "shorting" path. If this shorting path is across the diode, it can essentially keep the diode from affecting the response of the network.

In the p–n semiconductor diode, there are two capacitive effects to be considered. Both types of capacitance are present in the forward- and reverse-bias regions, but one so outweighs the other in each region that we consider the effects of only one in each region.

In the reverse-bias region we have the transition- or depletion-region capacitance (C_T), whereas in the forward-bias region we have the diffusion (C_D) or storage capacitance.

Recall that the basic equation for the capacitance of a parallel-plate capacitor is defined by $C = \epsilon A/d$, where ϵ is the permittivity of the dielectric (insulator) between the plates of area A separated by a distance d. In the reverse-bias region there is a depletion region (free of carriers) that behaves essentially like an insulator between the layers of opposite charge. Since the depletion width (d) will increase with increased reverse-bias potential, the resulting transition capacitance will decrease, as shown in Fig. 1.33. The fact that the capacitance is dependent on the applied reverse-bias potential has application in a number of electronic systems. In fact, in Chapter 16 a diode will be introduced whose operation is wholly dependent on this phenomenon.

Although the effect described above will also be present in the forward-bias region, it is overshadowed by a capacitance effect directly dependent on the rate at which charge is injected into the regions just outside the depletion region. The result is that increased levels of

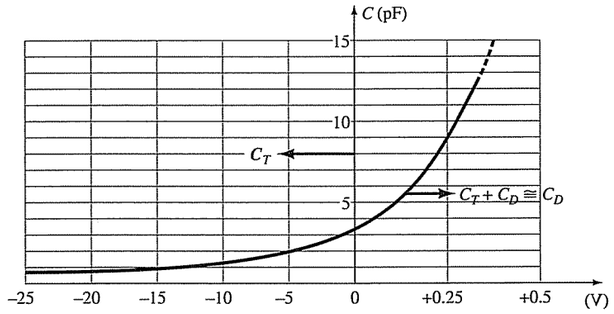


FIG. 1.33
Transition and diffusion capacitance versus applied bias for a silicon diode.

current will result in increased levels of diffusion capacitance. However, increased levels of current result in a reduced level of associated resistance (to be demonstrated shortly), and the resulting time constant ($\tau = RC$), which is very important in high-speed applications, does not become excessive.

The capacitive effects described above are represented by capacitors in parallel with the ideal diode, as shown in Fig. 1.34. For low- or mid-frequency applications (except in the power area), however, the capacitor is normally not included in the diode symbol.

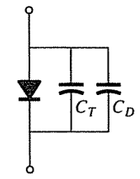


FIG. 1.34
Including the effect of the transition or diffusion capacitance on the semiconductor diode.

1.11 REVERSE RECOVERY TIME

There are certain pieces of data that are normally provided on diode specification sheets provided by manufacturers. One such quantity that has not been considered yet is the reverse recovery time, denoted by t_{rr}. In the forward-bias state it was shown earlier that there are a large number of electrons from the n-type material progressing through the p-type material and a large number of holes in the n-type material—a requirement for conduction. The electrons in the p-type material and holes progressing through the n-type material establish a large number of minority carriers in each material. If the applied voltage should be reversed to establish a reverse-bias situation, we would ideally like to see the diode change instantaneously from the conduction state to the nonconduction state. However, because of the large number of minority carriers in each material, the diode current will simply reverse as shown in Fig. 1.35 and stay at this measurable level for the period of time t_s (storage time) required for the minority carriers to return to their majority-carrier state in the opposite material. In essence, the diode will remain in the short-circuit state with a current $I_{reverse}$ determined by the network parameters. Eventually, when this storage phase has passed, the current will be reduced in level to that associated with the nonconduction state. This second period of time is denoted by t_t (transition interval). The reverse recovery time is the sum of these two intervals: $t_{rr} = t_s + t_t$. This is an important consideration in high-speed switching applications. Most commercially available switching diodes have a t_{rr} in the range of a few nanoseconds to 1 μs. Units are available, however, with a t_{rr} of only a few hundred picoseconds (10^{-12} s).

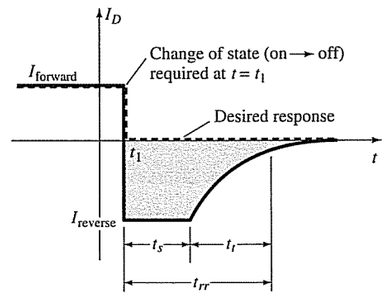


FIG. 1.35
Defining the reverse recovery time.

1.12 DIODE SPECIFICATION SHEETS

Data on specific semiconductor devices are normally provided by the manufacturer in one of two forms. Most frequently, they give a very brief description limited to perhaps one page. At other times, they give a thorough examination of the characteristics using graphs, artwork, tables, and so on. In either case, there are specific pieces of data that must be included for proper use of the device. They include:

1. The forward voltage V_F (at a specified current and temperature)
2. The maximum forward current I_F (at a specified temperature)
3. The reverse saturation current I_R (at a specified voltage and temperature)
4. The reverse-voltage rating [PIV or PRV or V(BR), where BR comes from the term "breakdown" (at a specified temperature)]

DIFFUSED SILICON PLANAR

A — • BV . . . 125 V (MIN) @ 100 μA (BAY73)

ABSOLUTE MAXIMUM RATINGS (Note 1)

Temperatures

Storage Temperature Range	–65°C to +200°C
B — Maximum Junction Operating Temperature	+175°C
Lead Temperature	+260°C

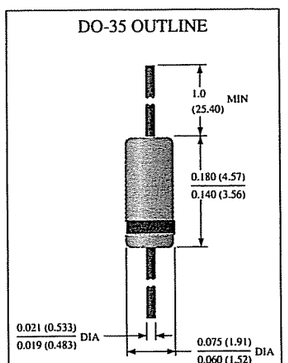
Power Dissipation (Note 2)

C — Maximum Total Power Dissipation at 25°C Ambient	500 mW
Linear Power Derating Factor (from 25°C)	3.33 mW/°C

Maximum Voltage and Currents

WIV	Working Inverse Voltage	BAY73	100 V
I_O	Average Rectified Current		200 mA
D — I_F	Continuous Forward Current		500 mA
i_f	Peak Repetitive Forward Current		600 mA
$i_{f\,(surge)}$	Peak Forward Surge Current		
	Pulse Width = 1 s		1.0 A
	Pulse Width = 1 μs		4.0 A

DO-35 OUTLINE



NOTES:
Copper clad steel leads, tin plated
Gold plated leads available
Hermetically sealed glass package
Package weight is 0.14 gram

ELECTRICAL CHARACTERISTICS (25°C Ambient Temperature unless otherwise noted)

SYMBOL	CHARACTERISTIC	BAY73 MIN	BAY73 MAX	UNITS	TEST CONDITIONS
E — V_F	Forward Voltage	0.85	1.00	V	I_F = 200 mA
		0.81	0.94	V	I_F = 100 mA
		0.78	0.88	V	I_F = 50 mA
		0.69	0.80	V	I_F = 10 mA
		0.67	0.75	V	I_F = 5.0 mA
		0.60	0.68	V	I_F = 1.0 mA
F — I_R	Reverse Current		500	nA	V_R = 20 V, T_A = 125°C
			1.0	μA	V_R = 100 V, T_A = 125°C
			0.2	nA	V_R = 20 V, T_A = 25°C
			0.5	nA	V_R = 100 V, T_A = 25°C
BV	Breakdown Voltage	125		V	I_R = 100 μA
G — C	Capacitance		8.0	pF	V_R = 0, f = 1.0 MHz
H — t_{rr}	Reverse Recovery Time		3.0	μs	I_F = 10 mA, V_R = 35 V, R_L = 1.0 to 100 kΩ, C_L = 10 pF, JAN 256

NOTES
1 These ratings are limiting values above which the serviceability of the diode may be impaired.
2 These are steady state limits. The factory should be consulted on applications involving pulses or low duty-cycle operation.

FIG. 1.36
Electrical characteristics of a high-voltage, low-leakage diode.

5. The maximum power dissipation level at a particular temperature
6. Capacitance levels
7. Reverse recovery time t_{rr}
8. Operating temperature range

Depending on the type of diode being considered, additional data may also be provided, such as frequency range, noise level, switching time, thermal resistance levels, and peak repetitive values. For the application in mind, the significance of the data will usually be self-apparent. If the maximum power or dissipation rating is also provided, it is understood to be equal to the following product:

$$P_{D\,\max} = V_D I_D \tag{1.8}$$

where I_D and V_D are the diode current and voltage, respectively, at a particular point of operation.

If we apply the simplified model for a particular application (a common occurrence), we can substitute $V_D = V_T = 0.7$ V for a silicon diode in Eq. (1.8) and determine the resulting power dissipation for comparison against the maximum power rating. That is,

$$P_{\text{dissipated}} \cong (0.7\text{ V})I_D \tag{1.9}$$

The data provided for a high-voltage/low-leakage diode appear in Figs. 1.36 and 1.37. This example would represent the expanded list of data and characteristics. The term *rectifier* is applied to a diode when it is frequently used in a *rectification* process, described in Chapter 2.

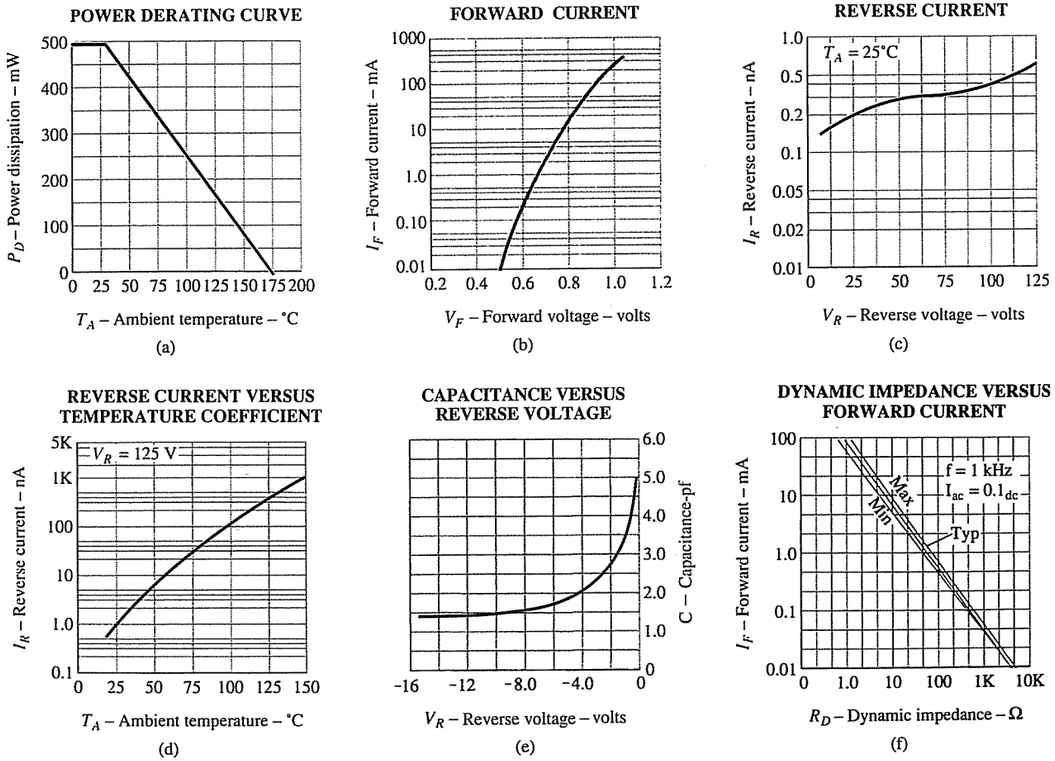


FIG. 1.37
Terminal characteristics of a high-voltage diode.

Specific areas of the specification sheet are highlighted in blue, with letters corresponding to the following description:

A The data sheet highlights the fact that the silicon high-voltage diode has a *minimum* reverse-bias voltage of 125 V at a specified reverse-bias current.

B Note the wide range of temperature operation. Always be aware that data sheets typically use the centigrade scale, with 200°C = 392°F and −65°C = −85°F.

C The maximum power dissipation level is given by $P_D = V_D I_D = 500\ \text{mW} = 0.5\ \text{W}$. The effect of the linear derating factor of 3.33 mW/°C is demonstrated in Fig. 1.37a. Once the temperature exceeds 25°C the maximum power rating will drop by 3.33 mW for each 1°C increase in temperature. At a temperature of 100°C, which is the boiling point of water, the maximum power rating has dropped to one half of its original value. An initial temperature of 25°C is typical inside a cabinet containing operating electronic equipment in a low-power situation.

D The maximum sustainable current is 500 mA. The plot of Fig. 1.37b reveals that the forward current at 0.5 V is about 0.01 mA, but jumps to 1 mA (100 times greater) at about 0.65 V. At 0.8 V the current is more than 10 mA, and just above 0.9 V it is close to 100 mA. The curve of Fig. 1.37b certainly looks nothing like the characteristic curves appearing in the last few sections. This is a result of using a log scale for the current and a linear scale for the voltage.

Log scales are often used to provide a broader range of values for a variable in a limited amount of space.

If a linear scale were used for the current, it would be impossible to show a range of values from 0.01 mA to 1000 mA. If the vertical divisions were in 0.01-mA increments, it would take 100,000 equal intervals on the vertical axis to reach 1000 mA. For the moment recognize that the voltage level at given levels of current can be found by using the intersection with the curve. For vertical values above a level such as 1.0 mA, the next level is 2 mA, followed by 3 mA, 4 mA, and 5 mA. The levels of 6 mA to 10 mA can be determined by simply dividing the distance into equal intervals (not the true distribution, but close enough for the provided graphs). For the next level it would be 10 mA, 20 mA, 30 mA, and so on. The graph of Fig. 1.37b is called a *semi-log plot* to reflect the fact that only one axis uses a log scale. A great deal more will be said about log scales in Chapter 9.

E The data provide a range of V_F (forward-bias voltages) for each current level. The higher the forward current, the higher is the applied forward bias. At 1 mA we find V_F can range from 0.6 V to 0.68 V, but at 200 mA it can be as high as 0.85 V to 1.00 V. For the full range of current levels with 0.6 V at 1 mA and 0.85 V at 200 mA it is certainly a reasonable approximation to use 0.7 V as the average value.

F The data provided clearly reveal how the reverse saturation current increases with applied reverse bias at a fixed temperature. At 25°C the maximum reverse-bias current increases from 0.2 nA to 0.5 nA due to an increase in reverse-bias voltage by the same factor of 5. At 125°C it jumps by a factor of 2 to the high level of 1 μA. Note the extreme change in reverse saturation current with temperature as the maximum current rating jumps from 0.2 nA at 25°C to 500 nA at 125°C (at a fixed reverse-bias voltage of 20 V). A similar increase occurs at a reverse-bias potential of 100 V. The semi-log plots of Figs. 1.37c and 1.37d provide an indication of how the reverse saturation current changes with changes in reverse voltage and temperature. At first glance Fig. 1.37c might suggest that the reverse saturation current is fairly steady for changes in reverse voltage. However, this can sometimes be the effect of using a log scale for the vertical axis. The current has actually changed from a level of 0.2 nA to a level of 0.7 nA for the range of voltages representing a change of almost 6 to 1. The dramatic effect of temperature on the reverse saturation current is clearly displayed in Fig. 1.37d. At a reverse-bias voltage of 125 V the reverse-bias current increases from a level of about 1 nA at 25°C to about 1 μA at 150°C, an increase of a factor of 1000 over the initial value.

Temperature and applied reverse bias are very important factors in designs sensitive to the reverse saturation current.

G As shown in the data listing and on Fig. 1.37e, the transition capacitance at a reverse-bias voltage of 0 V is 6 pF at a test frequency of 1 MHz. Note the severe change in capacitance level as the reverse-bias voltage is increased. As mentioned earlier, this sensitive region can be put to good use in the design of a device (Varactor; Chapter 16) whose terminal capacitance is sensitive to the applied voltage.

H The reverse recovery time is 3 μs for the test conditions shown. This is not a fast time for some of the current high-performance systems in use today. However, for a variety of low- and mid-frequency applications it is acceptable.

The curves of Fig. 1.37f provide an indication of the magnitude of the ac resistance of the diode versus forward current. Section 1.8 clearly demonstrated that the dynamic resistance of a diode decreases with increase in current. As we go up the current axis of Fig. 1.37f it is clear that if we follow the curve, the dynamic resistance will decrease. At 0.1 mA it is close to 1 kΩ; at 10 mA, 10 Ω; and at 100 mA, only 1 Ω; this clearly supports the earlier discussion. Unless one has had experience reading log scales, the curve is challenging to read for levels between those indicated because it is a *log–log* plot. Both the vertical axis and the horizontal axis employ a log scale.

The more one is exposed to specification sheets, the "friendlier" they will become, especially when the impact of each parameter is clearly understood for the application under investigation.

1.13 SEMICONDUCTOR DIODE NOTATION

The notation most frequently used for semiconductor diodes is provided in Fig. 1.38. For most diodes any marking such as a dot or band, as shown in Fig. 1.38, appears at the cathode end. The terminology anode and cathode is a carryover from vacuum-tube notation. The anode refers to the higher or positive potential, and the cathode refers to the lower or negative terminal. This combination of bias levels will result in a forward-bias or "on" condition for the diode. A number of commercially available semiconductor diodes appear in Fig. 1.39.

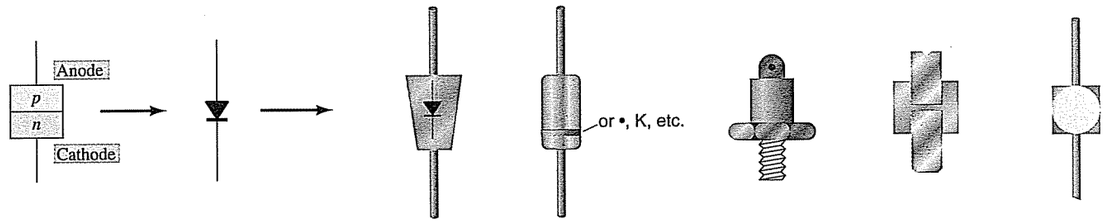


FIG. 1.38
Semiconductor diode notation.

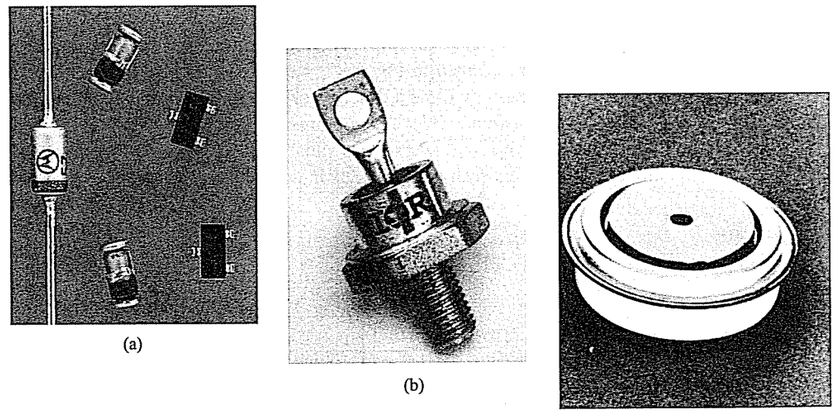


FIG. 1.39
Various types of junction diodes. [(a) Courtesy of Motorola Inc.; (b) and (c) Courtesy International Rectifier Corporation.]

1.14 DIODE TESTING

The condition of a semiconductor diode can be determined quickly using (1) a digital display meter (DDM) with a *diode checking function*, (2) the *ohmmeter section* of a multimeter, or (3) a *curve tracer.*



FIG. 1.40
Digital display meter. (Courtesy of Fluke Corporation. Reproduced with permission.)

Diode Checking Function

A digital display meter with a diode checking capability appears in Fig. 1.40. Note the small diode symbol as the bottom option of the rotating dial. When set in this position and hooked up as shown in Fig. 1.41a, the diode should be in the "on" state and the display will provide an indication of the forward-bias voltage such as 0.67 V (for Si). The meter has an internal constant-current source (about 2 mA) that will define the voltage level as indicated in Fig. 1.41b. An OL indication with the hookup of Fig. 1.41a reveals an open (defective) diode. If the leads are reversed, an OL indication should result due to the expected open-circuit equivalence for the diode. In general, therefore, an OL indication in both directions is an indication of an open or defective diode.

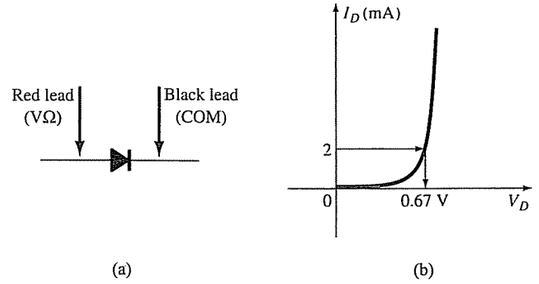


FIG. 1.41
Checking a diode in the forward-bias state.

Ohmmeter Testing

In Section 1.8 we found that the forward-bias resistance of a semiconductor diode is quite low compared to the reverse-bias level. Therefore, if we measure the resistance of a diode using the connections indicated in Fig. 1.42, we can expect a relatively low level. The resulting ohmmeter indication will be a function of the current established through the diode by the internal battery (often 1.5 V) of the ohmmeter circuit. The higher the current, the lower is the resistance level. For the reverse-bias situation the reading should be quite high, requiring a high resistance scale on the meter, as indicated in Fig. 1.42b. A high resistance reading in both directions obviously indicates an open (defective-device) condition, whereas a very low resistance reading in both directions will probably indicate a shorted device.

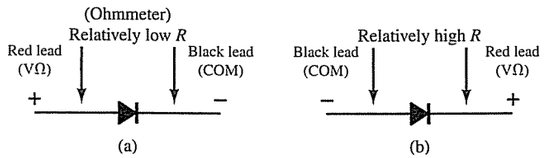


FIG. 1.42
Checking a diode with an ohmmeter.

Curve Tracer

The curve tracer of Fig. 1.43 can display the characteristics of a host of devices, including the semiconductor diode. By properly connecting the diode to the test panel at the bottom center of the unit and adjusting the controls, one can obtain the display of Fig. 1.44. Note that the vertical scaling is 1 mA/div, resulting in the levels indicated. For the horizontal axis the scaling is 100 mV/div, resulting in the voltage levels indicated. For a 2-mA level as defined for a DDM, the resulting voltage would be about 625 mV = 0.625 V. Although the instrument initially appears quite complex, the instruction manual and a few moments of exposure will reveal that the desired results can usually be obtained without an excessive amount of effort and time. The display of the instrument will appear on more than one occasion in the chapters to follow as we investigate the characteristics of the variety of devices.

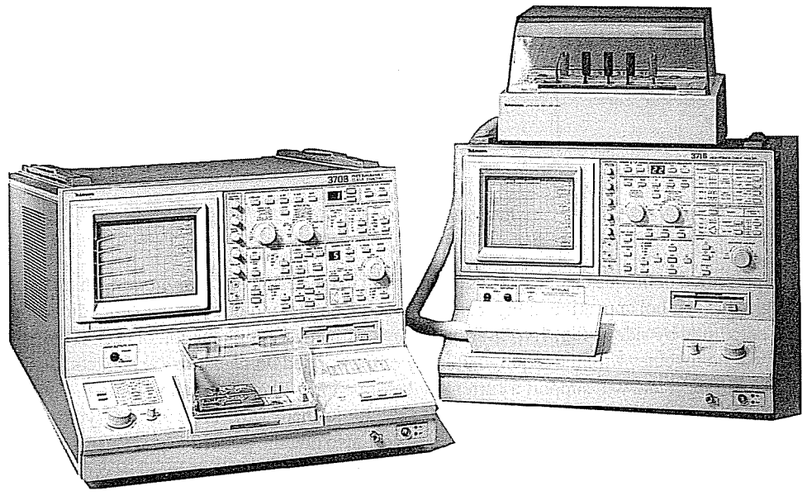


FIG. 1.43
Curve tracers. (Used with permission from Tektronix Inc.)

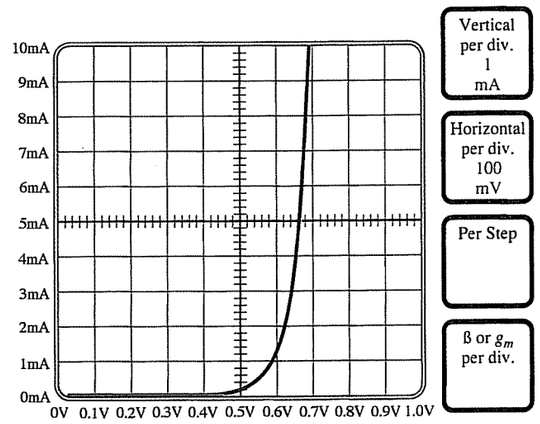


FIG. 1.44
Curve tracer response to IN4007 silicon diode.

1.15 ZENER DIODES

The Zener region of Fig. 1.45 was discussed in some detail in Section 1.6. The characteristic drops in an almost vertical manner at a reverse-bias potential denoted V_Z. The fact that the curve drops down and away from the horizontal axis rather than up and away for the positive-V_D region reveals that the current in the Zener region has a direction opposite to that of a forward-biased diode. The slight slope to the curve in the Zener region reveals that there is a level of resistance to be associated with the Zener diode in the conduction mode.

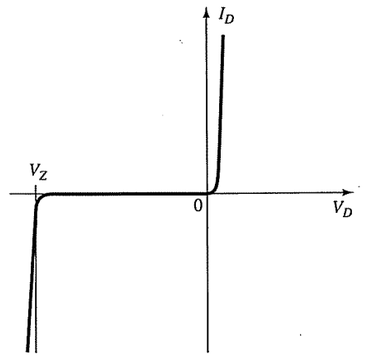


FIG. 1.45
Reviewing the Zener region.

This region of unique characteristics is employed in the design of *Zener diodes*, which have the graphic symbol appearing in Fig. 1.46a. The semiconductor diode and the Zener diode are presented side by side in Fig. 1.46 to ensure that the direction of conduction of each is clearly understood together with the required polarity of the applied voltage. For the semiconductor diode the "on" state will support a current in the direction of the arrow in the symbol. For the Zener diode the direction of conduction is opposite to that of the arrow in the symbol, as pointed out in the introduction to this section. Note also that the polarity of V_D and V_Z are the same as would be obtained if each were a resistive element as shown in Fig. 1.46c.

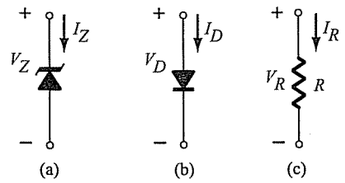


FIG. 1.46
Conduction direction: (a) Zener diode; (b) semiconductor diode; (c) resistive element.

The location of the Zener region can be controlled by varying the doping levels. An increase in doping that produces an increase in the number of added impurities, will decrease the Zener potential. Zener diodes are available having Zener potentials of 1.8 V to 200 V with power ratings from ¼ W to 50 W. Because of its excellent temperature and current capabilities, silicon is the preferred material in the manufacture of Zener diodes.

It would be nice to assume the Zener diode is ideal with a straight vertical line at the Zener potential. However, there is a slight slope to the characteristics requiring the piecewise equivalent model appearing in Fig. 1.47 for that region. For most of the applications appearing in this text the series resistive element can be ignored and the reduced equivalent model of just a dc battery of V_Z volts employed. Since some applications of Zener diodes

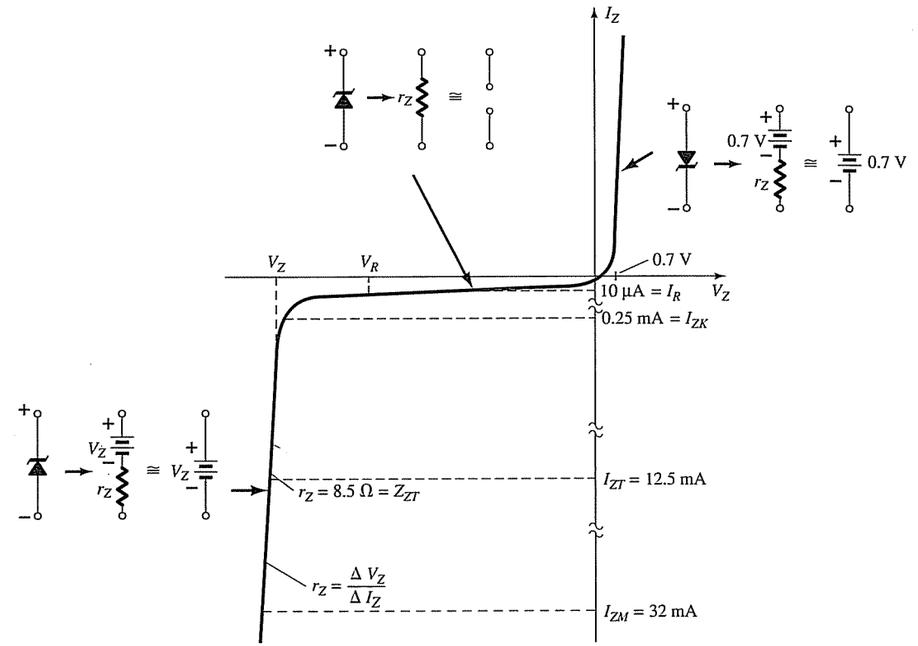


FIG. 1.47
Zener diode characteristics with the equivalent model for each region.

swing between the Zener region and the forward-bias region, it is important to understand the operation of the Zener diode in all regions. As shown in Fig. 1.47, the equivalent model for a Zener diode in the reverse-bias region below V_Z is a very large resistor (as for the standard diode). For most applications this resistance is so large it can be ignored and the open-circuit equivalent employed. For the forward-bias region the piecewise equivalent is the same as described in earlier sections.

The specification sheet for a 10-V, 500-mW, 20% Zener diode is provided as Table 1.7, and a plot of the important parameters is given in Fig. 1.48. The term *nominal* used in the specification of the Zener voltage simply indicates that it is a typical average value. Since this is a 20% diode, the Zener potential of the unit one picks out of a *lot* (a term used to describe a package of diodes) can be expected to vary as 10 V + 20%, or from 8 V to 12 V. Both 10% and 50% diodes are also readily available. The test current I_{ZT} is the current defined by the ¼-power level. It is the current that will define the dynamic resistance Z_{ZT} and appears in the general equation for the power rating of the device. That is,

$$\boxed{P_{Z_{max}} = 4I_{ZT}V_Z} \tag{1.10}$$

Substituting I_{ZT} into the equation with the nominal Zener voltage results in

$$P_{Z_{max}} = 4I_{ZT}V_Z = 4(12.5\,\text{mA})(10\,\text{V}) = 500\,\text{mW}$$

TABLE 1.7
Electrical Characteristics (25°C Ambient Temperature)

Zener Voltage Nominal V_Z (V)	Test Current I_{ZT} (mA)	Maximum Dynamic Impedance Z_{ZT} at I_{ZT} (Ω)	Maximum Knee Impedance Z_{ZK} at I_{ZK} (Ω)	(mA)	Maximum Reverse Current I_R at V_R (μA)	Test Voltage V_R (V)	Maximum Regulator Current I_{ZM} (mA)	Typical Temperature Coefficient (%/°C)
10	12.5	8.5	700	0.25	10	7.2	32	+0.072

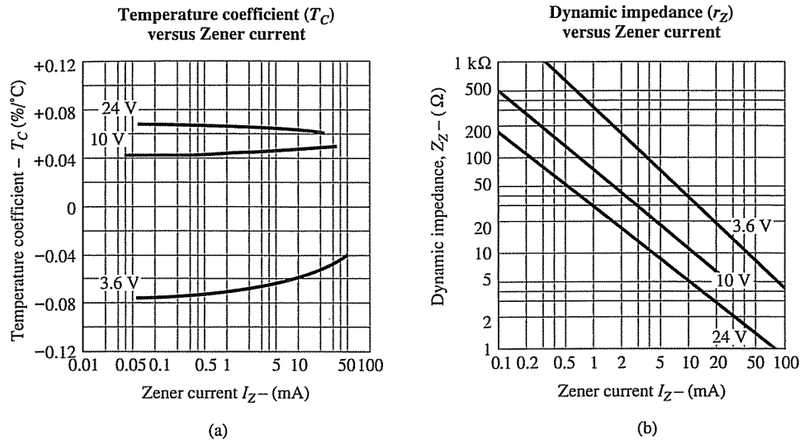


FIG. 1.48
Electrical characteristics for a 10-V, 500-mW Zener diode.

which matches the 500-mW label appearing above. For this device the dynamic resistance is 8.5 Ω, which is usually small enough to be ignored in most applications. The maximum knee impedance is defined at the center of the knee at a current of $I_{ZK} = 0.25$ mA. Note that in all the above the letter T is used in subscripts to indicate test values and the letter K to indicate knee values. For any level of current below 0.25 mA the resistance will only get larger in the reverse-bias region. The knee value therefore reveals when the diode will start to show very high series resistance elements that one may not be able to ignore in an application. Certainly 500 Ω = 0.5 kΩ may be a level that can come into play. At a reverse-bias voltage the application of a test voltage of 7.2 V results in a reverse saturation current of 10 μA, a level that could be of some concern in some applications. The maximum regulator current is the maximum continuous current one would want to support in the use of the Zener diode in a regulator configuration. Finally, we have the temperature coefficient (T_C) in percent per degree centigrade.

The Zener potential of a Zener diode is very sensitive to the temperature of operation.

The temperature coefficient can be used to find the change in Zener potential due to a change in temperature using the following equation:

$$T_C = \frac{\Delta V_Z / V_Z}{T_1 - T_0} \times 100\%/°C \quad (\%/°C) \tag{1.11}$$

where T_1 is the new temperature level
T_0 is room temperature in an enclosed cabinet (25°C)
T_C is the temperature coefficient
and V_Z is the nominal Zener potential at 25°C.

To demonstrate the effect of the temperature coefficient on the Zener potential, consider the following example.

EXAMPLE 1.4 Analyze the 10-V Zener diode described by Table 1.7 if the temperature is increased to 100°C (the boiling point of water).

Solution: Substituting into Eq. (1.11), we obtain

$$\Delta V_Z = \frac{T_C V_Z}{100\%}(T_1 - T_0)$$

$$= \frac{(0.072\%/°C)(10\text{ V})}{100\%}(100°C - 25°C)$$

and $$\Delta V_Z = 0.54\text{ V}$$

The resulting Zener potential is now

$$V_Z' = V_Z + 0.54\text{ V} = \mathbf{10.54\text{ V}}$$

which is not an insignificant change.

It is important to realize that in this case the temperature coefficient was positive. For Zener diodes with Zener potentials less than 5 V it is very common to see negative temperature coefficients, where the Zener voltage drops with an increase in temperature. Figure 1.48a provides a plot of T versus Zener current for three different levels of diodes. Note that the 3.6-V diode has a negative temperature coefficient, whereas the others have positive values.

The change in dynamic resistance with current for the Zener diode in its avalanche region is provided in Fig. 1.48b. Again, we have a log–log plot, which has to be carefully read. Initially it would appear that there is an inverse linear relationship between the dynamic resistance because of the straight line. That would imply that if one doubles the current, one cuts the resistance in half. However, it is only the log–log plot that gives this impression, because if we plot the dynamic resistance for the 24-V Zener diode versus current using linear scales we obtain the plot of Fig. 1.49, which is almost exponential in appearance. Note on both plots that the dynamic resistance at very low currents that enter the knee of the curve is fairly high at about 200 Ω. However, at higher Zener currents, away from the knee, at, say 10 mA, the dynamic resistance drops to about 5 Ω.

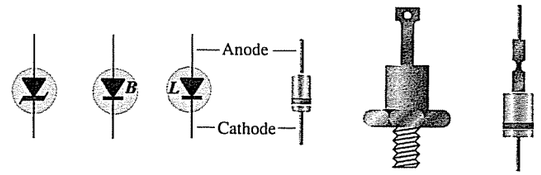


FIG. 1.49
Zener terminal identification and symbols.

The terminal identification and the casing for a variety of Zener diodes appear in Fig. 1.49. Figure 1.50 provides a photograph of a variety of Zener diodes. Their appearance is similar in many ways to that of the standard diode. Some areas of application for the Zener diode will be examined in Chapter 2.

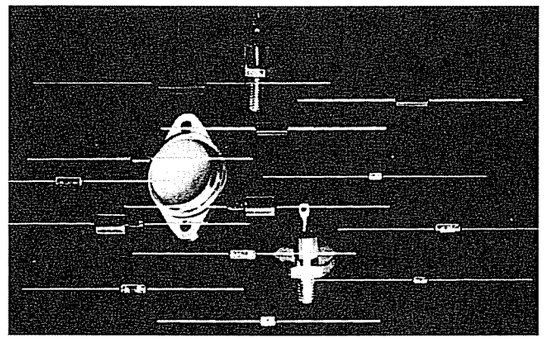


FIG. 1.50
Zener diodes. (Courtesy Siemens Corporation.)

1.16 LIGHT-EMITTING DIODES

The increasing use of digital displays in calculators, watches, and all forms of instrumentation has contributed to an extensive interest in structures that emit light when properly biased. The two types in common use to perform this function are the light-emitting diode (LED)

and the liquid-crystal display (LCD). Since the LED falls within the family of p–n junction devices and will appear in some of the networks of the next few chapters, it will be introduced in this chapter. The LCD display is described in Chapter 16.

As the name implies, the light-emitting diode is a diode that gives off visible or invisible (infrared) light when energized. In any forward-biased p–n junction there is, within the structure and primarily close to the junction, a recombination of holes and electrons. This recombination requires that the energy possessed by the unbound free electrons be transferred to another state. In all semiconductor p–n junctions some of this energy is given off in the form of heat and some in the form of photons.

In Si and Ge diodes the greater percentage of the energy converted during recombination at the junction is dissipated in the form of heat within the structure, and the emitted light is insignificant.

For this reason, silicon and germanium are not used in the construction of LED devices. On the other hand:

Diodes constructed of GaAs emit light in the infrared (invisible) zone during the recombination process at the p–n junction.

Even though the light is not visible, infrared LEDs have numerous applications where visible light is not a desirable effect. These include security systems, industrial processing, optical coupling, safety controls such as on garage door openers, and in home entertainment centers, where the infrared light of the remote control is the controlling element.

Through other combinations of elements a coherent visible light can be generated. Table 1.8 provides a list of common compound semiconductors and the light they generate. In addition, the typical range of forward bias potentials for each is listed.

TABLE 1.8
Light-Emitting Diodes

Color	Construction	Typical Forward Voltage (V)
Amber	AlInGaP	2.1
Blue	GaN	5.0
Green	GaP	2.2
Orange	GaAsP	2.0
Red	GaAsP	1.8
White	GaN	4.1
Yellow	AlInGaP	2.1

The basic construction of an LED appears in Fig. 1.51 with the standard symbol used for the device. The external metallic conducting surface connected to the p-type material is smaller to permit the emergence of the maximum number of photons of light energy when the device is forward-biased. Note in the figure that the recombination of the injected carriers due to the forward-biased junction results in emitted light at the site of the recombination. There will, of course, be some absorption of the packages of photon energy in the structure itself, but a very large percentage can leave, as shown in the figure.

Just as different sounds have different frequency spectra (high-pitched sounds generally have high-frequency components, and low sounds have a variety of low-frequency components), the same is true for different light emissions.

The frequency spectrum for infrared light extends from about 100 THz (T = tera = 10^{12}) to 400 THz, with the visible light spectrum extending from about 400 to 750 THz.

It is interesting to note that invisible light has a lower frequency spectrum than visible light.

In general, when one talks about the response of electroluminescent devices, one references their wavelength rather than their frequency.

The two quantities are related by the following equation:

$$\lambda = \frac{c}{f} \quad \text{(m)} \tag{1.12}$$

where $c = 3 \times 10^8$ m/s (the speed of light in a vacuum)
$f =$ frequency in Hertz
$\lambda =$ wavelength in meters.

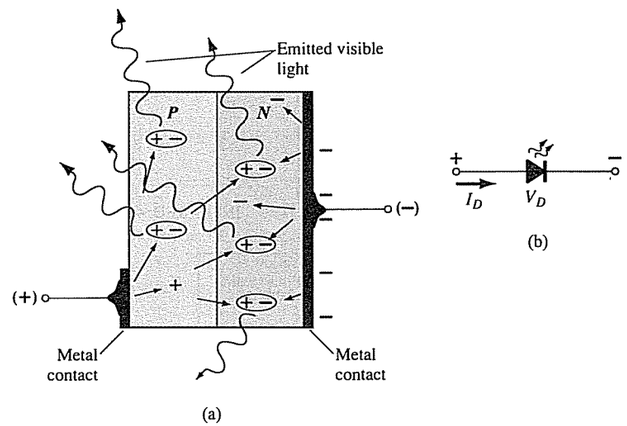


FIG. 1.51
(a) Process of electroluminescence in the LED; (b) graphic symbol.



EXAMPLE 1.5 Using Eq. (1.12), find the wavelength for the frequency range provided for visible light above.

Solution:

$$c = 3 \times 10^8 \frac{\text{m}}{\text{s}}\left[\frac{10^9 \text{ nm}}{\text{m}}\right] = 3 \times 10^{17} \text{ nm/s}$$

$$\lambda = \frac{c}{f} = \frac{3 \times 10^{17} \text{ nm/s}}{400 \text{ THz}} = \frac{3 \times 10^{17} \text{ nm/s}}{400 \times 10^{12} \text{ Hz}} = \mathbf{750 \text{ nm}}$$

$$\lambda = \frac{c}{f} = \frac{3 \times 10^{17} \text{ nm/s}}{750 \text{ THz}} = \frac{3 \times 10^{17} \text{ nm/s}}{750 \times 10^{12} \text{ Hz}} = \mathbf{400 \text{ nm}}$$

Note in the above example the resulting inversion from higher frequency to smaller wavelength. That is, the higher frequency results in the smaller wavelength. Also, most charts use either nanometers (nm) or angstrom (Å) units. One angstrom unit is equal to 10^{-10} m.

The response of the average human eye is provided in Fig. 1.52. It extends from about 350 nm to 800 nm with a peak near 550 nm. It is interesting to note that the peak response of the eye is to the color green, with red and blue at the lower ends of the bell curve. The curve reveals that a red or a blue LED must have a much stronger efficiency than a green one to be visible at the same intensity. In other words, the eye is more sensitive to the color green than to other colors. Keep in mind that the wavelengths shown are for the peak response of each color. All the colors indicated on the plot will have a bell-shaped curve response, so green, for example, is still visible at 600 nm, but at a lower intensity level.

In Section 1.4 it was mentioned briefly that GaAs with its higher energy gap of 1.43 eV made it suitable for electromagnetic radiation of visible light, whereas Si at 1.1 eV resulted primarily in heat dissipation on recombination. The effect of this difference in energy gaps can be explained to some degree by realizing that to move an electron from one discrete energy level to another requires a specific amount of energy. The amount of energy involved is given by

$$E_g = \frac{hc}{\lambda} \tag{1.13}$$

with $h =$ Planck's constant $= 6.626 \times 10^{-34}$ J · s.

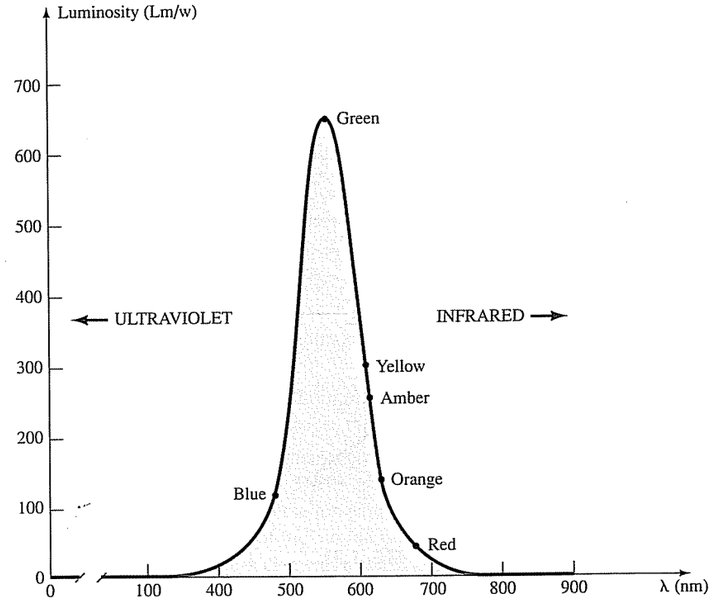


FIG. 1.52

Standard response curve of the human eye, showing the eye's response to light energy peaks at green and falls off for blue and red.

If we substitute the energy gap level of 1.43 eV into the equation, we obtain the following wavelength:

$$1.43 \cancel{eV}\left[\frac{1.6 \times 10^{-19}\ \text{J}}{1\ \cancel{eV}}\right] = 2.288 \times 10^{-19}\ \text{J}$$

and

$$\lambda = \frac{hc}{E_g} = \frac{(6.626 \times 10^{-34}\ \text{J}\cdot\text{s})(3 \times 10^{8}\ \text{m/s})}{2.288 \times 10^{-19}\ \text{J}}$$

$$= \mathbf{869\ nm}$$

This certainly places GaAs in the wavelength zone typically used in infrared devices. For a compound material such as GaAsP with a band gap of 1.9 eV the resulting wavelength is 654 nm, which is in the center of the red zone, making it an excellent compound semiconductor for LED production. In general, therefore:

The wavelength and frequency of light of a specific color are directly related to the energy band gap of the material.

A first step, therefore, in the production of a compound semiconductor that can be used to generate light is to come up with a combination of elements that will generate the desired energy band gap.

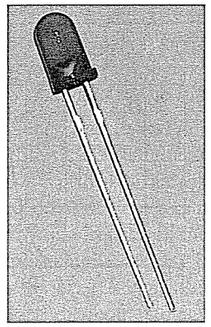
The appearance and characteristics of a subminiature high-efficiency red LED manufactured by Hewlett-Packard are given in Fig. 1.53. Note in Fig. 1.53b that the peak forward current is 60 mA, with 20 mA the typical average forward current. The text conditions listed in Fig. 1.53c, however, are for a forward current of 10 mA. The level of V_D under forward-bias conditions is listed as V_F and extends from 2.2 to 3 V. In other words, one can expect a typical operating current of about 10 mA at 2.3 V for good light emission, as shown in Fig. 1.53e. In particular, note the typical diode characteristics for an LED, permitting similar analysis techniques to be described in the next chapter.

Two quantities yet undefined appear under the heading Electrical/Optical Characteristics at $T_A = 25°C$. They are the *axial luminous intensity* (I_V) and the *luminous efficacy* (η_V). Light intensity is measured in *candelas*. One candela (cd) corresponds to a light flux of 4π lumens (lm) and is equivalent to an illumination of *1 footcandle* on a 1-ft^2 area 1 ft from the light source. Even if this description may not provide a clear understanding of the candela as a unit of measure, it should be enough to allow its level to be compared between similar devices. Figure 1.53f is a normalized plot of the relative luminous intensity versus forward current. The term *normalized* is used frequently on graphs to give comparisons of response to a particular level.

A normalized plot is one where the variable of interest is plotted with a specific level defined as the reference value with a magnitude of one.

In Fig. 1.53f the normalized level is taken at $I_F = 10$ mA. Note that the relative luminous intensity is one at $I_F = 10$ mA. The graph quickly reveals that the intensity of the light is almost doubled at a current of 15 mA and is almost three times as much at a current of 30 mA. It is important to therefore note that:

The light intensity of an LED will increase with forward current until a point of saturation arrives where any further increase in current will not effectively increase the level of illumination.



(a)

Absolute Maximum Ratings at $T_A = 25°C$

Parameter	*High-Efficiency Red 4160*	*Units*
Power dissipation	120	mW
Average forward current	20[1]	mA
Peak forward current	60	mA
Operating and storage temperature range	–55°C to 100°C	
Lead soldering temperature [1.6 mm (0.063 in.) from body]	230°C for 3 s	

NOTE: 1. Derate from 50°C at 0.2 mV/°C.

(b)

Electrical/Optical Characteristics at $T_A = 25°C$

Symbol	*Description*	*High-Efficiency Red 4160* Min.	Typ.	Max.	*Units*	*Test Conditions*
						$I_F = 10$ mA
I_V	Axial luminous intensity	1.0	3.0		mcd	
$2\theta_{1/2}$	Included angle between half luminous intensity points		80		degree	Note 1
λ_{peak}	Peak wavelength		635		nm	Measurement at peak
λ_d	Dominant wavelength		628		nm	Note 2
τ_s	Speed of response		90		ns	
C	Capacitance		11		pF	$V_F = 0$; $f = 1$ Mhz
θ_{JC}	Thermal resistance		120		°C/W	Junction to cathode lead at 0.79 mm (0.031 in.) from body
V_F	Forward voltage		2.2	3.0	V	$I_F = 10$ mA
BV_R	Reverse breakdown voltage	5.0			V	$I_R = 100\ \mu$A
η_v	Luminous efficacy		147		lm/W	Note 3

NOTES:
1. $\theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength that defines the color of the device.
3. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_v/\eta_v$, where I_v is the luminous intensity in candelas and η_v is the luminous efficacy in lumens/watt.

(c)

FIG. 1.53

Hewlett-Packard subminiature high-efficiency red solid-state lamp: (a) appearance; (b) absolute maximum ratings; (c) electrical/optical characteristics; (d) relative intensity versus wavelength; (e) forward current versus forward voltage; (f) relative luminous intensity versus forward current; (g) relative efficiency versus peak current; (h) relative luminous intensity versus angular displacement. (Courtesy Hewlett-Packard Corporation.)

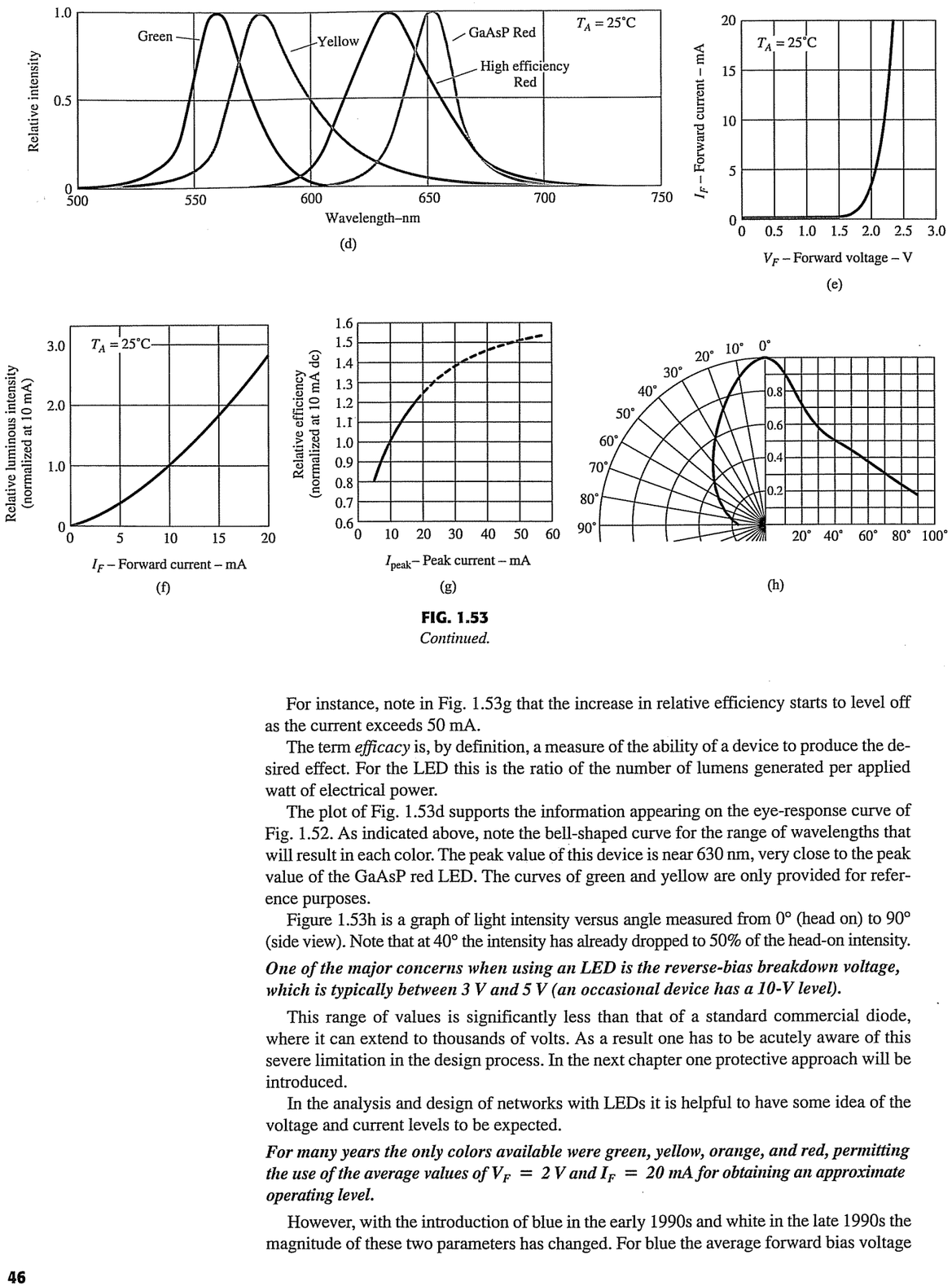


FIG. 1.53
Continued.

For instance, note in Fig. 1.53g that the increase in relative efficiency starts to level off as the current exceeds 50 mA.

The term *efficacy* is, by definition, a measure of the ability of a device to produce the desired effect. For the LED this is the ratio of the number of lumens generated per applied watt of electrical power.

The plot of Fig. 1.53d supports the information appearing on the eye-response curve of Fig. 1.52. As indicated above, note the bell-shaped curve for the range of wavelengths that will result in each color. The peak value of this device is near 630 nm, very close to the peak value of the GaAsP red LED. The curves of green and yellow are only provided for reference purposes.

Figure 1.53h is a graph of light intensity versus angle measured from 0° (head on) to 90° (side view). Note that at 40° the intensity has already dropped to 50% of the head-on intensity.

One of the major concerns when using an LED is the reverse-bias breakdown voltage, which is typically between 3 V and 5 V (an occasional device has a 10-V level).

This range of values is significantly less than that of a standard commercial diode, where it can extend to thousands of volts. As a result one has to be acutely aware of this severe limitation in the design process. In the next chapter one protective approach will be introduced.

In the analysis and design of networks with LEDs it is helpful to have some idea of the voltage and current levels to be expected.

For many years the only colors available were green, yellow, orange, and red, permitting the use of the average values of $V_F = 2$ V and $I_F = 20$ mA for obtaining an approximate operating level.

However, with the introduction of blue in the early 1990s and white in the late 1990s the magnitude of these two parameters has changed. For blue the average forward bias voltage

can be as high as 5 V, and for white about 4.1 V, although both have a typical operating current of 20 mA or more. In general, therefore:

Assume an average forward-bias voltage of 5 V for blue and 4 V for white LEDs at currents of 20 mA to initiate an analysis of networks with these types of LEDs.

Every once in a while a device is introduced that seems to open the door to a slue of possibilities. Such is the case with the introduction of white LEDs. The slow start for white LEDs is primarily due to the fact that it is not a primary color like green, blue, and red. Every other color that one requires, such as on a TV screen, can be generated from these three colors (as in virtually all monitors available today). Yes, the right combination of these three colors can give white—hard to believe, but it works. The best evidence is the human eye, which only has cones sensitive to red, green, and blue. The brain is responsible for processing the input and perceiving the "white" light and color we see in our everyday lives. The same reasoning was used to generate some of the first white LEDs, by combining the right proportions of a red, a green, and a blue LED in a single package. Today, however, most white LEDs are constructed of a blue *gallium nitride* LED below a film *of yttrium-aluminum garnet* (YAG) phosphor. When the blue light hits the phosphor, a yellow light is generated. The mix of this yellow emission with that of the central blue LED forms a white light—incredible, but true.

Now, we have an LED that gives off white light, as shown in Fig. 1.54a; what are its limitations, considering that most of the lighting for homes and offices is a white light? The thought that these small solid-state devices with lifetimes thousands of times that of an incandescent bulb could replace current lighting techniques has entered the realm of the possible. In fact, the Fioravanti Yak concept car presented at the Geneva Motor Show uses white LEDs for its headlamps, fog lights, and signals as shown in Fig. 1.54b. Today white LEDs can generate about 25 lm/W, but in 2012 they are forecast to reach 150 lm/W, with maxima near 400 lm/W. At this rate 7 W of power will some day be able to generate 1000 lm of light, which exceeds the illumination of a 60-W bulb and can be run off four D batteries. To demonstrate the interest in this area of development, there are already specially designed offices and meeting rooms that use LEDs for their complete lighting, an exciting development to follow in the next few decades. No more fragile bulbs to replace, just solid-state devices with lifetime guarantees exceeding 10 years and significantly lower power levels.

Before leaving the subject, let us look at a seven-segment digital display housed in a typical dual in-line integrated circuit package as shown in Fig. 1.55. By energizing the proper pins with a typical 5-V dc level, a number of the LEDs can be energized and the desired numeral displayed. In Fig. 1.55a the pins are defined by looking at the face of the display and counting counterclockwise from the top left pin. Most seven-segment displays are either common-anode or common-cathode displays, with the term *anode* referring to the defined positive side of each diode and the *cathode* referring to the negative side. For the common-cathode option the pins have the functions listed in Fig. 1.55b and appear as in Fig. 1.55c. In the common-cathode configuration all the cathodes are

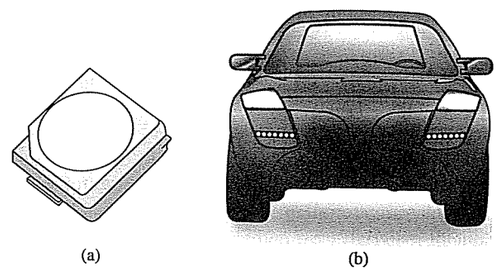
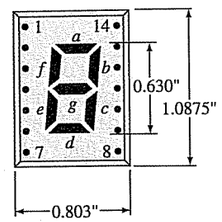
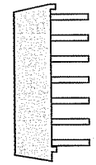
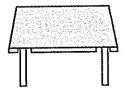


FIG. 1.54
(a) White LED unit; (b) used in the headlamps, fog lights, and turn signals of the Fioravanti Yak concept car. (After IEEE Spectrum, *September 2002.)*



(a)

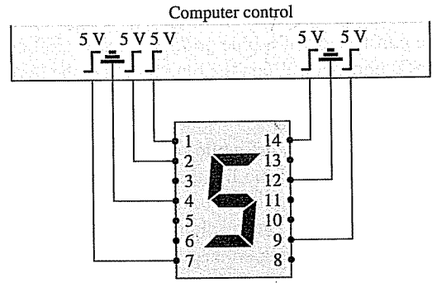




COMMON CATHODE

PIN #	FUNCTION
1.	Anode f
2.	ANODE g
3.	NO PIN
4.	COMMON CATHODE
5.	NO PIN
6.	ANODE e
7.	ANODE d
8.	ANODE c
9.	ANODE d
10.	NO PIN
11.	NO PIN
12.	COMMON CATHODE
13.	ANODE b
14.	ANODE a

(b)



(c)



Multisim

FIG. 1.55

Seven-segment display: (a) face with pin idenfication; (b) pin function; (c) displaying the numeral 5.

connected together to form a common point for the negative side of each LED. Any LED with a positive 5 V applied to the anode or numerically numbered pin side will turn on and produce light for that segment. In Fig. 1.55c, 5 V has been applied to the terminals that generate the numeral 5. For this particular unit the average forward turn-on voltage is 2.1 V at a current of 10 mA.

Various LED configurations are examined in the next chapter.

1.17 SUMMARY

Important Conclusions and Concepts

1. The characteristics of an ideal diode are a close match with those of a **simple switch** except for the important fact that an ideal diode can **conduct in only one direction**.
2. The ideal diode is a **short** in the region of conduction and an **open circuit** in the region of nonconduction.
3. A semiconductor is a material that has a conductivity level somewhere **between** that of a good conductor and that of an insulator.
4. A bonding of atoms, strengthened by the **sharing of electrons** between neighboring atoms, is called covalent bonding.
5. Increasing temperatures can cause a **significant increase** in the number of free electrons in a semiconductor material.
6. Most semiconductor materials used in the electronics industry have **negative temperature coefficients**; that is, the resistance drops with an increase in temperature.
7. Intrinsic materials are those semiconductors that have very **low level of impurities**, whereas extrinsic materials are semiconductors that have been **exposed to a doping process**.
8. An *n*-type material is formed by adding **donor** atoms that have **five** valence electrons to establish a high level of relatively free electrons. In an *n*-type material, the **electron is the majority carrier** and the hole is the minority carrier.

9. A *p*-type material is formed by adding **acceptor** atoms with **three** valence electrons to establish a high level of holes in the material. In a *p*-type material, the hole is the majority carrier and the electron is the minority carrier.
10. The region near the junction of a diode that has very few carriers is called the **depletion** region.
11. In the **absence** of any externally applied bias, the diode current is zero.
12. In the forward-bias region the diode current **increases exponentially** with increase in voltage across the diode.
13. In the reverse-bias region the diode current is the **very small reverse saturation current** until Zener breakdown is reached and current will flow in the opposite direction through the diode.
14. The reverse saturation current I_s will just about **double** in magnitude for every 10-fold increase in temperature.
15. The dc resistance of a diode is determined by the **ratio** of the diode voltage and current at the point of interest and is **not sensitive** to the shape of the curve. The dc resistance **decreases** with increase in diode current or voltage.
16. The ac resistance of a diode is sensitive to the shape of the curve in the region of interest and decreases for higher levels of diode current or voltage.
17. The threshold voltage is about **0.7 V** for silicon diodes and **0.3 V** for germanium diodes.
18. The maximum power dissipation level of a diode is equal to the **product** of the diode voltage and current.
19. The capacitance of a diode **increases exponentially** with increase in the forward-bias voltage. Its lowest levels are in the reverse-bias region.
20. The direction of conduction for a Zener diode is **opposite** to that of the arrow in the symbol, and the Zener voltage has a polarity opposite to that of a forward-biased diode.
21. Light-emitting diodes (LEDs) emit light under **forward-bias conditions** but require 2 V to 4 V for good emission.

Equations

$$I_D = I_s(e^{V_D/nV_T} - 1) \qquad V_T = \frac{kT}{q} \qquad T_K = T_C + 273° \qquad k = 1.38 \times 10^{-23}\ \text{J/K}$$

$$V_K \cong 0.7\ \text{V (Si)}$$
$$V_K \cong 1.2\ \text{V (GaAs)}$$
$$V_K \cong 0.3\ \text{V (Ge)}$$

$$R_D = \frac{V_D}{I_D}$$

$$r_d = \frac{\Delta V_d}{\Delta I_d} = \frac{26\ \text{mV}}{I_D}$$

$$r_{av} = \left.\frac{\Delta V_d}{\Delta I_d}\right|_{\text{pt. to pt.}}$$

$$P_{D_{max}} = V_D I_D$$

1.18 COMPUTER ANALYSIS

The computer has now become such an integral part of the electronics industry that the capabilities of this working "tool" must be introduced at the earliest possible opportunity. For those students with no prior computer experience there is a common initial fear of this seemingly complicated powerful system. With this in mind the computer analysis of this book was designed to make the computer system more "friendly" by revealing the relative ease with which it can be applied to perform some very helpful and special tasks in a minimum amount of time with a high degree of accuracy. The material was written with the assumption that the reader has no prior computer experience or exposure to the terminology to be applied. There is also no suggestion that the content of this book is sufficient to permit a complete understanding of the "hows" and "whys" that will surface. The purpose here is

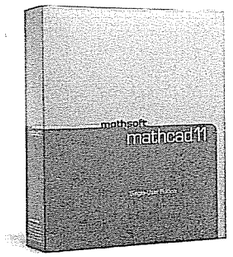


FIG. 1.56
Mathcad 11 package. (Courtesy of Mathsoft. Mathcad and Mathsoft are registered trademarks of Mathsoft Engineering and Education, Inc., http://www.mathsoft.com.)

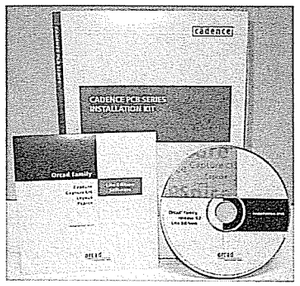


FIG. 1.57
PSpice Design package. OrCAD version 9.2.

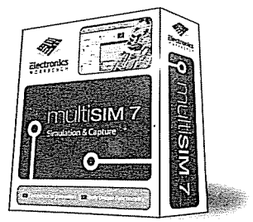


FIG. 1.58
Multisim 7. (Courtesy of Electronics Workbench.)

solely to introduce some of the terminology, discuss a few of its capabilities, reveal the possibilities available, touch on some of its limitations, and demonstrate its versatility with a number of carefully chosen examples.

In general, the computer analysis of electronic systems can take one of two approaches: using a *language* such as C++, Pascal, FORTRAN, or QBASIC; or using a *software package* such as PSpice, Multisim (Electronics Workbench, EWB), MicroCap II, Breadboard, or Circuit Master, to name a few. A language, through its symbolic notation, forms a bridge between the user and the computer that permits a dialogue between the two for establishing the operations to be performed.

In earlier editions of this text, the chosen language was BASIC, primarily because it uses a number of familiar words and phrases from the English language that in themselves reveal the operation to be performed. When a language is employed to analyze a system, a *program* is developed that sequentially defines the operations to be performed—in much the same order in which we perform the same analysis in longhand. As with the longhand approach, one wrong step and the result obtained can be completely meaningless. Programs typically develop with time and application as more efficient paths toward a solution become obvious. Once established in its "best" form it can be cataloged for future use. The important advantage of the language approach is that a program can be tailored to meet all the special needs of the user. It permits innovative "moves" by the user that can result in printouts of data in an informative and interesting manner.

The alternative approach referred to above uses a software package to perform the desired investigation. A software package is a program written and tested over a period of time designed to perform a particular type of analysis or synthesis in an efficient manner with a high level of accuracy. The package itself cannot be altered by the user, and its application is limited to the operations built into the system. A user must adjust his or her desire for output information to the range of possibilities offered by the package. In addition, the user must input information exactly as requested by the package or the data may be misinterpreted.

The software packages available today have become so extensive in their coverage and range of operations that extensive exposure is now required to become truly proficient in their use. In fact, an associate with the broadest exposure to a particular software package is always an important source of information for those just starting out. The help that such an associate can initially provide is often invaluable in the time and effort it can save. But always keep in mind that at one time that local expert also had to pick his or her way through the provided manuals and sources of help to get a task done. Becoming proficient in the use of any software package is simply the end result of many hours of exposure, with the ability to ask questions and seek help when needed.

In this text, three software packages will be used extensively. However, the coverage is very introductory in nature, so the guidance provided by this text and the software manuals should be more than enough to enable readers to clearly understand the examples and work through the exercises. Mathcad will be introduced to provide an awareness of the type of available mathematical assistance that extends well beyond the capability of the typical scientific calculator. Although the Mathcad 11 package appearing in Fig. 1.56 is used in this text, the level of coverage is such that all the operations can be accomplished with older versions of Mathcad. For the networks to be explored in this text, two software packages were employed: PSpice and Multisim. A photograph of the PSpice OrCAD Capture 9.2–Lite Edition appears in Fig. 1.57 in the CD-ROM format. A more sophisticated version, referred to simply as SPICE, has widespread application in industry. The package for Version 7 of Multisim appears in Fig. 1.58. Again, the coverage of this text is such that older versions can also be used to complete the exercises. For all the software packages, an effort was made to provide sufficient detail in the text to take the reader through each step in the analysis process. If questions do arise, first consult with your instructor and the software manuals, and as a last resort use the help-line provided with each package.

PSpice Windows

Readers familiar with the older versions of PSpice such as version 8 will find that the major changes in this latest 9.2 version are primarily in the front end and the simulation process.

After executing a few programs, you will find that most of the procedures you learned from older versions will be applicable here also—at least the sequential process has a number of strong similarities. The introduction in this text is to the **Orcad Family Release 9.2 Lite Edition**.

Once the CD has been installed and selected, the PSpice screen will appear. The first step is to establish a **folder** for the storage of the various networks to be analyzed. This is accomplished by first placing the cursor on the Start pad at the bottom left of the screen and performing a right click of the mouse. Then use the sequence **File-New-Folder** to obtain a new folder on the screen, waiting for a label. Type in **PSpice** (the author's choice) followed by a left click of the mouse to install. Then exit the **Exploring-Start** dialog box, and the first step is complete. The folder PSpice has been established for all the projects you plan to work on in this text.

In the next chapter the procedure for labeling the network will be introduced along with the construction of the network. Finally, an analysis will be performed and compared to a handwritten solution to verify the results.

Multisim

Fortunately, there are a number of similarities between PSpice and Multisim. Of course, there are also an extensive number of differences, but the point is that once you become proficient in the use of one software package, the other will be much easier to learn.

Once the Multisim icon is chosen, the screen of Fig. 1.59 will appear. At first, the menu bars seem quite extensive. In fact, simply familiarizing yourself with the range of options already available can take some time. Keep in mind, however, that for each item on a menu bar there is probably a subset that can be chosen, so the list of options is quite extensive. First note at the top of the screen that the menu bar (second row of options) has been broken up into six distinct sections. The **system toolbar**, which includes the first four sections starting from the left, should be somewhat familiar from other software packages such as Microsoft Word. The remaining set of eight pads, called the **Multisim design bar**, is specifically designed for Multisim. Each will be described in detail as the need arises. The vertical toolbars to the left of the screen are an extensive list of components to choose from.

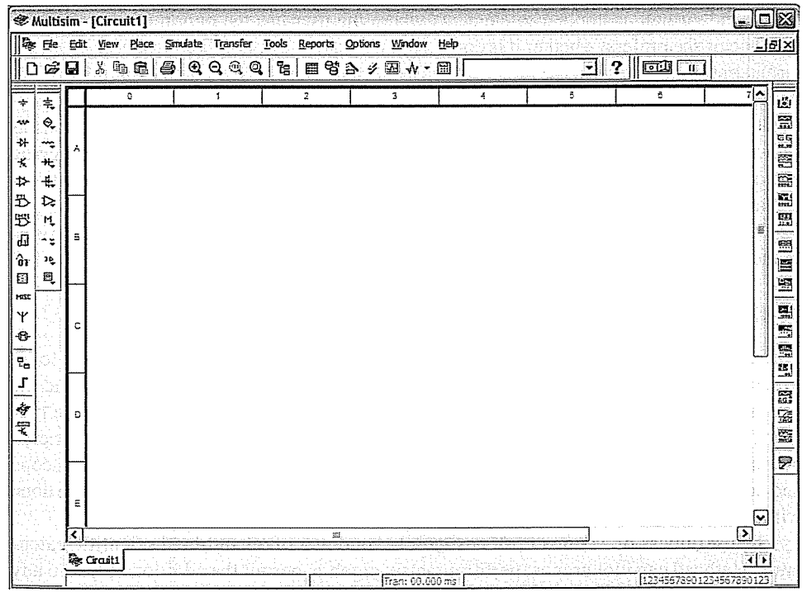


FIG. 1.59
Basic Multisim screen.

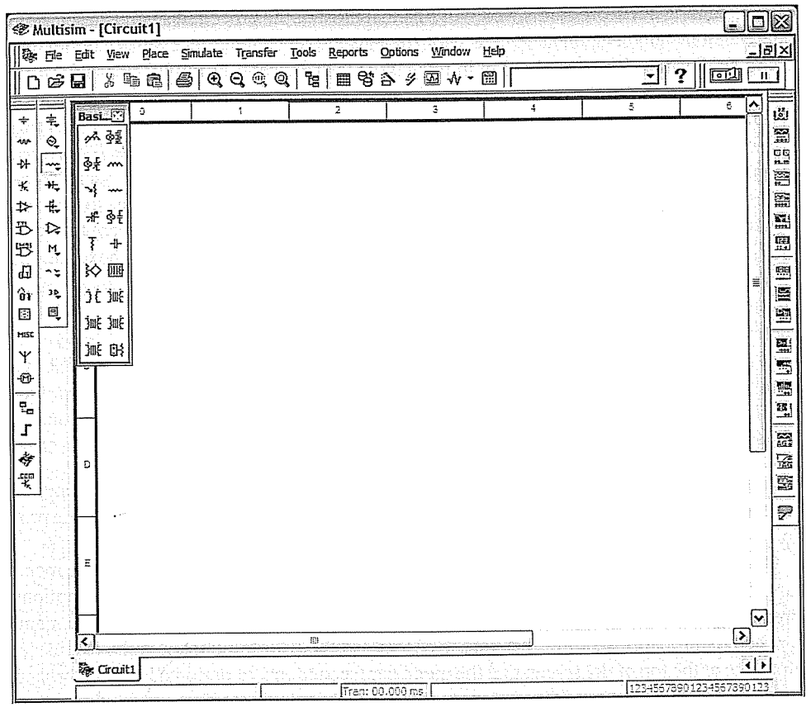


FIG. 1.60
Multisim component family toolbar.

When you enter Multisim you have the choice of using "real" components or "virtual" components. The term "real" is applied to standard values available on a commercial basis. The term "virtual" is applied to elements where the user has the option of choosing any value he or she prefers, whether it is commercially available or not. For most of this text the virtual option will be used the most frequently because it is the less complex of the two options. Selecting the third pad down on the right vertical toolbar of Fig. 1.59 (looks like a resistor symbol) will result in the **BASIC COMPONENTS** dialog box with 18 options as shown in Fig. 1.60. The appearance of this dialog box can be changed by simply dragging one of the edges to establish the desired shape. In the next chapter the details of how to select and place an element from this list are described in detail.

The remaining options of the Multisim design bar will be described as the need arises. In the next chapter a simple circuit will be constructed and tested.

Mathcad

Throughout the text a mathematical software package called **Mathcad®** will be used to introduce the student to the variety of operations this popular package can perform and the advantages associated with its use. There is no need to obtain a copy of the software program unless you feel inclined to learn and use it after this brief introduction. In general, however, the coverage is only at the very introductory level to simply introduce the scope and power of the package. All the exercises appearing at the end of each chapter can be done without resorting to Mathcad.

The usefulness of Mathcad extends well beyond that of a hand-held scientific calculator. Mathcad can plot graphs, perform matrix algebra, permit the addition of text to any calculation, communicate with other data sources such as Excel® and MATLAB® or the Internet, store data, store information, and so on—the list is quite extensive and impressive. The more you learn about the package, the more uses you will find for it on a daily basis.

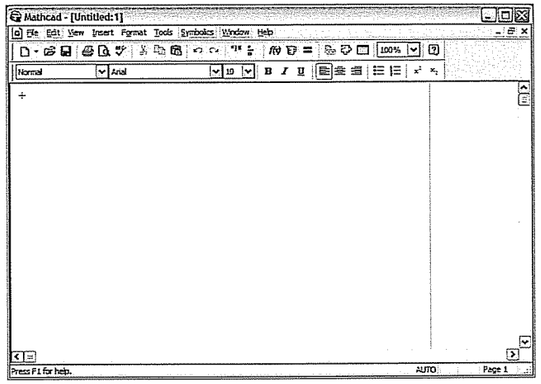


FIG. 1.61
Basic Mathcad screen.

Once the package is installed, all operations begin with the basic screen of Fig. 1.61; labels have been added to this screen to identify the components of the display. In general, all the mathematical operations are performed in specific sequence such as shown in Fig. 1.62, that is, from left to right and then from top to bottom. For example, if line 2 is to operate on a variable, the value of the variable must be defined to the left on the same line or on line 1. Note that Mathcad is very sensitive to this order of things. For example, if you define a series of quantities on the same line but place one a little bit higher than the others, it will not be recognized by the other variables if it happens to be part of their definition. In other words, when writing on the same line, be absolutely sure that you stay on that same line for each new entry. Fortunately, Mathcad is well equipped to tell you when something is wrong. When you first use the program, you will get tired of seeing things in red, indicating that something was not entered or defined correctly. But, in time, as with any learning process, you will become quite comfortable with the software.

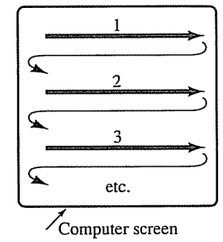


FIG. 1.62
Defining the order of mathematical operations for Mathcad.

To perform basic arithmetic operations, simply click on the screen **at any point** to establish a crosshair on the display (the location of the first entry). If you decide you don't like the location, simply move the arrow to another location, and a simple click will move the crosshair. Then type in the mathematical operation $20 - 2 \times 8/6$ as shown in Fig. 1.63. The instant the equal sign is typed, the result will appear as shown in Fig. 1.63. The equal sign can come from the keyboard or the menu bar at the top of the screen. In fact, by going

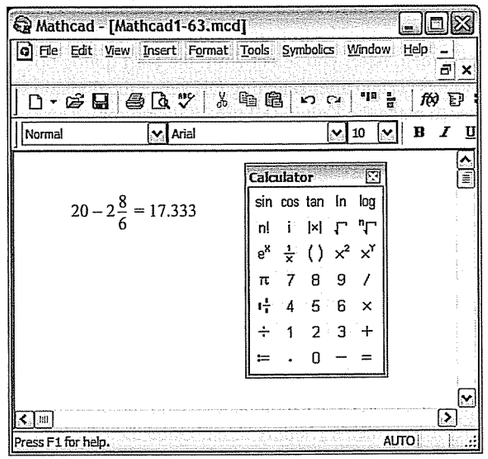


FIG. 1.63
Basic mathematical operation.

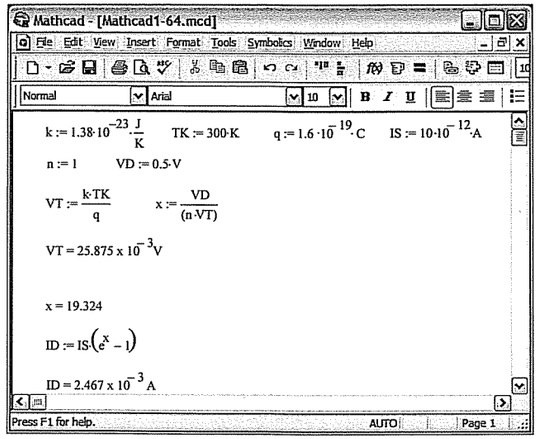


FIG. 1.64
Determining the diode current I_D with $V_D = 0.5$ V.

to **View-Tool bars-Calculator**, you can use the calculator in Fig. 1.63 and enter the entire expression and get the result using the mouse in the same way you use your finger on a typical calculator. All the other mathematical operations such as powers, square roots, sine, tangent, and so on, found in a typical scientific calculator are also available.

For practice using variables, let us calculate the current of a diode using Eq. (1.1). For equations with variables, the letter or symbol applied to the variable is first typed as shown in Fig. 1.64 followed by a colon sign. When the colon sign is entered, an equal sign will also appear as shown in the same figure. The value of the constant for the first series of calculations can then be entered. Next, enter the remaining constants on the same line, and continue by calculating additional variables on the second line that are a function of those on the first two lines. Note that **x** requires that **k**, **TK**, **q**, **IS**, **n**, and **VD** first be defined on the previous lines or to the left on the same line. On the next line the value of **x** can be found by simply typing **x** followed by an equal sign. The multiplication process between constants and their units and between variables in an equation is obtained using the star (*) key (above the number 8) on the keyboard. It will appear as a dot when entering the data or equation but appear as a x in the solution. For numbers with powers of 10, the superscript (^) key (above the number 6) on the keyboard is used to enter the power of 10. Throughout the process of entering data and equations the arrow keys of the keyboard (normally in the bottom right) control where the entered piece of data will appear. The units for each are obtained by first selecting the multiplication operation followed by the **Insert** option appearing at the head of the screen. After you select **Unit**, the **Unit** dialog box will appear. For the constant *k* first find Joules (J) and after selecting OK select the division sign on the keyboard and repeat the process to place the Kelvin (K) unit at the bottom. The result will be the units appearing in Fig. 1.64 for the constant *k*. **It is important to realize that a result will only have the proper unit of measurement if all the units are entered for each quantity in the equation.** The computer will check that all the units were properly entered and in fact will display the units obtained through its internal checking process. If the entries are correct, the result will have the correct units. Note in Fig. 1.64 that the units are in amperes as required. Note also, however, that the powers of 10 are written in long form rather than the abbreviated form using mA. The units associated with the constants can be entered using prefixes before ampere such as m, k, M, and so on, but the results will always display the corresponding power of 10.

The correct response of 19.324 will appear immediately. Now Eq. (1.1) must be entered. As you enter each quantity, a bracket will appear around the quantity defining the quantity to be entered. In time, it becomes a friendly asset. Once the equation is correctly entered, **ID** can be written on the next line (or to the right of the equation), and the result of 2.467 mA will appear directly after the equal sign is selected. The result is that for a voltage of 0.5 V the current for this diode is 2.467 mA.

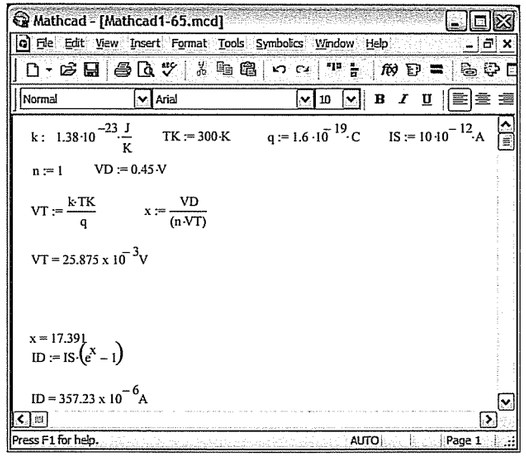


FIG. 1.65
Demonstrating the effect of changing the parameter V_D.

The beauty of Mathcad can now be effectively demonstrated by simply changing the voltage **VD** to 0.45 V. The instant the value is changed, the new level of **x** and **ID** will appear as shown in Fig. 1.65. A reduction in **VD** has reduced the diode current to 0.357 mA. There is no need to enter the entire sequence of calculations again or to calculate all the quantities over again with a calculator. The results appear immediately.

Additional examples using Mathcad will appear throughout the text, but keep in mind that it is not necessary to become proficient in its use to grasp the material of this text—our purpose is simply to introduce the available software.

PROBLEMS

**Note:* Asterisks indicate more difficult problems.

1.3 Covalent Bonding and Intrinsic Materials

1. Sketch the atomic structure of copper and discuss why it is a good conductor and how its structure is different from that of germanium, silicon, and gallium arsenide.
2. In your own words, define an intrinsic material, a negative temperature coefficient, and covalent bonding.
3. Consult your reference library and list three materials that have a negative temperature coefficient and three that have a positive temperature coefficient.

1.4 Energy Levels

4. How much energy in joules is required to move a charge of 6 C through a difference in potential of 3 V?
5. If 48 eV of energy is required to move a charge through a potential difference of 12 V, determine the charge involved.
6. Consult your reference library and determine the level of E_g for GaP and ZnS, two semiconductor materials of practical value. In addition, determine the written name for each material.

1.5 Extrinsic Materials: *n*-Type and *p*-Type Materials

7. Describe the difference between *n*-type and *p*-type semiconductor materials.
8. Describe the difference between donor and acceptor impurities.
9. Describe the difference between majority and minority carriers.
10. Sketch the atomic structure of silicon and insert an impurity of arsenic as demonstrated for silicon in Fig. 1.7.
11. Repeat Problem 10, but insert an impurity of indium.

12. Consult your reference library and find another explanation of hole versus electron flow. Using both descriptions, describe in your own words the process of hole conduction.

1.6 Semiconductor Diode

13. Describe in your own words the conditions established by forward- and reverse-bias conditions on a *p–n* junction diode and how the resulting current is affected.
14. Describe how you will remember the forward- and reverse-bias states of the *p–n* junction diode. That is, how you will remember which potential (positive or negative) is applied to which terminal?
15. Using Eq. (1.1), determine the diode current at 20°C for a silicon diode with $I_s = 50$ nA and an applied forward bias of 0.6 V.
16. Repeat Problem 15 for $T = 100$°C (boiling point of water). Assume that I_s has increased to 5.0 μA.
17. **a.** Using Eq. (1.1), determine the diode current at 20°C for a silicon diode with $I_s = 0.1$ μA at a reverse-bias potential of -10 V.
    b. Is the result expected? Why?
18. **a.** Plot the function $y = e^x$ for x from 0 to 10. Why is it difficult to plot?
    b. What is the value of $y = e^x$ at $x = 0$?
    c. Based on the results of part (b), why is the factor -1 important in Eq. (1.1)?
19. In the reverse-bias region the saturation current of a silicon diode is about 0.1 μA ($T = 20$°C). Determine its approximate value if the temperature is increased 40°C.
20. Compare the characteristics of a silicon and a germanium diode and determine which you would prefer to use for most practical applications. Give some details. Refer to a manufacturer's listing and compare the characteristics of a germanium and a silicon diode of similar maximum ratings.
21. Determine the forward voltage drop across the diode whose characteristics appear in Fig. 1.19 at temperatures of -75°C, 25°C, 100°C, and 200°C and a current of 10 mA. For each temperature, determine the level of saturation current. Compare the extremes of each and comment on the ratio of the two.

1.7 Ideal versus Practical

22. Describe in your own words the meaning of the word *ideal* as applied to a device or a system.
23. Describe in your own words the characteristics of the *ideal* diode and how they determine the on and off states of the device. That is, describe why the short-circuit and open-circuit equivalents are appropriate.
24. What is the one important difference between the characteristics of a simple switch and those of an ideal diode?

1.8 Resistance Levels

25. Determine the static or dc resistance of the commercially available diode of Fig. 1.15 at a forward current of 2 mA.
26. Repeat Problem 25 at a forward current of 15 mA and compare results.
27. Determine the static or dc resistance of the commercially available diode of Fig. 1.15 at a reverse voltage of -10 V. How does it compare to the value determined at a reverse voltage of -30 V?
28. **a.** Determine the dynamic (ac) resistance of the diode of Fig. 1.27 at a forward current of 10 mA using Eq. (1.4).
    b. Determine the dynamic (ac) resistance of the diode of Fig. 1.27 at a forward current of 10 mA using Eq. (1.5).
    c. Compare solutions of parts (a) and (b).
29. Calculate the dc and ac resistances for the diode of Fig. 1.27 at a forward current of 10 mA and compare their magnitudes.
30. Using Eq. (1.4), determine the ac resistance at a current of 1 mA and 15 mA for the diode of Fig. 1.27. Compare the solutions and develop a general conclusion regarding the ac resistance and increasing levels of diode current.
31. Using Eq. (1.5), determine the ac resistance at a current of 1 mA and 15 mA for the diode of Fig. 1.15. Modify the equation as necessary for low levels of diode current. Compare to the solutions obtained in Problem 30.
32. Determine the average ac resistance for the diode of Fig. 1.15 for the region between 0.6 V and 0.9 V.
33. Determine the ac resistance for the diode of Fig. 1.15 at 0.75 V and compare it to the average ac resistance obtained in Problem 32.

1.9 Diode Equivalent Circuits

34. Find the piecewise-linear equivalent circuit for the diode of Fig. 1.15. Use a straight-line segment that intersects the horizontal axis at 0.7 V and best approximates the curve for the region greater than 0.7 V.
35. Repeat Problem 34 for the diode of Fig. 1.27.

1.10 Transition and Diffusion Capacitance

*36. **a.** Referring to Fig. 1.33, determine the transition capacitance at reverse-bias potentials of -25 V and -10 V. What is the ratio of the change in capacitance to the change in voltage?
    b. Repeat part (a) for reverse-bias potentials of -10 V and -1 V. Determine the ratio of the change in capacitance to the change in voltage.
    c. How do the ratios determined in parts (a) and (b) compare? What does this tell you about which range may have more areas of practical application?
37. Referring to Fig. 1.33, determine the diffusion capacitance at 0 V and 0.25 V.
38. Describe in your own words how diffusion and transition capacitances differ.
39. Determine the reactance offered by a diode described by the characteristics of Fig. 1.33 at a forward potential of 0.2 V and a reverse potential of -20 V if the applied frequency is 6 MHz.

1.11 Reverse Recovery Time

40. Sketch the waveform for i of the network of Fig. 1.66 if $t_t = 2t_s$ and the total reverse recovery time is 9 ns.

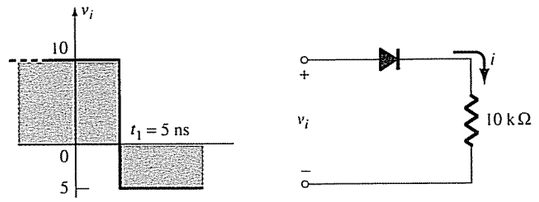


FIG. 1.66
Problem 40.

1.12 Diode Specification Sheets

*41. Plot I_F versus V_F using linear scales for the diode of Fig. 1.37. Note that the provided graph employs a log scale for the vertical axis (log scales are covered in Sections 9.2 and 9.3).
42. Comment on the change in capacitance level with increase in reverse-bias potential for the diode of Fig. 1.37.
43. Does the reverse saturation current of the diode of Fig. 1.37 change significantly in magnitude for reverse-bias potentials in the range -25 V to -100 V?
*44. For the diode of Fig. 1.37 determine the level of I_R at room temperature (25°C) and the boiling point of water (100°C). Is the change significant? Does the level just about double for every 10°C increase in temperature?
45. For the diode of Fig. 1.37, determine the maximum ac (dynamic) resistance at a forward current of 0.1, 1.5, and 20 mA. Compare levels and comment on whether the results support conclusions derived in earlier sections of this chapter.
46. Using the characteristics of Fig. 1.37, determine the maximum power dissipation levels for the diode at room temperature (25°C) and 100°C. Assuming that V_F remains fixed at 0.7 V, how has the maximum level of I_F changed between the two temperature levels?
47. Using the characteristics of Fig. 1.37, determine the temperature at which the diode current will be 50% of its value at room temperature (25°C).

1.15 Zener Diodes

48. The following characteristics are specified for a particular Zener diode: $V_Z = 29$ V, $V_R = 16.8$ V, $I_{ZT} = 10$ mA, $I_R = 20$ μA, and $I_{ZM} = 40$ mA. Sketch the characteristic curve in the manner displayed in Fig. 1.47.

*49. At what temperature will the 10-V Zener diode of Fig. 1.47 have a nominal voltage of 10.75 V? (*Hint*: Note the data in Table 1.7.)

50. Determine the temperature coefficient of a 5-V Zener diode (rated 25°C value) if the nominal voltage drops to 4.8 V at a temperature of 100°C.

51. Using the curves of Fig. 1.48a, what level of temperature coefficient would you expect for a 20-V diode? Repeat for a 5-V diode. Assume a linear scale between nominal voltage levels and a current level of 0.1 mA.

52. Determine the dynamic impedance for the 24-V diode at $I_Z = 10$ mA for Fig. 1.48b. Note that it is a log scale.

*53. Compare the levels of dynamic impedance for the 24-V diode of Fig. 1.48b at current levels of 0.2, 1, and 10 mA. How do the results relate to the shape of the characteristics in this region?

1.16 Light-Emitting Diodes

54. Referring to Fig. 1.53e, what would appear to be an appropriate value of V_K for this device? How does it compare to the value of V_K for silicon and germanium?

55. Using the information provided in Fig. 1.53, determine the forward voltage across the diode if the relative luminous intensity is l.5.

*56. a. What is the percentage increase in relative efficiency of the device of Fig. 1.53 if the peak current is increased from 5 mA to 10 mA?
b. Repeat part (a) for 30 mA to 35 mA (the same increase in current).
c. Compare the percentage increase from parts (a) and (b). At what point on the curve would you say there is little to be gained by further increasing the peak current?

57. a. If the luminous intensity at 0° angular displacement is 3.0 mcd for the device of Fig. 1.53, at what angle will it be 0.75 mcd?
b. At what angle does the loss of luminous intensity drop below the 50% level?

*58. Sketch the current derating curve for the average forward current of the high-efficiency red LED of Fig. 1.53 as determined by temperature. (Note the absolute maximum ratings.)

2 Diode Applications

CHAPTER OUTLINE

2.1 Introduction
2.2 Load-Line Analysis
2.3 Series Diode Configurations
2.4 Parallel and Series–Parallel Configurations
2.5 AND/OR Gates
2.6 Sinusoidal Inputs; Half-Wave Rectification
2.7 Full-Wave Rectification
2.8 Clippers
2.9 Clampers
2.10 Zener Diodes
2.11 Voltage-Multiplier Circuits
2.12 Practical Applications
2.13 Summary
2.14 Computer Analysis

2.1 INTRODUCTION

The construction, characteristics, and models of semiconductor diodes were introduced in Chapter 1. The primary goal of this chapter is to develop a working knowledge of the diode in a variety of configurations using models appropriate for the area of application. By chapter's end, the fundamental behavior pattern of diodes in dc and ac networks should be clearly understood. The concepts learned in this chapter will have significant carryover in the chapters to follow. For instance, diodes are frequently employed in the description of the basic construction of transistors and in the analysis of transistor networks in the dc and ac domains.

This chapter demonstrates an interesting and very useful aspect of the study of a field such as electronic devices and systems:

Once the basic behavior of a device is understood, its function and response in an infinite variety of configurations can be examined.

In other words, now that we have a basic knowledge of the characteristics of a diode along with its response to applied voltages and currents, we can use this knowledge to examine a wide variety of networks. There is no need to reexamine the response of the device for each application.

In general:

The analysis of electronic circuits can follow one of two paths: using the actual characteristics or applying an approximate model for the device.

For the diode the initial discussion will include the actual characteristics to clearly demonstrate how the characteristics of a device and the network parameters interact. Once there is confidence in the results obtained, the approximate piecewise model will be employed to verify the results found using the complete characteristics. It is important that the role and the response of various elements of an electronic system be understood without continually having to resort to lengthy mathematical procedures. This is usually accomplished through the approximation process, which can develop into an art itself. Although the results obtained using the actual characteristics may be slightly different from those obtained using a series of approximations, keep in mind that the characteristics obtained from a specification sheet may be slightly different from those of the device in actual use. In other words, for example, the characteristics of a 1N4001 semiconductor diode may vary from one element to the next in the same lot. The variation may be slight, but it will often be sufficient to justify the approximations employed in the analysis. Also consider the other elements of the network: Is the resistor labeled 100 Ω exactly 100 Ω? Is the applied voltage exactly 10 V or perhaps 10.08 V? All these tolerances contribute to the general belief that a response determined through an appropriate set of approximations can often be "as accurate" as one that employs the full characteristics. In this book the emphasis is toward developing a working knowledge of a device through the use of appropriate approximations, thereby avoiding an unnecessary level of mathematical complexity. Sufficient detail will normally be provided, however, to permit a detailed mathematical analysis if desired.

2.2 LOAD-LINE ANALYSIS

The circuit of Fig. 2.1 is the simplest of diode configurations. It will be used to describe the analysis of a diode circuit using its actual characteristics. In the next section we will replace the characteristics by an approximate model for the diode and compare solutions. Solving the circuit of Fig. 2.1 is all about finding the current and voltage levels that will satisfy both the characteristics of the diode and the chosen network parameters at the same time.

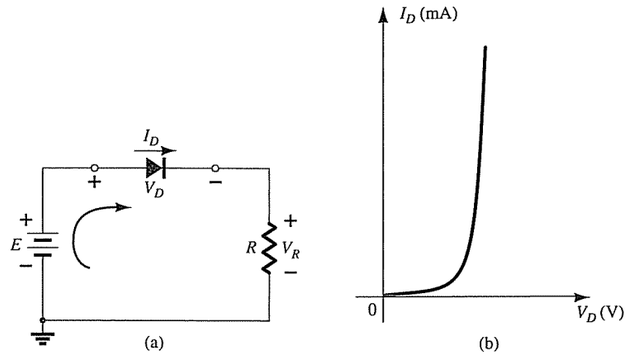


FIG. 2.1
Series diode configuration: (a) circuit; (b) characteristics.

In Fig. 2.2 the diode characteristics are placed on the same set of axes as a straight line defined by the parameters of the network. The straight line is called a *load line* because the intersection on the vertical axis is defined by the applied load R. The analysis to follow is therefore called *load-line analysis*. The intersection of the two curves will define the solution for the network and define the current and voltage levels for the network.

Before reviewing the details of drawing the load line on the characteristics, we need to determine the expected response of the simple circuit of Fig. 2.1. Note in Fig. 2.1 that the effect of the "pressure" established by the dc supply is to establish a conventional current

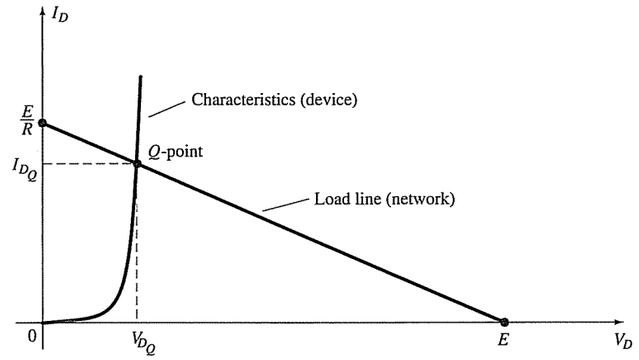


FIG. 2.2
Drawing the load line and finding the point of operation.

in the direction indicated by the clockwise arrow. The fact that the direction of this current has the same direction as the arrow in the diode symbol reveals that the diode is in the "on" state and will conduct a high level of current. In other words, the applied voltage has resulted in a forward-bias situation. With the current direction established, the polarities for the voltage across the diode and resistor can be superimposed. The polarity of V_D and the direction of I_D clearly reveal that the diode is indeed in the forward-bias state, resulting in a voltage across the diode in the neighborhood of 0.7 V and a current on the order of 10 mA or more.

The intersections of the load line on the characteristics of Fig. 2.2 can be determined by first applying Kirchhoff's voltage law in the clockwise direction, which results in

$$+E - V_D - V_R = 0$$

or

$$\boxed{E = V_D + I_D R} \tag{2.1}$$

The two variables of Eq. (2.1), V_D and I_D, are the same as the diode axis variables of Fig. 2.2. This similarity permits plotting Eq. (2.1) on the same characteristics of Fig. 2.2.

The intersections of the load line on the characteristics can easily be determined if one simply employs the fact that anywhere on the horizontal axis $I_D = 0$ A and anywhere on the vertical axis $V_D = 0$ V.

If we *set* $V_D = 0$ V in Eq. (2.1) and solve for I_D, we have the magnitude of I_D *on* the vertical axis. Therefore, with $V_D = 0$ V, Eq. (2.1) becomes

$$\begin{aligned} E &= V_D + I_D R \\ &= 0\,\text{V} + I_D R \end{aligned}$$

and

$$\boxed{I_D = \left.\frac{E}{R}\right|_{V_D = 0\,\text{V}}} \tag{2.2}$$

as shown in Fig. 2.2. If we *set* $I_D = 0$ A in Eq. (2.1) and solve for V_D, we have the magnitude of V_D *on* the horizontal axis. Therefore, with $I_D = 0$ A, Eq. (2.1) becomes

$$\begin{aligned} E &= V_D + I_D R \\ &= V_D + (0\,\text{A})R \end{aligned}$$

and

$$\boxed{V_D = E\big|_{I_D = 0\,\text{A}}} \tag{2.3}$$

as shown in Fig. 2.2. A straight line drawn between the two points will define the load line as depicted in Fig. 2.2. Change the level of R (the load) and the intersection on the vertical axis will change. The result will be a change in the slope of the load line and a different point of intersection between the load line and the device characteristics.

We now have a load line defined by the network and a characteristic curve defined by the device. The point of intersection between the two is the point of operation for this circuit.

By simply drawing a line down to the horizontal axis, we can determine the diode voltage V_{D_Q}, whereas a horizontal line from the point of intersection to the vertical axis will provide the level of I_{D_Q}. The current I_D is actually the current through the entire series configuration of Fig. 2.1a. The point of operation is usually called the *quiescent point* (abbreviated "Q-point") to reflect its "still, unmoving" qualities as defined by a dc network.

The solution obtained at the intersection of the two curves is the same as would be obtained by a simultaneous mathematical solution of

$$I_D = \frac{E}{R} - \frac{V_D}{R} \qquad \text{[derived from Eq. (2.1)]}$$

and

$$I_D = I_s(e^{V_D/nV_T} - 1)$$

as demonstrated later in this section in a Mathcad example. Since the curve for a diode has nonlinear characteristics, the mathematics involved would require the use of nonlinear techniques that are beyond the needs and scope of this book. The load-line analysis described above provides a solution with a minimum of effort and a "pictorial" description of why the levels of solution for V_{D_Q} and I_{D_Q} were obtained. The next example demonstrates the techniques introduced above and reveals the relative ease with which the load line can be drawn using Eqs. (2.2) and (2.3).

Multisim PSpice

EXAMPLE 2.1 For the series diode configuration of Fig. 2.3a, employing the diode characteristics of Fig. 2.3b, determine:

a. V_{D_Q} and I_{D_Q}.
b. V_R.

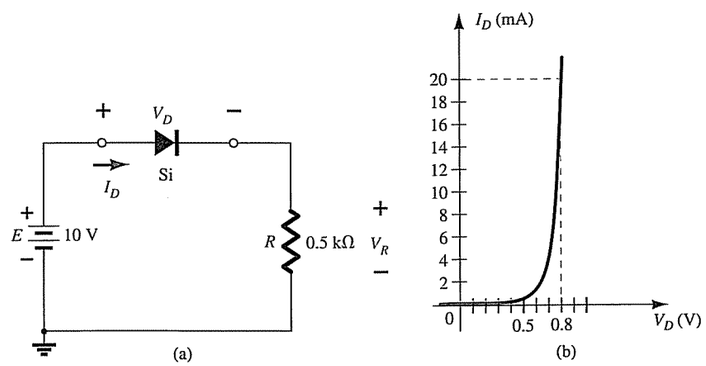


FIG. 2.3
(a) Circuit; (b) characteristics.

Solution:

a. Eq. (2.2): $$I_D = \frac{E}{R}\bigg|_{V_D=0\,\text{V}} = \frac{10\,\text{V}}{0.5\,\text{k}\Omega} = 20\,\text{mA}$$

Eq. (2.3): $$V_D = E|_{I_D=0\,\text{A}} = 10\,\text{V}$$

The resulting load line appears in Fig. 2.4. The intersection between the load line and the characteristic curve defines the Q-point as

$$V_{D_Q} \cong \mathbf{0.78\ V}$$
$$I_{D_Q} \cong \mathbf{18.5\ mA}$$

The level of V_D is certainly an estimate, and the accuracy of I_D is limited by the chosen scale. A higher degree of accuracy would require a plot that would be much larger and perhaps unwieldy.

b. $V_R = I_R R = I_{D_Q} R = (18.5\,\text{mA})(1\,\text{k}\Omega) = \mathbf{18.5\ V}$

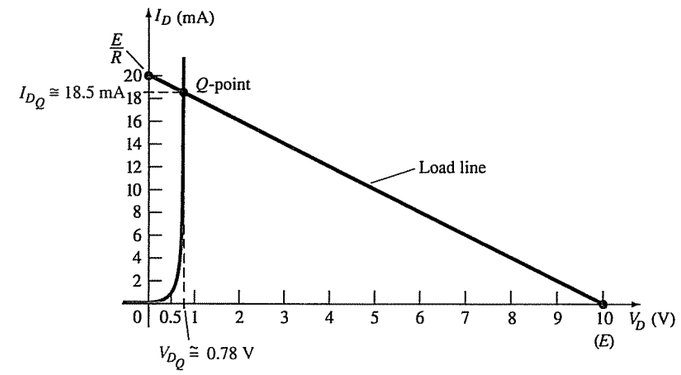


FIG. 2.4
Solution to Example 2.1.

As noted in the example above, the load line is determined solely by the applied network, whereas the characteristics are defined by the chosen device. If we turn to our approximate model for the diode and do not disturb the network, the load line will be exactly the same as obtained in the example above. In fact, the next two examples repeat the analysis of Example 2.1 using the approximate model to permit a comparison of the results.

EXAMPLE 2.2 Repeat Example 2.1 using the approximate equivalent model for the silicon semiconductor diode.

Solution: The load line is redrawn as shown in Fig. 2.5 with the same intersections as defined in Example 2.1. The characteristics of the approximate equivalent circuit for the diode have also been sketched on the same graph. The resulting Q-point is

$$V_{D_Q} = \mathbf{0.7\ V}$$
$$I_{D_Q} = \mathbf{18.5\ mA}$$

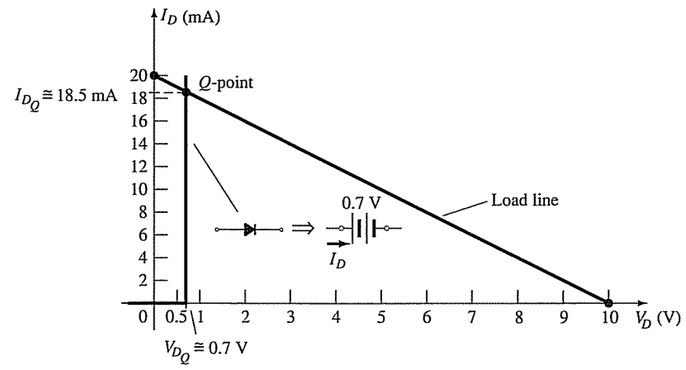


FIG. 2.5
Solution to Example 2.1 using the diode approximate model.

The results obtained in Example 2.2 are quite interesting. The level of I_{D_Q} is exactly the same as obtained in Example 2.1 using a characteristic curve that is a great deal easier to draw than that appearing in Fig. 2.4. The $V_D = 0.7$ V here and the 0.78 V from Example 2.1 are of a different magnitude to the hundredths place, but they are certainly in the same neighborhood if we compare their magnitudes to the magnitudes of the other voltages of the network.

In the next example we go a step further and substitute the ideal model. The results will reveal the conditions that must be satisfied to apply the ideal equivalent properly.

EXAMPLE 2.3 Repeat Example 2.1 using the ideal diode model.

Solution: As shown in Fig. 2.6, the load line is the same, but the ideal characteristics now intersect the load line on the vertical axis. The *Q*-point is therefore defined by

$$V_{D_Q} = \mathbf{0\ V}$$
$$I_{D_Q} = \mathbf{20\ mA}$$

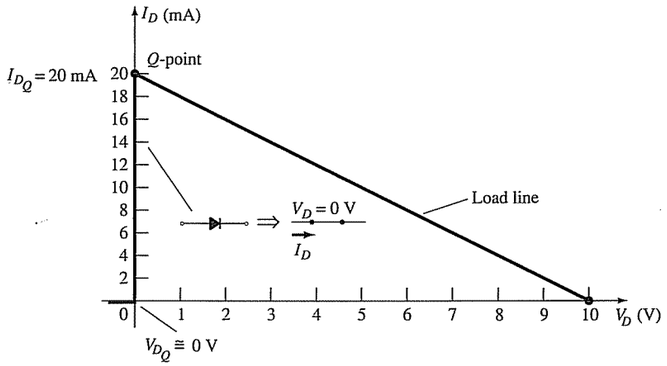


FIG. 2.6
Solution to Example 2.1 using the ideal diode model.

The results are sufficiently different from the solutions of Example 2.1 to cause some concern about their accuracy. Certainly, they do provide some indication of the level of voltage and current to be expected relative to the other voltage levels of the network, but the additional effort of simply including the 0.7-V offset suggests that the approach of Example 2.2 is more appropriate.

Use of the ideal diode model therefore should be reserved for those occasions when the role of a diode is more important than voltage levels that differ by tenths of a volt and in those situations where the applied voltages are considerably larger than the threshold voltage V_K. In the next few sections the approximate model will be employed exclusively since the voltage levels obtained will be sensitive to variations that approach V_K. In later sections the ideal model will be employed more frequently since the applied voltages will frequently be quite a bit larger than V_K and the authors want to ensure that the role of the diode is correctly and clearly understood.

Mathcad

Mathcad will now be used to find the solution of the two simultaneous equations defined by the diode and network of Fig. 2.7.

The diode's characteristics are defined by

$$I_D = I_s(e^{V_D/nV_T} - 1) = 10\,\text{pA}\,(e^{V_D/39.0\,\text{mV}} - 1)$$

In the equation for the diode n was chosen to be 1.5 to establish characteristics that would provide a better match with commercial units. Increasing n has the effect of shifting the characteristics to the right.

Applying Kirchhoff's voltage law around the closed loop, we have

$$E - V_D - V_R = 0 \Rightarrow E - V_D = I_R R \Rightarrow E - V_D = I_D R$$

and solving for the diode current results in

$$I_D = \frac{E - V_D}{R} = \frac{E}{R} - \frac{V_D}{R}$$

$$I_D = \frac{10\ \text{V}}{0.5\ \text{k}\Omega} - \frac{V_D}{0.5\ \text{k}\Omega}$$

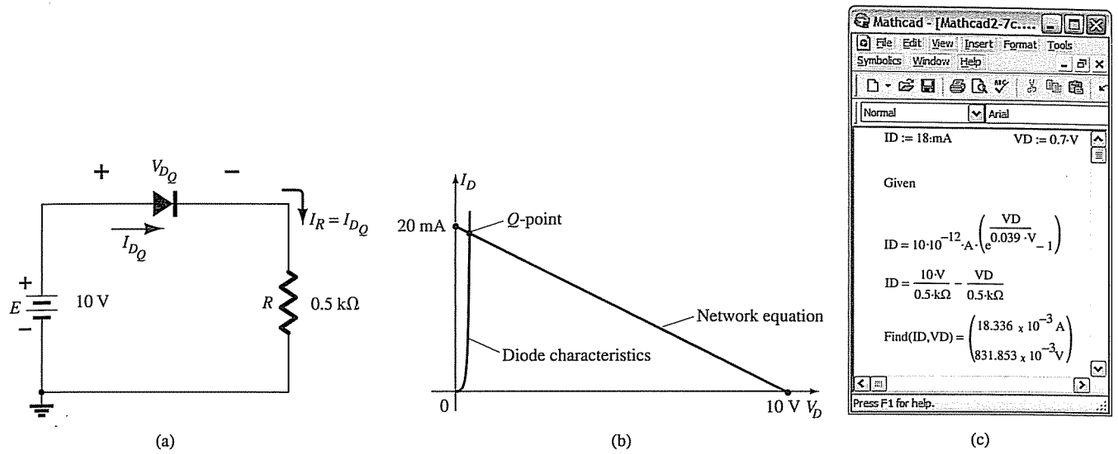


FIG. 2.7
Finding the operating point defined by a diode's characteristics and the network. (a) Network; (b) graphical solution; (c) computer solution.

Since we now have two equations and two unknowns (I_D and V_D), we can solve for each unknown using Mathcad as follows:

When using Mathcad to solve simultaneous equations, you must **guess** a value for each quantity to give the computer some direction in its **iterative process**. In other words, the computer will test solutions and work its way toward the actual solution by responding to the results obtained.

For our situation the initial guesses for **ID** and **VD** were 18 mA and 0.7 V, respectively, as shown on the top of Fig. 2.7c. Then, following the word **Given** (required), the two equations are entered using the equal sign obtained from **Ctrl** = . Note throughout Fig. 2.7c that units are applied to the guess values and to all the equations, a requirement if the results are to have units also. Note, however, that the guess values and the equations can use prefixes, as in mA and kΩ, but the answer will always be in a power-of-10 format. Text, type **Find(ID,VD)** to tell the computer what needs to be determined. Once the equal sign is entered, the results will appear as shown in Fig. 2.7c and as supported by Fig. 2.7b, $I_D = 18.34$ mA and $V_D = 0.83$ V.

2.3 SERIES DIODE CONFIGURATIONS

In the last section we found that the results obtained using the approximate piecewise-linear equivalent model were quite close, if not equal, to the response obtained using the full characteristics. In fact, if one considers all the variations possible due to tolerances, temperature, and so on, one could certainly consider one solution to be "as accurate" as the other. Since the use of the approximate model normally results in a reduced expenditure of time and effort to obtain the desired results, it is the approach that will be employed in this book unless otherwise specified. Recall the following:

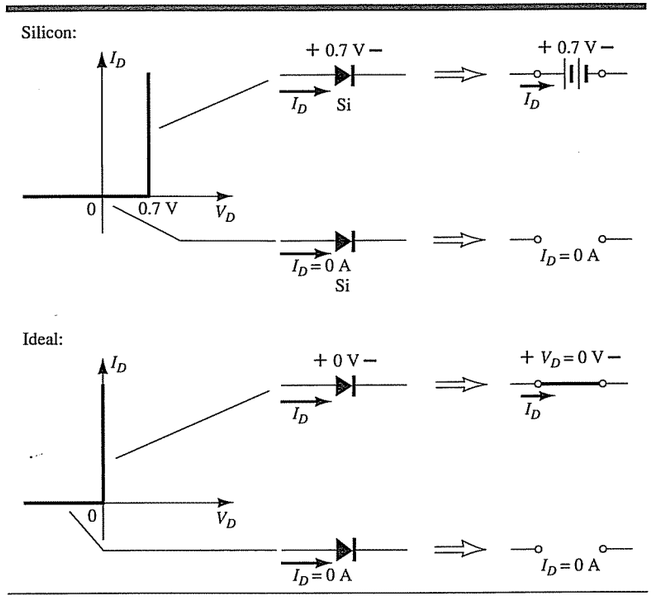
The primary purpose of this text is to develop a general knowledge of the behavior, capabilities, and possible areas of application of a device in a manner that will minimize the need for extensive mathematical developments.

For all the analysis to follow in this chapter it is assumed that

The forward resistance of the diode is usually so small compared to the other series elements of the network that it can be ignored.

This is a valid approximation for the vast majority of applications that employ diodes. Using this fact will result in the approximate equivalents for a silicon diode and an ideal diode that appear in Table 2.1. For the conduction region the only difference between the silicon diode and the ideal diode is the vertical shift in the characteristics, which is accounted for in the equivalent model by a dc supply of 0.7 V opposing the direction of forward current through the device. For voltages less than 0.7 V for a silicon diode and 0 V for the ideal diode the resistance is so high compared to other elements of the network that its equivalent is the open circuit.

TABLE 2.1
Approximate and Ideal Semiconductor Diode Models.



For a Ge diode the offset voltage is 0.3 V and for a GaAs diode it is 1.2 V. Otherwise the equivalent networks are the same. For each diode the label Si, Ge, or GaAs will appear along with the diode symbol. For networks with ideal diodes the diode symbol will appear as shown in Table 2.1 without any labels.

The approximate models will now be used to investigate a number of series diode configurations with dc inputs. This will establish a foundation in diode analysis that will carry over into the sections and chapters to follow. The procedure described can, in fact, be applied to networks with any number of diodes in a variety of configurations.

For each configuration the state of each diode must first be determined. Which diodes are "on" and which are "off"? Once determined, the appropriate equivalent can be substituted and the remaining parameters of the network determined.

In general, a diode is in the "on" state if the current established by the applied sources is such that its direction matches that of the arrow in the diode symbol, and $V_D \geq 0.7$ V for silicon, $V_D \geq 0.3$ V for germanium, and $V_D \geq 1.2$ V for gallium arsenide.

For each configuration, *mentally* replace the diodes with resistive elements and note the resulting current direction as established by the applied voltages ("pressure"). If the resulting direction is a "match" with the arrow in the diode symbol, conduction through the diode will occur and the device is in the "on" state. The description above is, of course, contingent on the supply having a voltage greater than the "turn-on" voltage (V_K) of each diode.

If a diode is in the "on" state, one can either place a 0.7-V drop across the element or redraw the network with the V_K equivalent circuit as defined in Table 2.1. In time the preference will probably simply be to include the 0.7-V drop across each "on" diode and draw a line through each diode in the "off" or open state. Initially, however, the substitution method will be used to ensure that the proper voltage and current levels are determined.

The series circuit of Fig. 2.8 described in some detail in Section 2.2 will be used to demonstrate the approach described in the above paragraphs. The state of the diode is first determined by mentally replacing the diode with a resistive element as shown in Fig. 2.9a. The resulting direction of I is a match with the arrow in the diode symbol, and since $E > V_K$, the diode is in the "on" state. The network is then redrawn as shown in Fig. 2.9b with the appropriate equivalent model for the forward-biased silicon diode. Note for future reference

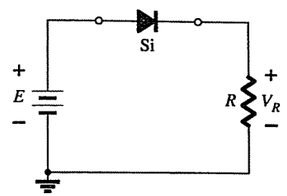


FIG. 2.8
Series diode configuration.

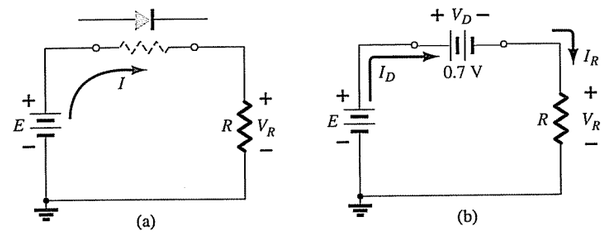


FIG. 2.9
(a) Determining the state of the diode of Fig. 2.8; (b) substituting the equivalent model for the "on" diode of Fig. 2.9a.

that the polarity of V_D is the same as would result if in fact the diode were a resistive element. The resulting voltage and current levels are the following:

$$V_D = V_K \tag{2.4}$$

$$V_R = E - V_K \tag{2.5}$$

$$I_D = I_R = \frac{V_R}{R} \tag{2.6}$$

In Fig. 2.10 the diode of Fig. 2.7 has been reversed. Mentally replacing the diode with a resistive element as shown in Fig. 2.11 will reveal that the resulting current direction does not match the arrow in the diode symbol. The diode is in the "off" state, resulting in the equivalent circuit of Fig. 2.12. Due to the open circuit, the diode current is 0 A and the voltage across the resistor R is the following:

$$V_R = I_R R = I_D R = (0\,\text{A})R = \mathbf{0\,V}$$

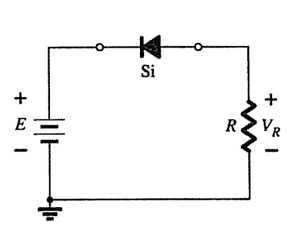


FIG. 2.10
Reversing the diode of Fig. 2.8.

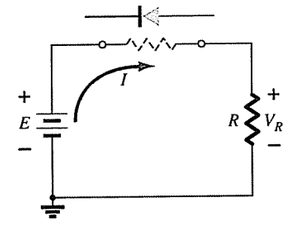


FIG. 2.11
Determining the state of the diode of Fig. 2.10.

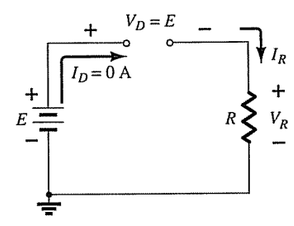


FIG. 2.12
Substituting the equivalent model for the "off" diode of Fig. 2.10.

The fact that $V_R = 0$ V will establish E volts across the open circuit as defined by Kirchhoff's voltage law. Always keep in mind that under any circumstances—dc, ac instantaneous values, pulses, and so on—Kirchhoff's voltage law must be satisfied!

EXAMPLE 2.4 For the series diode configuration of Fig. 2.13, determine V_D, V_R, and I_D.

Solution: Since the applied voltage establishes a current in the clockwise direction to match the arrow of the symbol and the diode is in the "on" state,



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$$V_D = \mathbf{0.7\,V}$$

$$V_R = E - V_D = 8\,\text{V} - 0.7\,\text{V} = \mathbf{7.3\,V}$$

$$I_D = I_R = \frac{V_R}{R} = \frac{7.3\,\text{V}}{2.2\,\text{k}\Omega} \cong \mathbf{3.32\,mA}$$

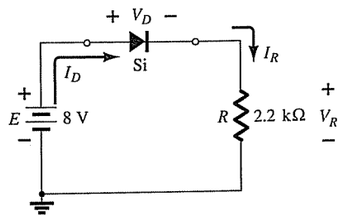


FIG. 2.13
Circuit for Example 2.4.

EXAMPLE 2.5 Repeat Example 2.4 with the diode reversed.

Solution: Removing the diode, we find that the direction of I is opposite to the arrow in the diode symbol and the diode equivalent is the open circuit no matter which model is employed. The result is the network of Fig. 2.14, where $I_D = \mathbf{0\ A}$ due to the open circuit. Since $V_R = I_R R$, we have $V_R = (0)R = \mathbf{0\ V}$. Applying Kirchhoff's voltage law around the closed loop yields

$$E - V_D - V_R = 0$$

and

$$V_D = E - V_R = E - 0 = E = \mathbf{8\ V}$$

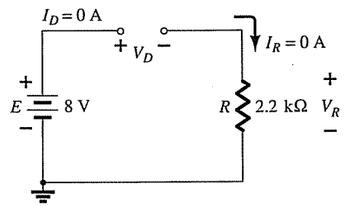


FIG. 2.14
Determining the unknown quantities for Example 2.5.

In particular, note in Example 2.5 the high voltage across the diode even though it is an "off" state. The current is zero, but the voltage is significant. For review purposes, keep the following in mind for the analysis to follow:

An open circuit can have any voltage across its terminals, but the current is always 0 A.

A short circuit has a 0-V drop across its terminals, but the current is limited only by the surrounding network.

In the next example the notation of Fig. 2.15 will be employed for the applied voltage. It is a common industry notation and one with which the reader should become very familiar. Such notation and other defined voltage levels are treated further in Chapter 4.

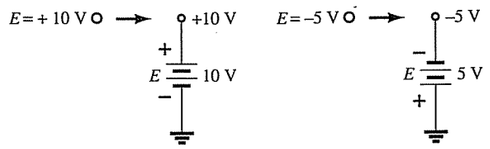


FIG. 2.15
Source notation.

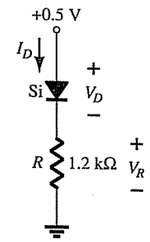


FIG. 2.16
Series diode circuit for Example 2.6.

EXAMPLE 2.6 For the series diode configuration of Fig. 2.16, determine V_D, V_R, and I_D.

Solution: Although the "pressure" establishes a current with the same direction as the arrow symbol, the level of applied voltage is insufficient to turn the silicon diode "on." The point of operation on the characteristics is shown in Fig. 2.17, establishing the open-circuit equivalent as the appropriate approximation, as shown in Fig. 2.18. The resulting voltage and current levels are therefore the following:

$$I_D = \mathbf{0\ A}$$

$$V_R = I_R R = I_D R = (0\ \text{A})\,1.2\,\text{k}\Omega = \mathbf{0\ V}$$

and

$$V_D = E = \mathbf{0.5\ V}$$

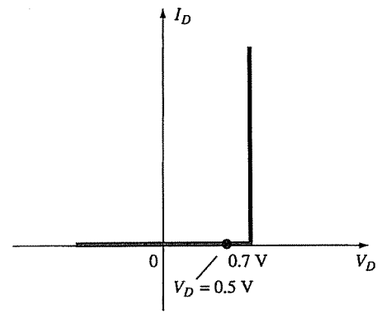


FIG. 2.17
Operating point with $E = 0.5$ V.

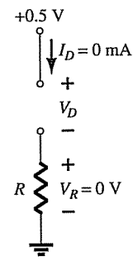


FIG. 2.18
Determining I_D, V_R, and V_D for the circuit of Fig. 2.16.

EXAMPLE 2.7 Determine V_o and I_D for the series circuit of Fig. 2.19.

Solution: An attack similar to that applied in Example 2.4 will reveal that the resulting current has the same direction as the arrowheads of the symbols of both diodes, and the network of Fig. 2.20 results because $E = 12\ \text{V} > (0.7\ \text{V} + 1.8\ \text{V}\ [\text{Table 1.8}]) = 2.5\ \text{V}$. Note the redrawn supply of 12 V and the polarity of V_o across the 680-Ω resistor. The resulting voltage is

$$V_o = E - V_{K_1} - V_{K_2} = 12\ \text{V} - 2.5\ \text{V} = \mathbf{9.5\ V}$$

and

$$I_D = I_R = \frac{V_R}{R} = \frac{V_o}{R} = \frac{9.5\ \text{V}}{680\ \Omega} = \mathbf{13.97\ mA}$$

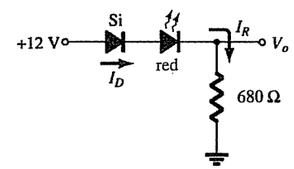


FIG. 2.19
Circuit for Example 2.7.

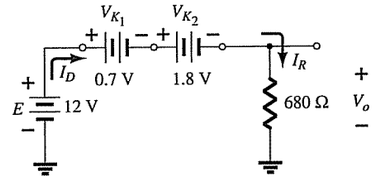


FIG. 2.20
Determining the unknown quantities for Example 2.7.

EXAMPLE 2.8 Determine I_D, V_{D_2}, and V_o for the circuit of Fig. 2.21.

Solution: Removing the diodes and determining the direction of the resulting current I result in the circuit of Fig. 2.22. There is a match in current direction for the silicon diode but not for the germanium diode. The combination of a short circuit in series with an open circuit always results in an open circuit and $I_D = \mathbf{0\ A}$, as shown in Fig. 2.23.

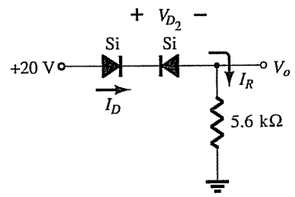


FIG. 2.21
Circuit for Example 2.8.

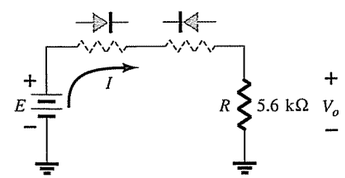


FIG. 2.22
Determining the state of the diodes of Fig. 2.21.

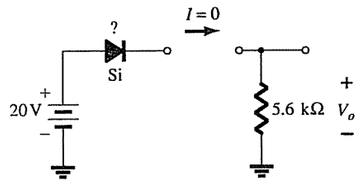


FIG. 2.23
Substituting the equivalent state for the open diode.

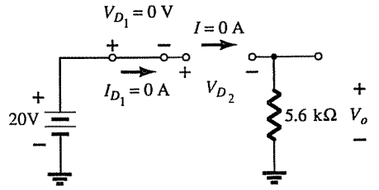


FIG. 2.24
Determining the unknown quantities for the circuit of Example 2.8.

The question remains as to what to substitute for the silicon diode. For the analysis to follow in this and succeeding chapters, simply recall for the actual practical diode that when $I_D = 0$ A, $V_D = 0$ V (and vice versa), as described for the no-bias situation in Chapter 1. The conditions described by $I_D = 0$ A and $V_{D_1} = 0$ V are indicated in Fig. 2.24. We have

$$V_o = I_R R = I_D R = (0\,\text{A})R = \mathbf{0\,V}$$

and

$$V_{D_2} = V_{\text{open circuit}} = E = \mathbf{20\,V}$$

Applying Kirchhoff's voltage law in a clockwise direction gives

$$E - V_{D_1} - V_{D_2} - V_o = 0$$

and

$$V_{D_2} = E - V_{D_1} - V_o = 20\,\text{V} - 0 - 0$$
$$= \mathbf{20\,V}$$

with

$$V_o = \mathbf{0\,V}$$

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EXAMPLE 2.9 Determine I, V_1, V_2, and V_o for the series dc configuration of Fig. 2.25.

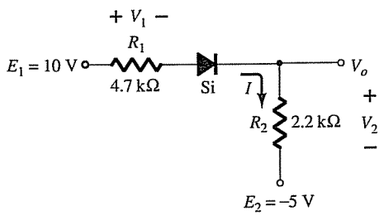


FIG. 2.25
Circuit for Example 2.9.

Solution: The sources are drawn and the current direction indicated as shown in Fig. 2.26. The diode is in the "on" state and the notation appearing in Fig. 2.27 is included to indicate this state. Note that the "on" state is noted simply by the additional $V_D = 0.7$ V on the figure. This eliminates the need to redraw the network and avoids any confusion that may

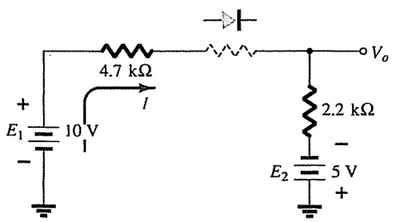


FIG. 2.26
Determining the state of the diode for the network of Fig. 2.25.

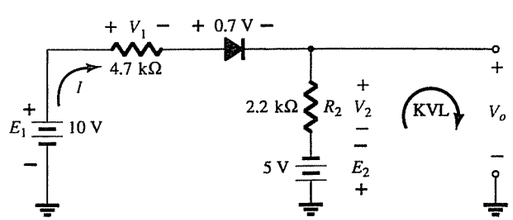


FIG. 2.27
Determining the unknown quantities for the network of Fig. 2.25. KVL, Kirchhoff voltage loop.

result from the appearance of another source. As indicated in the introduction to this section, this is probably the path and notation that one will take when a level of confidence has been established in the analysis of diode configurations. In time the entire analysis will be performed simply by referring to the original network. Recall that a reverse-biased diode can simply be indicated by a line through the device.

The resulting current through the circuit is

$$I = \frac{E_1 + E_2 - V_D}{R_1 + R_2} = \frac{10\,\text{V} + 5\,\text{V} - 0.7\,\text{V}}{4.7\,\text{k}\Omega + 2.2\,\text{k}\Omega} = \frac{14.3\,\text{V}}{6.9\,\text{k}\Omega}$$
$$\cong \mathbf{2.07\,mA}$$

and the voltages are

$$V_1 = IR_1 = (2.07\,\text{mA})(4.7\,\text{k}\Omega) = \mathbf{9.73\,V}$$
$$V_2 = IR_2 = (2.07\,\text{mA})(2.2\,\text{k}\Omega) = \mathbf{4.55\,V}$$

Applying Kirchhoff's voltage law to the output section in the clockwise direction results in

$$-E_2 + V_2 - V_o = 0$$

and

$$V_o = V_2 - E_2 = 4.55\,\text{V} - 5\,\text{V} = \mathbf{-0.45\,V}$$

The minus sign indicates that V_o has a polarity opposite to that appearing in Fig. 2.25.

2.4 PARALLEL AND SERIES–PARALLEL CONFIGURATIONS

The methods applied in Section 2.3 can be extended to the analysis of parallel and series–parallel configurations. For each area of application, simply match the sequential series of steps applied to series diode configurations.

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EXAMPLE 2.10 Determine V_o, I_1, I_{D_1}, and I_{D_2} for the parallel diode configuration of Fig. 2.28.

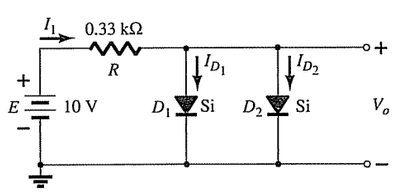


FIG. 2.28
Network for Example 2.10.

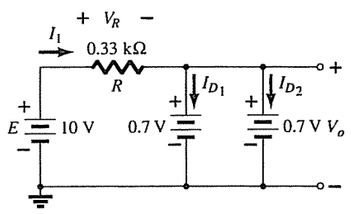


FIG. 2.29
Determining the unknown quantities for the network of Example 2.10.

Solution: For the applied voltage the "pressure" of the source acts to establish a current through each diode in the same direction as shown in Fig. 2.29. Since the resulting current direction matches that of the arrow in each diode symbol and the applied voltage is greater than 0.7 V, both diodes are in the "on" state. The voltage across parallel elements is always the same and

$$V_o = \mathbf{0.7\,V}$$

The current is

$$I_1 = \frac{V_R}{R} = \frac{E - V_D}{R} = \frac{10\,\text{V} - 0.7\,\text{V}}{0.33\,\text{k}\Omega} = \mathbf{28.18\,mA}$$

Assuming diodes of similar characteristics, we have

$$I_{D_1} = I_{D_2} = \frac{I_1}{2} = \frac{28.18\,\text{mA}}{2} = \mathbf{14.09\,mA}$$

This example demonstrates one reason for placing diodes in parallel. If the current rating of the diodes of Fig. 2.28 is only 20 mA, a current of 28.18 mA would damage the device if it appeared alone in Fig. 2.28. By placing two in parallel, we limit the current to a safe value of 14.09 mA with the same terminal voltage.

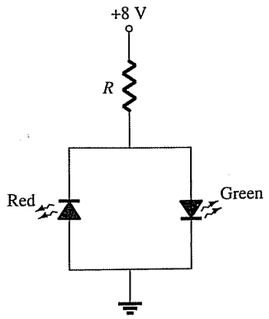


FIG. 2.30
Network for Example 2.11.

EXAMPLE 2.11 In this example there are two LEDs that can be used as a polarity detector. Apply a positive source voltage and a green light results. Negative supplies result in a red light. Packages of such combinations are commercially available.

Find the resistor R to ensure a current of 20 mA through the "on" diode for the configuration of Fig. 2.30. Both diodes have a reverse breakdown voltage of 3 V and an average turn-on voltage of 2 V.

Solution: The application of a positive supply voltage results in a conventional current that matches the arrow of the green diode and turns it on.

The polarity of the voltage across the green diode is such that it reverse biases the red diode by the same amount. The result is the equivalent network of Fig. 2.31.

Applying Ohm's law, we obtain

$$I = 20\,\text{mA} = \frac{E - V_{\text{LED}}}{R} = \frac{8\,\text{V} - 2\,\text{V}}{R}$$

and

$$R = \frac{6\,\text{V}}{20\,\text{mA}} = \mathbf{300\ \Omega}$$

Note that the reverse breakdown voltage across the red diode is 2 V, which is fine for an LED with a reverse breakdown voltage of 3 V.

However, if the green diode were to be replaced by a blue diode, problems would develop, as shown in Fig. 2.32. Recall that the forward bias required to turn on a blue diode is about 5 V. The result would appear to require a smaller resistor R to establish the current of 20 mA. However, note that the reverse bias voltage of the red LED is 5 V, but the reverse breakdown voltage of the diode is only 3 V. The result is the voltage across the red LED would lock in at 3 V as shown in Fig. 2.33. The voltage across R would be 5 V and the current limited to 20 mA with a 250 Ω resistor but neither LED would be on.

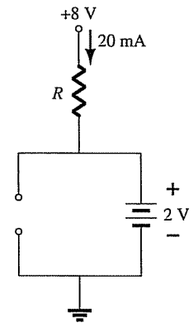


FIG. 2.31
Operating conditions for the network of Fig. 2.30.

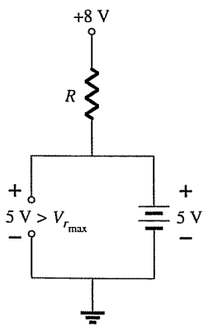


FIG. 2.32
Network of Fig. 2.31 with a blue diode.

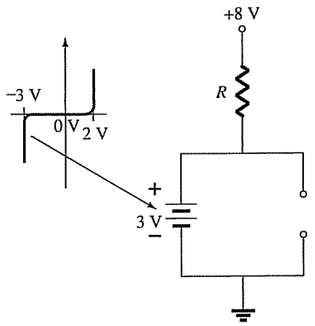


FIG. 2.33
Demonstrating damage to the red LED if the reverse breakdown voltage is exceeded.

A simple solution to the above is to simply add the appropriate resistance level in series with each diode to establish the desired 20 mA and to include another diode to add to the reverse-bias total reverse breakdown voltage rating, as shown in Fig. 2.34. When the blue LED is on, the diode in series with the blue LED will also be on, causing a total voltage drop of 5.7 V across the two series diodes and a voltage of 2.3 V across the resistor R_1, establishing a high emission current of 19.17 mA. At the same time the red LED diode and

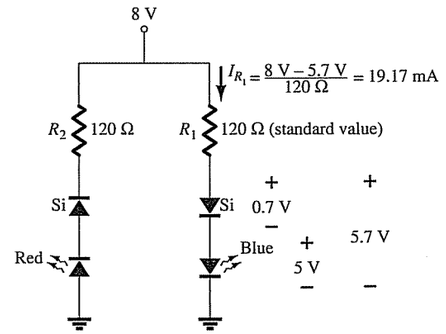


FIG. 2.34
Protective measure for the red LED of Fig. 2.33.

its series diode will also be reverse biased, but now the standard diode with a reverse breakdown voltage of 20 V will prevent the full reverse-bias voltage of 8 V from appearing across the red LED. When forward biased the resistor R_2 will establish a current of 19.63 mA to ensure a high level of intensity for the red LED.

EXAMPLE 2.12 Determine the voltage V_o for the network of Fig. 2.35.

Solution: Initially, it might appear that the applied voltage will turn both diodes "on" because the applied voltage ("pressure") is trying to establish a conventional current through each diode that would suggest the "on" state. However, if both were on, there would be more than one voltage across the parallel diodes, violating one of the basic rules of network analysis: The voltage must be the same across parallel elements.

The resulting action can best be explained by remembering that there is a period of build-up of the supply voltage from 0 V to 12 V even though it may take milliseconds or microseconds. At the instant the increasing supply voltage reaches 0.7 V the silicon diode will turn "on" and maintain the level of 0.7 V since the characteristic is vertical at this voltage—the current of the silicon diode will simply rise to the defined level. The result is that the voltage across the green LED will never rise above 0.7 V and will remain in the equivalent open-circuit state as shown in Fig. 2.36.

The result is

$$V_o = 12\,\text{V} - 0.7\,\text{V} = \mathbf{11.3\ V}$$

FIG. 2.35
Network for Example 2.12.

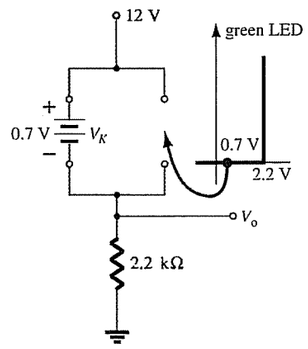


FIG. 2.36
Determining V_o for the network of Fig. 2.35.

EXAMPLE 2.13 Determine the currents I_1, I_2, and I_{D_2} for the network of Fig. 2.37.

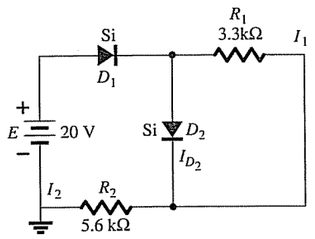


FIG. 2.37
Network for Example 2.13.

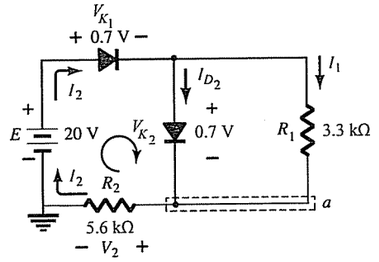


FIG. 2.38
Determining the unknown quantities for Example 2.13.

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Solution: The applied voltage (pressure) is such as to turn both diodes on, as indicated by the resulting current directions in the network of Fig. 2.38. Note the use of the abbreviated notation for "on" diodes and that the solution is obtained through an application of techniques applied to dc series–parallel networks. We have

$$I_1 = \frac{V_{K_2}}{R_1} = \frac{0.7\text{ V}}{3.3\text{ k}\Omega} = \mathbf{0.212\text{ mA}}$$

Applying Kirchhoff's voltage law around the indicated loop in the clockwise direction yields

$$-V_2 + E - V_{K_1} - V_{K_2} = 0$$

and

$$V_2 = E - V_{K_1} - V_{K_2} = 20\text{ V} - 0.7\text{ V} - 0.7\text{ V} = \mathbf{18.6\text{ V}}$$

with

$$I_2 = \frac{V_2}{R_2} = \frac{18.6\text{ V}}{5.6\text{ k}\Omega} = \mathbf{3.32\text{ mA}}$$

At the bottom node a,

$$I_{D_2} + I_1 = I_2$$

and

$$I_{D_2} = I_2 - I_1 = 3.32\text{ mA} - 0.212\text{ mA} \cong \mathbf{3.11\text{ mA}}$$

2.5 AND/OR GATES

The tools of analysis are now at our disposal, and the opportunity to investigate a computer configuration is one that will demonstrate the range of applications of this relatively simple device. Our analysis will be limited to determining the voltage levels and will not include a detailed discussion of Boolean algebra or positive and negative logic.

The network to be analyzed in Example 2.14 is an OR gate for positive logic. That is, the 10-V level of Fig. 2.39 is assigned a "1" for Boolean algebra and the 0-V input is assigned a "0." An OR gate is such that the output voltage level will be a 1 if either *or* both inputs is a 1. The output is a 0 if both inputs are at the 0 level.

The analysis of AND/OR gates is made easier by using the approximate equivalent for a diode rather than the ideal because we can stipulate that the voltage across the diode must be 0.7 V positive for the silicon diode to switch to the "on" state.

In general, the best approach is simply to establish a "gut" feeling for the state of the diodes by noting the direction and the "pressure" established by the applied potentials. The analysis will then verify or negate your initial assumptions.

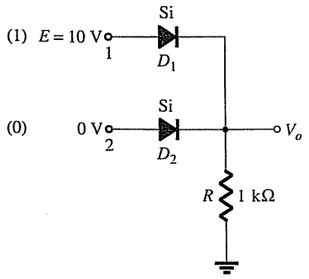


FIG. 2.39
Positive logic OR gate.

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EXAMPLE 2.14 Determine V_o for the network of Fig. 2.39.

Solution: First note that there is only one applied potential; 10 V at terminal 1. Terminal 2 with a 0-V input is essentially at ground potential, as shown in the redrawn network of Fig. 2.40. Figure 2.40 "suggests" that D_1 is probably in the "on" state due to the applied 10 V, whereas D_2 with its "positive" side at 0 V is probably "off." Assuming these states will result in the configuration of Fig. 2.41.

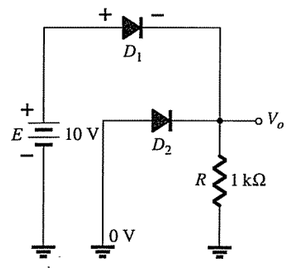


FIG. 2.40
Redrawn network of Fig. 2.39.

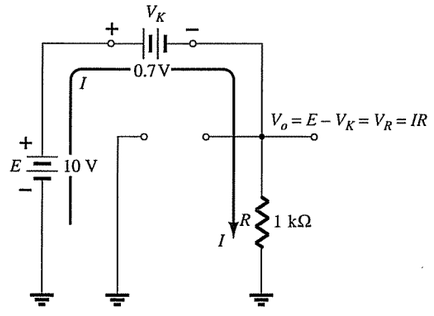


FIG. 2.41
Assumed diode states for Fig. 2.40.

The next step is simply to check that there is no contradiction in our assumptions. That is, note that the polarity across D_1 is such as to turn it on and the polarity across D_2 is such as to turn it off. For D_1 the "on" state establishes V_o at $V_o = E - V_D = 10\text{ V} - 0.7\text{ V} = \mathbf{9.3\text{ V}}$. With 9.3 V at the cathode (−) side of D_2 and 0 V at the anode (+) side, D_2 is definitely in the "off" state. The current direction and the resulting continuous path for conduction further confirm our assumption that D_1 is conducting. Our assumptions seem confirmed by the resulting voltages and current, and our initial analysis can be assumed to be correct. The output voltage level is not 10 V as defined for an input of 1, but the 9.3 V is sufficiently large to be considered a 1 level. The output is therefore at a 1 level with only one input, which suggests that the gate is an OR gate. An analysis of the same network with two 10-V inputs will result in both diodes being in the "on" state and an output of 9.3 V. A 0-V input at both inputs will not provide the 0.7 V required to turn the diodes on, and the output will be a 0 due to the 0-V output level. For the network of Fig. 2.41 the current level is determined by

$$I = \frac{E - V_D}{R} = \frac{10\text{ V} - 0.7\text{ V}}{1\text{ k}\Omega} = \mathbf{9.3\text{ mA}}$$

EXAMPLE 2.15 Determine the output level for the positive logic AND gate of Fig. 2.42.

Solution: Note in this case that an independent source appears in the grounded leg of the network. For reasons soon to become obvious, it is chosen at the same level as the input logic level. The network is redrawn in Fig. 2.43 with our initial assumptions regarding the state of the diodes. With 10 V at the cathode side of D_1 it is assumed that D_1 is in the "off" state even though there is a 10-V source connected to the anode of D_1 through the resistor.

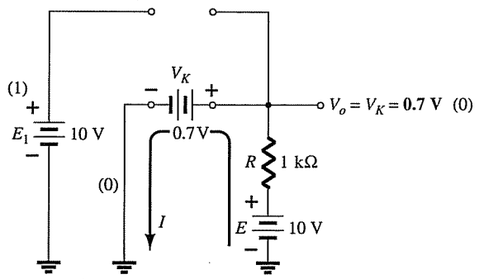


FIG. 2.43
Substituting the assumed states for the diodes of Fig. 2.42.

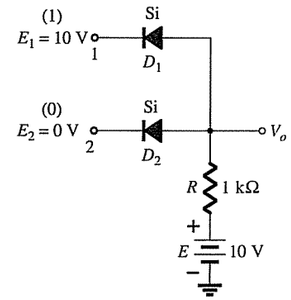


FIG. 2.42
Positive logic AND gate.

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However, recall that we mentioned in the introduction to this section that the use of the approximate model will be an aid to the analysis. For D_1, where will the 0.7 V come from if the input and source voltages are at the same level and creating opposing "pressures"? D_2 is assumed to be in the "on" state due to the low voltage at the cathode side and the availability of the 10-V source through the 1-kΩ resistor.

For the network of Fig. 2.43 the voltage at V_o is 0.7 V due to the forward-biased diode D_2. With 0.7 V at the anode of D_1 and 10 V at the cathode, D_1 is definitely in the "off" state. The current I will have the direction indicated in Fig. 2.43 and a magnitude equal to

$$I = \frac{E - V_K}{R} = \frac{10\text{ V} - 0.7\text{ V}}{1\text{ k}\Omega} = \mathbf{9.3\text{ mA}}$$

The state of the diodes is therefore confirmed and our earlier analysis was correct. Although not 0 V as earlier defined for the 0 level, the output voltage is sufficiently small to be considered a 0 level. For the AND gate, therefore, a single input will result in a 0-level output. The remaining states of the diodes for the possibilities of two inputs and no inputs will be examined in the problems at the end of the chapter.

2.6 SINUSOIDAL INPUTS; HALF-WAVE RECTIFICATION

The diode analysis will now be expanded to include time-varying functions such as the sinusoidal waveform and the square wave. There is no question that the degree of difficulty will increase, but once a few fundamental maneuvers are understood, the analysis will be fairly direct and follow a common thread.

The simplest of networks to examine with a time-varying signal appears in Fig. 2.44. For the moment we will use the ideal model (note the absence of the Si, Ge, or GaAs label) to ensure that the approach is not clouded by additional mathematical complexity.

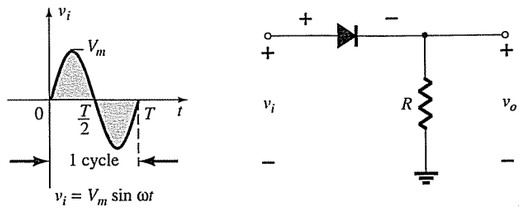


FIG. 2.44
Half-wave rectifier.

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Over one full cycle, defined by the period T of Fig. 2.44, the average value (the algebraic sum of the areas above and below the axis) is zero. The circuit of Fig. 2.44, called a *half-wave rectifier*, will generate a waveform v_o that will have an average value of particular use in the ac-to-dc conversion process. When employed in the rectification process, a diode is typically referred to as a *rectifier.* Its power and current ratings are typically much higher than those of diodes employed in other applications, such as computers and communication systems.

During the interval $t = 0 \rightarrow T/2$ in Fig. 2.44 the polarity of the applied voltage v_i is such as to establish "pressure" in the direction indicated and turn on the diode with the polarity appearing above the diode. Substituting the short-circuit equivalence for the ideal diode will result in the equivalent circuit of Fig. 2.45, where it is fairly obvious that the output signal is an exact replica of the applied signal. The two terminals defining the output voltage are connected directly to the applied signal via the short-circuit equivalence of the diode.

For the period $T/2 \rightarrow T$, the polarity of the input v_i is as shown in Fig. 2.46, and the resulting polarity across the ideal diode produces an "off" state with an open-circuit equivalent. The result is the absence of a path for charge to flow, and $v_o = iR = (0)R = 0$ V for the period $T/2 \rightarrow T$. The input v_i and the output v_o are sketched together in Fig. 2.47 for comparison purposes. The output signal v_o now has a net positive area above the axis over

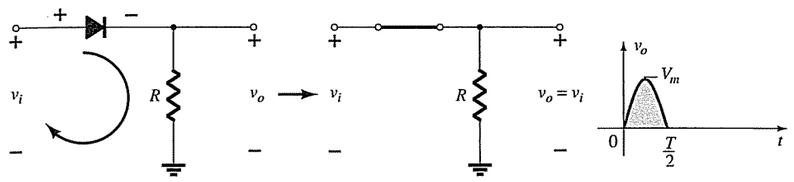


FIG. 2.45
Conduction region ($0 \rightarrow T/2$).

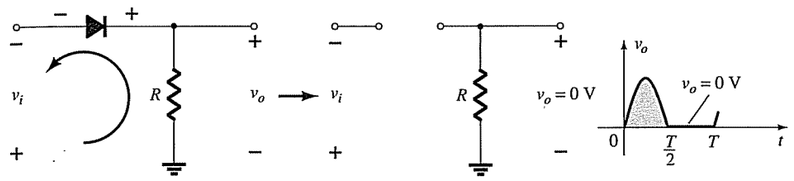


FIG. 2.46
Nonconduction region ($T/2 \rightarrow T$).

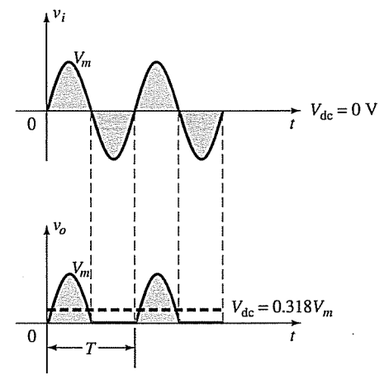


FIG. 2.47
Half-wave rectified signal.

a full period and an average value determined by

$$\boxed{V_{dc} = 0.318\,V_m}\ \text{half-wave} \qquad \textbf{(2.7)}$$

The process of removing one-half the input signal to establish a dc level is called *half-wave rectification.*

The effect of using a silicon diode with $V_K = 0.7$ V is demonstrated in Fig. 2.48 for the forward-bias region. The applied signal must now be at least 0.7 V before the diode can turn "on." For levels of v_i less than 0.7 V, the diode is still in an open-circuit state and $v_o = 0$ V, as shown in the same figure. When conducting, the difference between v_o and v_i is a fixed

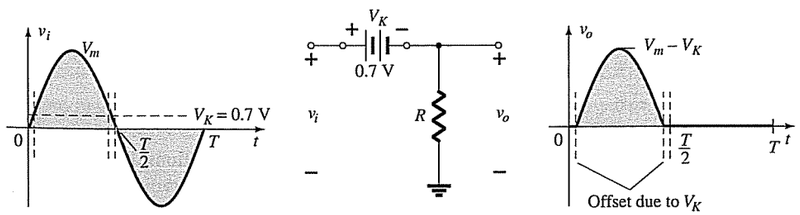


FIG. 2.48
Effect of V_K on half-wave rectified signal.

level of $V_K = 0.7$ V and $v_o = v_i - V_K$, as shown in the figure. The net effect is a reduction in area above the axis, which reduces the resulting dc voltage level. For situations where $V_m \gg V_K$, the following equation can be applied to determine the average value with a relatively high level of accuracy.

$$V_{dc} \cong 0.318(V_m - V_K) \tag{2.8}$$

In fact, if V_m is sufficiently greater than V_K, Eq. (2.7) is often applied as a first approximation for V_{dc}.



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EXAMPLE 2.16

a. Sketch the output v_o and determine the dc level of the output for the network of Fig. 2.49.
b. Repeat part (a) if the ideal diode is replaced by a silicon diode.
c. Repeat parts (a) and (b) if V_m is increased to 200 V, and compare solutions using Eqs. (2.7) and (2.8).

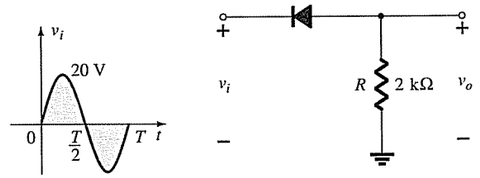


FIG. 2.49
Network for Example 2.16.

Solution:

a. In this situation the diode will conduct during the negative part of the input as shown in Fig. 2.50, and v_o will appear as shown in the same figure. For the full period, the dc level is

$$V_{dc} = -0.318V_m = -0.318(20\text{ V}) = \mathbf{-6.36\text{ V}}$$

The negative sign indicates that the polarity of the output is opposite to the defined polarity of Fig. 2.49.

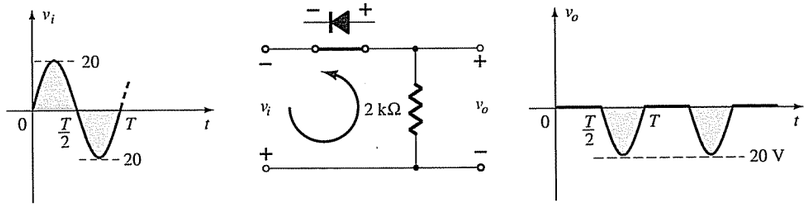


FIG. 2.50
Resulting v_o for the circuit of Example 2.16.

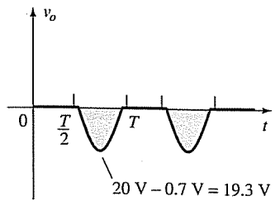


FIG. 2.51
Effect of V_K on output of Fig. 2.50.

b. For a silicon diode, the output has the appearance of Fig. 2.51, and

$$V_{dc} \cong -0.318(V_m - 0.7\text{ V}) = -0.318(19.3\text{ V}) \cong \mathbf{-6.14\text{ V}}$$

The resulting drop in dc level is 0.22 V, or about 3.5%.

c. Eq. (2.7): $V_{dc} = -0.318\,V_m = -0.318(200\text{ V}) = \mathbf{-63.6\text{ V}}$

Eq. (2.8): $V_{dc} = -0.318(V_m - V_K) = -0.318(200\text{ V} - 0.7\text{ V})$
$= -(0.318)(199.3\text{ V}) = \mathbf{-63.38\text{ V}}$

which is a difference that can certainly be ignored for most applications. For part (c) the offset and drop in amplitude due to V_K would not be discernible on a typical oscilloscope if the full pattern is displayed.

PIV (PRV)

The peak inverse voltage (PIV) [or PRV (peak reverse voltage)] rating of the diode is of primary importance in the design of rectification systems. Recall that it is the voltage rating that must not be exceeded in the reverse-bias region or the diode will enter the Zener avalanche region. The required PIV rating for the half-wave rectifier can be determined from Fig. 2.52, which displays the reverse-biased diode of Fig. 2.44 with maximum applied voltage. Applying Kirchhoff's voltage law, it is fairly obvious that the PIV rating of the diode must equal or exceed the peak value of the applied voltage. Therefore,

$$\text{PIV rating} \geqq V_m \quad \text{half-wave rectifier} \tag{2.9}$$

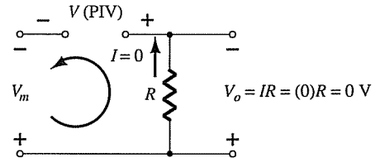


FIG. 2.52
Determining the required PIV rating for the half-wave rectifier.

2.7 FULL-WAVE RECTIFICATION

Bridge Network

The dc level obtained from a sinusoidal input can be improved 100% using a process called *full-wave rectification*. The most familiar network for performing such a function appears in Fig. 2.53 with its four diodes in a *bridge* configuration. During the period $t = 0$ to $T/2$ the polarity of the input is as shown in Fig. 2.54. The resulting polarities across the ideal diodes are also shown in Fig. 2.54 to reveal that D_2 and D_3 are conducting, whereas D_1 and D_4 are in the "off" state. The net result is the configuration of Fig. 2.55, with its indicated current and polarity across R. Since the diodes are ideal, the load voltage is $v_o = v_i$, as shown in the same figure.

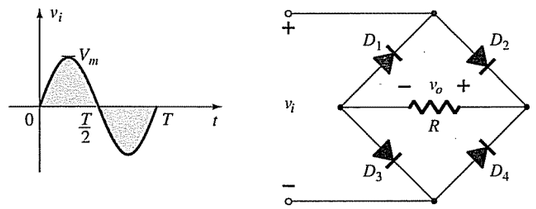


FIG. 2.53
Full-wave bridge rectifier.

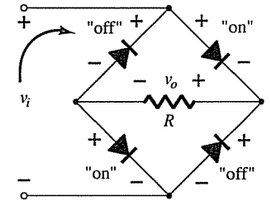


FIG. 2.54
Network of Fig. 2.53 for the period $0 \rightarrow T/2$ of the input voltage v_i.

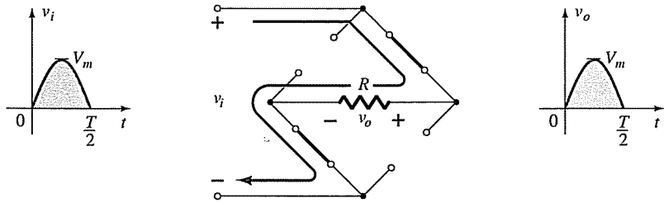


FIG. 2.55
Conduction path for the positive region of v_i.

For the negative region of the input the conducting diodes are D_1 and D_4, resulting in the configuration of Fig. 2.56. The important result is that the polarity across the load resistor R is the same as in Fig. 2.54, establishing a second positive pulse, as shown in Fig. 2.56. Over one full cycle the input and output voltages will appear as shown in Fig. 2.57.

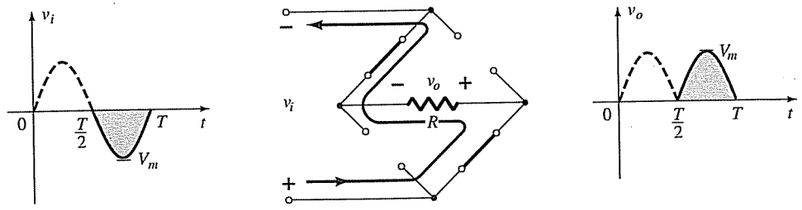


FIG. 2.56
Conduction path for the negative region of v_i.

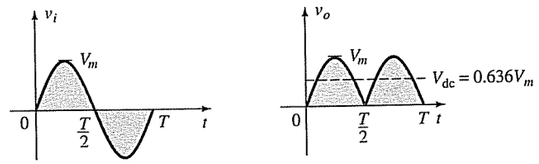


FIG. 2.57
Input and output waveforms for a full-wave rectifier.

Since the area above the axis for one full cycle is now twice that obtained for a half-wave system, the dc level has also been doubled and

$$V_{dc} = 2[\text{Eq. (2.7)}] = 2(0.318V_m)$$

or

$$\boxed{V_{dc} = 0.636\,V_m} \quad \text{full-wave} \qquad \textbf{(2.10)}$$

If silicon rather than ideal diodes are employed as shown in Fig. 2.58, the application of Kirchhoff's voltage law around the conduction path results in

$$v_i - V_K - v_o - V_K = 0$$

and

$$v_o = v_i - 2V_K$$

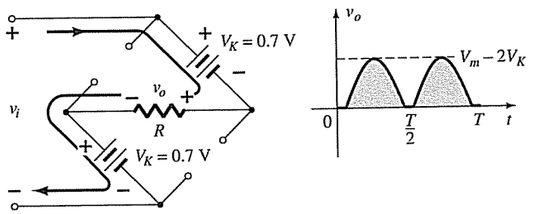


FIG. 2.58
Determining $V_{o_{max}}$ for silicon diodes in the bridge configuration.

The peak value of the output voltage v_o is therefore

$$V_{o_{max}} = V_m - 2V_K$$

For situations where $V_m \gg 2V_K$, the following equation can be applied for the average value with a relatively high level of accuracy:

$$\boxed{V_{dc} \cong 0.636(V_m - 2V_K)} \qquad \textbf{(2.11)}$$

Then again, if V_m is sufficiently greater than $2V_K$, then Eq. (2.10) is often applied as a first approximation for V_{dc}.

PIV The required PIV of each diode (ideal) can be determined from Fig. 2.59 obtained at the peak of the positive region of the input signal. For the indicated loop the maximum voltage across R is V_m and the PIV rating is defined by

$$\boxed{\text{PIV} \geqq V_m} \quad \text{full-wave bridge rectifier} \qquad \textbf{(2.12)}$$

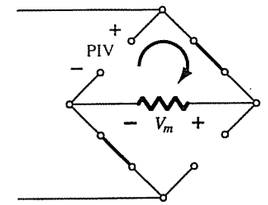


FIG. 2.59
Determining the required PIV for the bridge configuration.

Center-Tapped Transformer

A second popular full-wave rectifier appears in Fig. 2.60 with only two diodes but requiring a center-tapped (CT) transformer to establish the input signal across each section of the secondary of the transformer. During the positive portion of v_i applied to the primary of the transformer, the network will appear as shown in Fig. 2.61. D_1 assumes the short-circuit equivalent and D_2 the open-circuit equivalent, as determined by the secondary voltages and the resulting current directions. The output voltage appears as shown in Fig. 2.61.

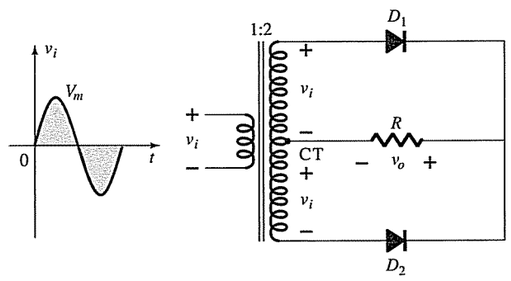


FIG. 2.60
Center-tapped transformer full-wave rectifier.

Multisim

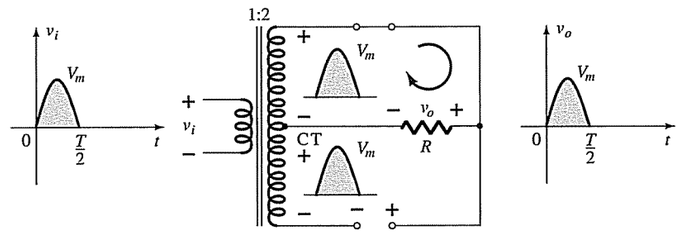


FIG. 2.61
Network conditions for the positive region of v_i.

During the negative portion of the input the network appears as shown in Fig. 2.62, reversing the roles of the diodes but maintaining the same polarity for the voltage across the load resistor R. The net effect is the same output as that appearing in Fig. 2.57 with the same dc levels.

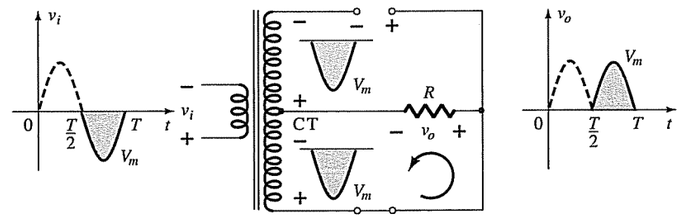


FIG. 2.62
Network conditions for the negative region of v_i.

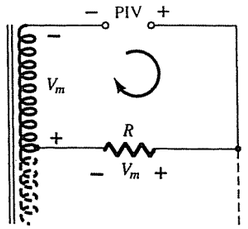


FIG. 2.63
Determining the PIV level for the diodes of the CT transformer full-wave rectifier.

PIV The network of Fig. 2.63 will help us determine the net PIV for each diode for this full-wave rectifier. Inserting the maximum voltage for the secondary voltage and V_m as established by the adjoining loop results in

$$\text{PIV} = V_{\text{secondary}} + V_R$$
$$= V_m + V_m$$

and

$$\boxed{\text{PIV} \geqq 2V_m} \quad \text{CT transformer, full-wave rectifier} \tag{2.13}$$

EXAMPLE 2.17 Determine the output waveform for the network of Fig. 2.64 and calculate the output dc level and the required PIV of each diode.

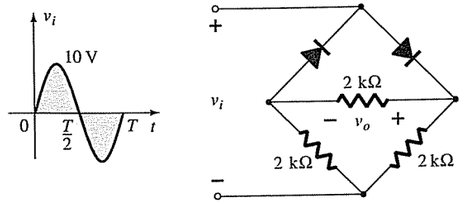


FIG. 2.64
Bridge network for Example 2.17.

PSpice

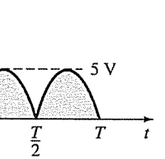
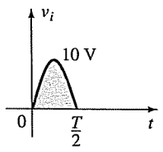


FIG. 2.67
Resulting output for Example 2.17.



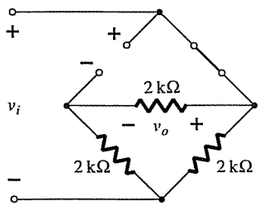


FIG. 2.65
Network of Fig. 2.64 for the positive region of v_i.

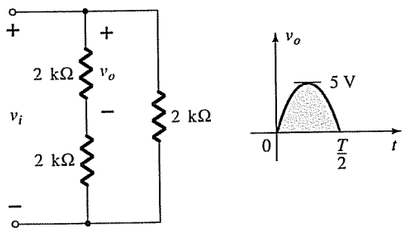


FIG. 2.66
Redrawn network of Fig. 2.65.

Solution: The network appears as shown in Fig. 2.65 for the positive region of the input voltage. Redrawing the network results in the configuration of Fig. 2.66, where $v_o = \frac{1}{2}v_i$ or $V_{o_{\max}} = \frac{1}{2}V_{i_{\max}} = \frac{1}{2}(10\,\text{V}) = 5\,\text{V}$, as shown in Fig. 2.66. For the negative part of the input the roles of the diodes are interchanged and v_o appears as shown in Fig. 2.67.

The effect of removing two diodes from the bridge configuration is therefore to reduce the available dc level to the following:

$$V_{\text{dc}} = 0.636(5\,\text{V}) = \mathbf{3.18\,V}$$

or that available from a half-wave rectifier with the same input. However, the PIV as determined from Fig. 2.59 is equal to the maximum voltage across R, which is 5 V, or half of that required for a half-wave rectifier with the same input.

2.8 CLIPPERS

The previous section on rectification gives clear evidence that diodes can be used to change the appearance of an applied waveform. This section on clippers and the next on clampers will expand on the wave-shaping abilities of diodes.

Clippers are networks that employ diodes to "clip" away a portion of an input signal without distorting the remaining part of the applied waveform.

The half-wave rectifier of Section 2.6 is an example of the simplest form of diode clipper—one resistor and a diode. Depending on the orientation of the diode, the positive or negative region of the applied signal is "clipped" off.

There are two general categories of clippers: *series* and *parallel*. The series configuration is defined as one where the diode is in series with the load, whereas the parallel variety has the diode in a branch parallel to the load.

Series

The response of the series configuration of Fig. 2.68a to a variety of alternating waveforms is provided in Fig. 2.68b. Although first introduced as a half-wave rectifier (for sinusoidal waveforms), there are no boundaries on the type of signals that can be applied to a clipper.

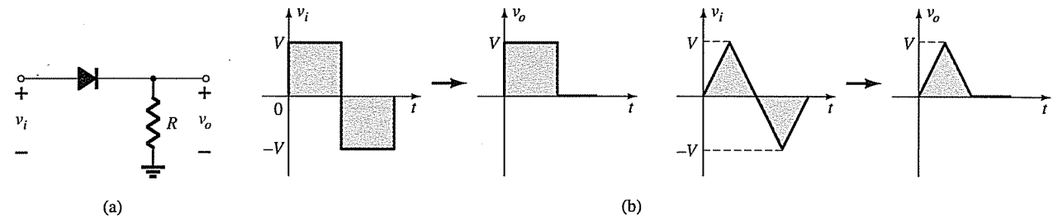


FIG. 2.68
Series clipper.

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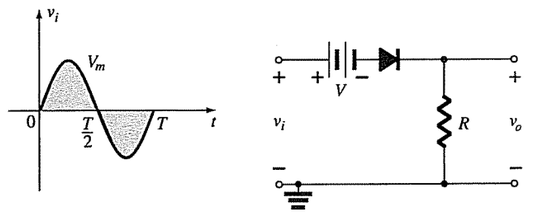


FIG. 2.69
Series clipper with a dc supply.

The addition of a dc supply to the network as shown in Fig. 2.69 can have a pronounced effect on the analysis of the series clipper configuration. The response is not as obvious because the dc supply can aid or work against the source voltage, and the dc supply can be in the leg between the supply and output or in the branch parallel to the output.

There is no general procedure for analyzing networks such as the type in Fig. 2.69, but there are some things one can do to give the analysis some direction.

First and most important:

1. **Take careful note of where the output voltage is defined.**

In Fig. 2.69 it is directly across the resistor R. In some cases it may be across a combination of series elements.

Next:

2. **Try to develop an overall sense of the response by simply noting the "pressure" established by each supply and the effect it will have on the conventional current direction through the diode.**

In Fig. 2.69, for instance, any positive voltage of the supply will try to turn the diode on by establishing a conventional current through the diode that matches the arrow in the diode symbol. However, the added dc supply V will oppose that applied voltage and try to keep the diode in the "off" state. The result is that any supply voltage greater than V volts will turn the diode on and conduction can be established through the load resistor. Keep in mind that we are dealing with an ideal diode for the moment, so the turn-on voltage is simply 0 V. In general, therefore, for the network of Fig. 2.69 we can conclude that the diode will be on

for any voltage v_i that is greater than V volts and off for any lesser voltage. For the "off" condition, the output would be 0 V due to the lack of current, and for the "on" condition it would simply be $v_o = v_i - V$ as determined by Kirchhoff's voltage law. In total, therefore, a solution was determined without having to pick up a pencil, just by reviewing the elements present and how they interact. Now, some networks will be more complex, so it is wise to consider applying the following steps.

3. **Determine the applied voltage (transition voltage) that will result in a change of state for the diode from the "off" to the "on" state.**

This step will help to define a region of the applied voltage when the diode is on and when it is off. On the characteristics of an ideal diode this will occur when $V_D = 0$ V and $I_D = 0$ mA. For the approximate equivalent this is determined by finding the applied voltage when the diode has a drop of 0.7 V across it (for silicon) and $I_D = 0$ mA.

This exercise was applied to the network of Fig. 2.69 as shown in Fig. 2.70. Note the substitution of the short-circuit equivalent for the diode and the fact that the voltage across the resistor is 0 V because the diode current is 0 mA. The result is $v_i - V = 0$, and so

$$\boxed{v_i = V} \tag{2.14}$$

is the transition voltage.

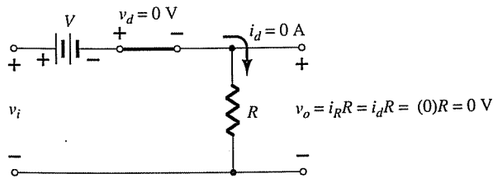


FIG. 2.70
Determining the transition level for the circuit of Fig. 2.69.

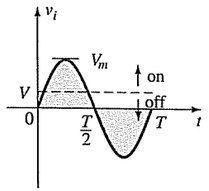


FIG. 2.71
Using the transition voltage to define the "on" and "off" regions.

This permits drawing a line on the sinusoidal supply voltage as shown in Fig. 2.71 to define the regions where the diode is on and off.

For the "on" region, as shown in Fig. 2.72, the diode is replaced by a short-circuit equivalent, and the output voltage is defined by

$$\boxed{v_o = v_i - V} \tag{2.15}$$

For the "off" region, the diode is an open circuit, $I_D = 0$ mA, and the output voltage is

$$\boxed{v_o = 0\,\text{V}}$$

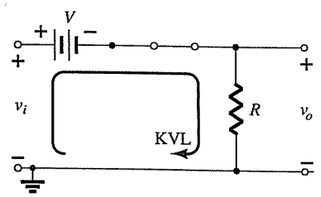


FIG. 2.72
Determining v_o for the diode in the "on" state.

4. **It is often helpful to draw the output waveform directly below the applied voltage using the same scales for the horizontal axis and the vertical axis.**

Using this last piece of information, we can establish the 0-V level on the plot of Fig. 2.73 for the region indicated. For the "on" condition, Eq. (2.15) can be used to find the output voltage when the applied voltage has its peak value:

$$v_{o_{peak}} = V_m - V$$

and this can be added to the plot of Fig. 2.73. It is then simple to fill in the missing section of the output curve.

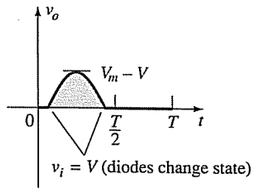


FIG. 2.73
Sketching the waveform of v_o using the results obtained for v_o above and below the transition level.

EXAMPLE 2.18 Determine the output waveform for the sinusoidal input of Fig. 2.74.

Solution:

Step 1: The output is again directly across the resistor R.

Step 2: The positive region of v_i and the dc supply are both applying "pressure" to turn the diode on. The result is that we can safely assume the diode is in the "on" state for the entire range of positive voltages for v_i. Once the supply goes negative, it would have to exceed the

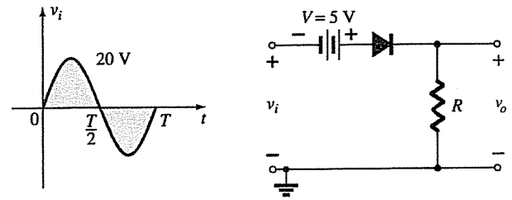


FIG. 2.74
Series clipper for Example 2.18.

dc supply voltage of 5 V before it could turn the diode off. A general feeling about the behavior of the network has therefore been established.

Step 3: The transition model is substituted in Fig. 2.75, and we find that the transition from one state to the other will occur when

$$v_i + 5\,\text{V} = 0\,\text{V}$$

or

$$v_i = -5\,\text{V}$$

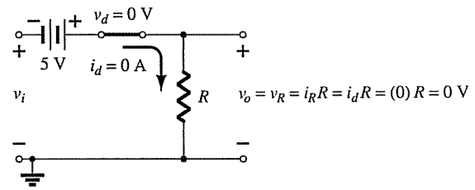


FIG. 2.75
Determining the transition level for the clipper of Fig. 2.74.

Step 4: In Fig. 2.76 a horizontal line is drawn through the applied voltage at the transition level. For voltages less than −5 V the diode is in the open-circuit state and the output is 0 V, as shown in the sketch of v_o. Using Fig. 2.76, we find that for conditions when the diode is on and the diode current is established the output voltage will be the following, as determined using Kirchhoff's voltage law:

$$v_o = v_i + 5\,\text{V}$$

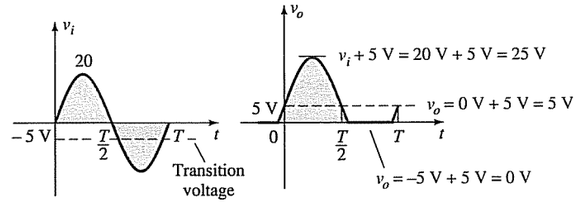


FIG. 2.76
Sketching v_o for Example 2.18.

The analysis of clipper networks with square-wave inputs is actually easier than with sinusoidal inputs because only two levels have to be considered. In other words, the network can be analyzed as if it had two dc level inputs with the resulting v_o plotted in the proper time frame. The next example demonstrates the procedure.

EXAMPLE 2.19 Find the output voltage for the network examined in Example 2.18 if the applied signal is the square wave of Fig. 2.77.

Solution: For $v_i = 20\,\text{V}\ (0 \rightarrow T/2)$ the network of Fig. 2.78 results. The diode is in the short-circuit state, and $v_o = 20\,\text{V} + 5\,\text{V} = 25\,\text{V}$. For $v_i = -10\,\text{V}$ the network of Fig. 2.79

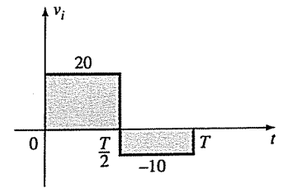


FIG. 2.77
Applied signal for Example 2.19.

results, placing the diode in the "off" state, and $v_o = i_R R = (0)R = 0$ V. The resulting output voltage appears in Fig. 2.80.

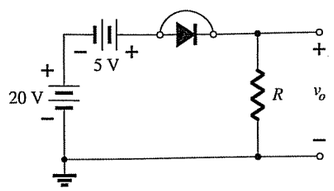


FIG. 2.78
v_o *at* $v_i = +20$ *V.*

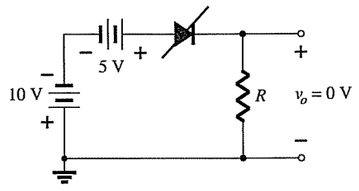


FIG. 2.79
v_o *at* $v_i = -10$ *V.*

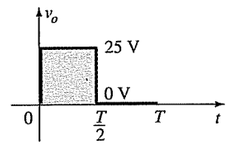


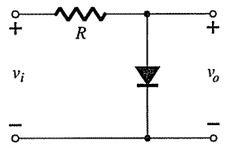
FIG. 2.80
Sketching v_o *for Example 2.19.*

Note in Example 2.19 that the clipper not only clipped off 5 V from the total swing, but also raised the dc level of the signal by 5 V.

Parallel

The network of Fig. 2.81 is the simplest of parallel diode configurations with the output for the same inputs of Fig. 2.68. The analysis of parallel configurations is very similar to that applied to series configurations, as demonstrated in the next example.

Multisim



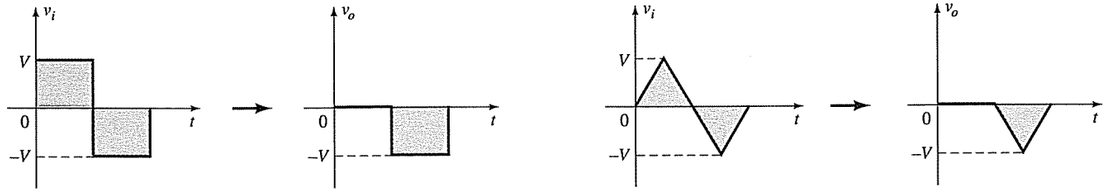


FIG. 2.81
Response to a parallel clipper.

EXAMPLE 2.20 Determine v_o for the network of Fig. 2.82.

Solution:

Step 1: In this example the output is defined across the series combination of the 4-V supply and the diode, not across the resistor *R*.

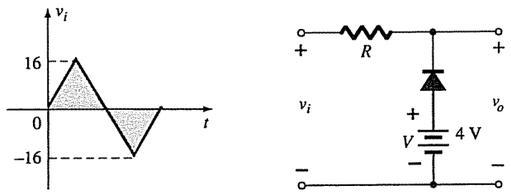


FIG. 2.82
Example 2.20.

Step 2: The polarity of the dc supply and the direction of the diode strongly suggest that the diode will be in the "on" state for a good portion of the negative region of the input signal. In fact, it is interesting to note that since the output is directly across the series combination, when the diode is in its short-circuit state the output voltage will be directly across the 4-V dc supply, requiring that the output be fixed at 4 V. In other words, when the diode is on the output will be 4 V. Other than that, when the diode is an open circuit, the current through the series network will be 0 mA and the voltage drop across the resistor will be 0 V. That will result in $v_o = v_i$ whenever the diode is off.

Step 3: The transition level of the input voltage can be found from Fig. 2.83 by substituting the short-circuit equivalent and remembering the diode current is 0 mA at the instant of transition. The result is a change in state when

$$v_i = 4 \text{ V}$$

Step 4: In Fig. 2.84 the transition level is drawn along with $v_o = 4$ V when the diode is on. For $v_i \geq 4$ V, $v_o = 4$ V, and the waveform is simply repeated on the output plot.

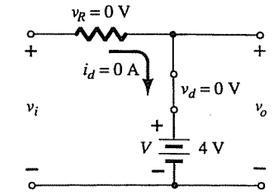


FIG. 2.83
Determining the transition level for Example 2.20.

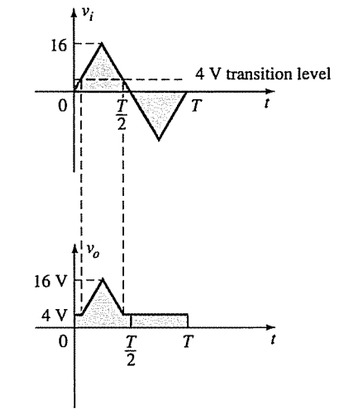


FIG. 2.84
Sketching v_o *for Example 2.20.*

To examine the effects of the knee voltage V_K of a silicon diode on the output response, the next example will specify a silicon diode rather than the ideal diode equivalent.

EXAMPLE 2.21 Repeat Example 2.20 using a silicon diode with $V_K = 0.7$ V.

Solution: The transition voltage can first be determined by applying the condition $i_d = 0$ A at $v_d = V_D = 0.7$ V and obtaining the network of Fig. 2.85. Applying Kirchhoff's voltage law around the output loop in the clockwise direction, we find that

$$v_i + V_K - V = 0$$

and

$$v_i = V - V_K = 4 \text{ V} - 0.7 \text{ V} = \mathbf{3.3\ V}$$

For input voltages greater than 3.3 V, the diode will be an open circuit and $v_o = v_i$. For input voltages less than 3.3 V, the diode will be in the "on" state and the network of Fig. 2.86 results, where

$$v_o = 4 \text{ V} - 0.7 \text{ V} = \mathbf{3.3\ V}$$

The resulting output waveform appears in Fig. 2.87. Note that the only effect of V_K was to drop the transition level to 3.3 from 4 V.

There is no question that including the effects of V_K will complicate the analysis somewhat, but once the analysis is understood with the ideal diode, the procedure, including the effects of V_K, will not be that difficult.

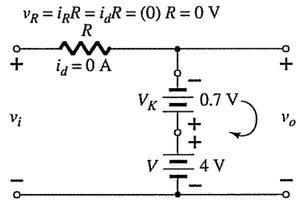


FIG. 2.85
Determining the transition level for the network of Fig. 2.82.

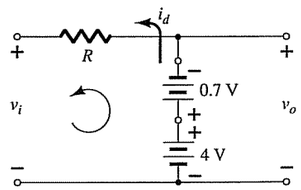


FIG. 2.86
Determining v_o *for the diode of Fig. 2.82 in the "on" state.*

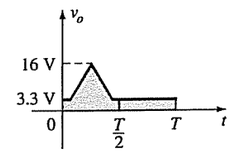
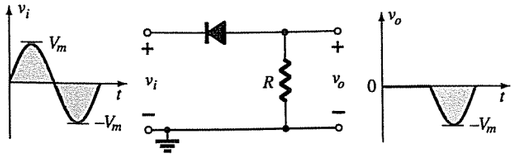


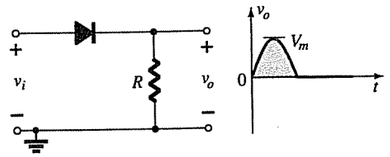
FIG. 2.87
Sketching v_o *for Example 2.21.*

Simple Series Clippers (Ideal Diodes)

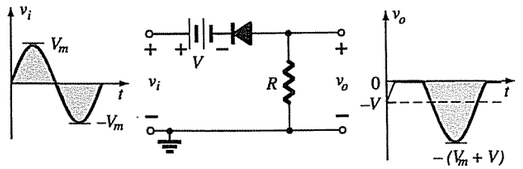
POSITIVE

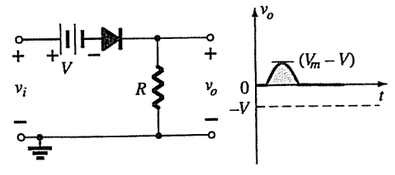


NEGATIVE

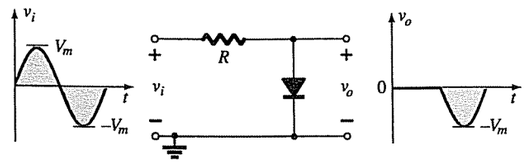


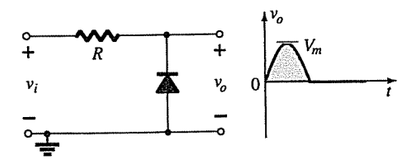
Biased Series Clippers (Ideal Diodes)



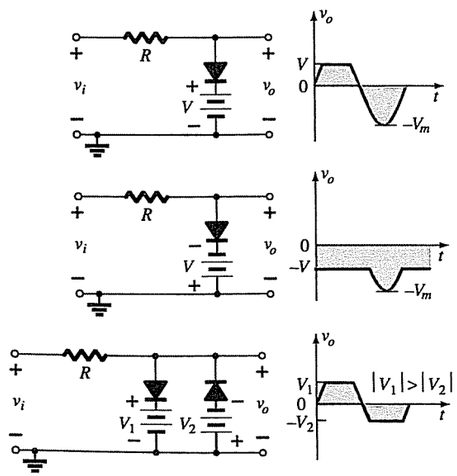


Simple Parallel Clippers (Ideal Diodes)





Biased Parallel Clippers (Ideal Diodes)



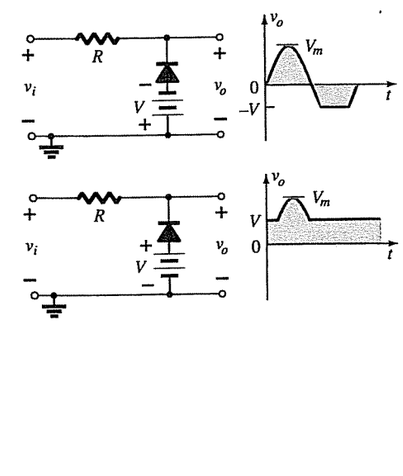


FIG. 2.88
Clipping circuits.

Summary

A variety of series and parallel clippers with the resulting output for the sinusoidal input are provided in Fig. 2.88. In particular, note the response of the last configuration, with its ability to clip off a positive and a negative section as determined by the magnitude of the dc supplies.

2.9 CLAMPERS

The previous section investigated a number of diode configurations that clipped off a portion of the applied signal without changing the remaining part of the waveform. This section will examine a variety of diode configurations that shift the applied signal to a different level.

A clamper is a network constructed of a diode, a resistor, and a capacitor that shifts a waveform to a different dc level without changing the appearance of the applied signal.

Additional shifts can also be obtained by introducing a dc supply to the basic structure. The chosen resistor and capacitor of the network must be chosen such that the time constant determined by $\tau = RC$ is sufficiently large to ensure that the voltage across the capacitor does not discharge significantly during the interval the diode is nonconducting. Throughout the analysis we assume that for all practical purposes the capacitor fully charges or discharges in five time constants.

The simplest of clamper networks is provided in Fig. 2.89. It is important to note that the capacitor is connected directly between input and output signals and the resistor and the diode are connected in parallel with the output signal.

Clamping networks have a capacitor connected directly from input to output with a resistive element in parallel with the output signal. The diode is also in parallel with the output signal but may or may not have a series dc supply as an added element.

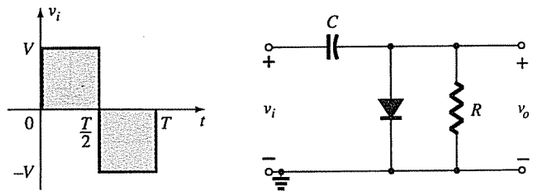


FIG. 2.89
Clamper.

There is a sequence of steps that can be applied to help make the analysis straightforward. It is not the only approach to examining clampers, but it does offer an option if difficulties surface.

Step 1: Start the analysis by examining the response of the portion of the input signal that will forward bias the diode.

Step 2: During the period that the diode is in the "on" state, assume that the capacitor will charge up instantaneously to a voltage level determined by the surrounding network.

For the network of Fig. 2.89 the diode will be forward biased for the positive portion of the applied signal. For the interval 0 to $T/2$ the network will appear as shown in Fig. 2.90. The short-circuit equivalent for the diode will result in $v_o = 0$ V for this time interval, as shown in the sketch of v_o in Fig. 2.92. During this same interval of time, the time constant determined by $\tau = RC$ is very small because the resistor R has been effectively "shorted out" by the conducting diode and the only resistance present is the inherent (contact, wire) resistance of the network. The result is that the capacitor will quickly charge to the peak value of V volts as shown in Fig. 2.90 with the polarity indicated.

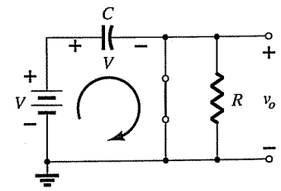


FIG. 2.90
Diode "on" and the capacitor charging to V volts.

Step 3: Assume that during the period when the diode is in the "off" state the capacitor holds on to its established voltage level.

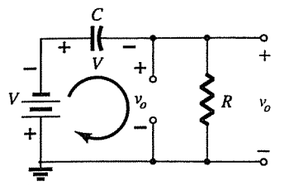


FIG. 2.91
Determining v_o with the diode "off."

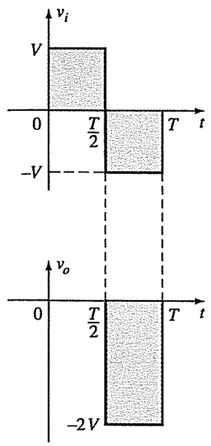


FIG. 2.92
Sketching v_o for the network of Fig. 2.91.

Step 4: Throughout the analysis, maintain a continual awareness of the location and defined polarity for v_o to ensure that the proper levels are obtained.

When the input switches to the $-V$ state, the network will appear as shown in Fig. 2.91, with the open-circuit equivalent for the diode determined by the applied signal and stored voltage across the capacitor—both "pressuring" current through the diode from cathode to anode. Now that R is back in the network the time constant determined by the RC product is sufficiently large to establish a discharge period 5τ, much greater than the period $T/2 \rightarrow T$, and it can be assumed on an approximate basis that the capacitor holds onto all its charge and, therefore, voltage (since $V = Q/C$) during this period.

Since v_o is in parallel with the diode and resistor, it can also be drawn in the alternative position shown in Fig. 2.91. Applying Kirchhoff's voltage law around the input loop results in

$$-V - V - v_o = 0$$

and

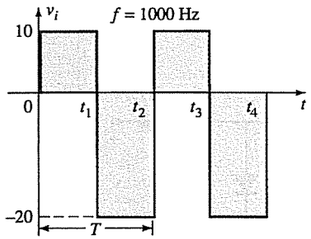
$$v_o = -2V$$

The negative sign results from the fact that the polarity of $2V$ is opposite to the polarity defined for v_o. The resulting output waveform appears in Fig. 2.92 with the input signal. The output signal is clamped to 0 V for the interval 0 to $T/2$ but maintains the same total swing ($2V$) as the input.

Step 5: Check that the total swing of the output matches that of the input.

This is a property that applies for all clamping networks, giving an excellent check on the results obtained.

EXAMPLE 2.22 Determine v_o for the network of Fig. 2.93 for the input indicated.



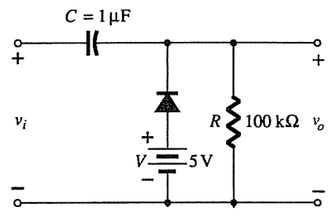


FIG. 2.93
Applied signal and network for Example 2.22.



Multisim
PSpice

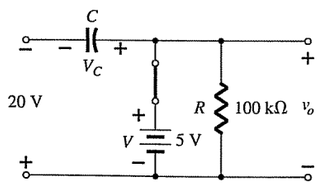


FIG. 2.94
Determining v_o and V_C with the diode in the "on" state.

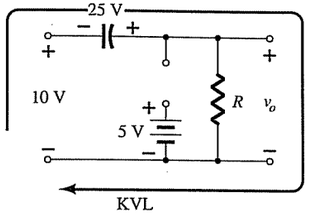


FIG. 2.95
Determining v_o with the diode in the "off" state.

Solution: Note that the frequency is 1000 Hz, resulting in a period of 1 ms and an interval of 0.5 ms between levels. The analysis will begin with the period $t_1 \rightarrow t_2$ of the input signal since the diode is in its short-circuit state. For this interval the network will appear as shown in Fig. 2.94. The output is across R, but it is also directly across the 5-V battery if one follows the direct connection between the defined terminals for v_o and the battery terminals. The result is $v_o = 5$ V for this interval. Applying Kirchhoff's voltage law around the input loop results in

$$-20\text{ V} + V_C - 5\text{ V} = 0$$

and

$$V_C = 25\text{ V}$$

The capacitor will therefore charge up to 25 V. In this case the resistor R is not shorted out by the diode, but a Thévenin equivalent circuit of that portion of the network that includes the battery and the resistor will result in $R_{Th} = 0\ \Omega$ with $E_{Th} = V = 5$ V. For the period $t_2 \rightarrow t_3$ the network will appear as shown in Fig. 2.95.

The open-circuit equivalent for the diode removes the 5-V battery from having any effect on v_o, and applying Kirchhoff's voltage law around the outside loop of the network results in

$$+10\text{ V} + 25\text{ V} - v_o = 0$$

and

$$v_o = 35\text{ V}$$

The time constant of the discharging network of Fig. 2.95 is determined by the product RC and has the magnitude

$$\tau = RC = (100\,\text{k}\Omega)(0.1\,\mu\text{F}) = 0.01\text{ s} = 10\text{ ms}$$

The total discharge time is therefore $5\tau = 5(10\text{ ms}) = 50$ ms.

Since the interval $t_2 \rightarrow t_3$ will only last for 0.5 ms, it is certainly a good approximation that the capacitor will hold its voltage during the discharge period between pulses of the input signal. The resulting output appears in Fig. 2.96 with the input signal. Note that the output swing of 30 V matches the input swing as noted in step 5.

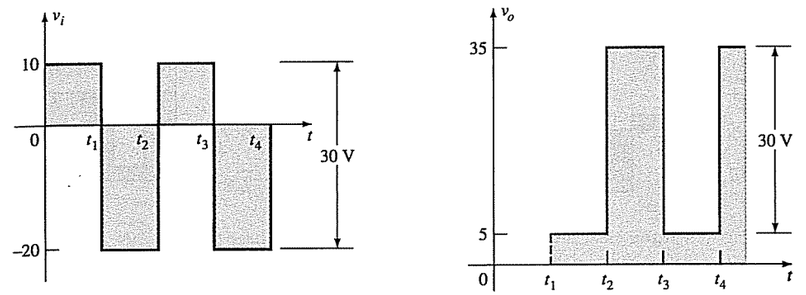


FIG. 2.96
v_i and v_o for the clamper of Fig. 2.93.

EXAMPLE 2.23 Repeat Example 2.22 using a silicon diode with $V_K = 0.7$ V.

Solution: For the short-circuit state the network now takes on the appearance of Fig. 2.97, and v_o can be determined by Kirchhoff's voltage law in the output section:

$$+5\text{ V} - 0.7\text{ V} - v_o = 0$$

and

$$v_o = 5\text{ V} - 0.7\text{ V} = 4.3\text{ V}$$

For the input section Kirchhoff's voltage law results in

$$-20\text{ V} + V_C + 0.7\text{ V} - 5\text{ V} = 0$$

and

$$V_C = 25\text{ V} - 0.7\text{ V} = 24.3\text{ V}$$

For the period $t_2 \rightarrow t_3$ the network will now appear as in Fig. 2.98, with the only change being the voltage across the capacitor. Applying Kirchhoff's voltage law yields

$$+10\text{ V} + 24.3\text{ V} - v_o = 0$$

and

$$v_o = 34.3\text{ V}$$

The resulting output appears in Fig. 2.99, verifying the statement that the input and output swings are the same.

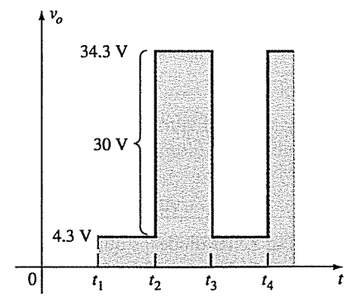


FIG. 2.99
Sketching v_o for the clamper of Fig. 2.93 with a silicon diode.

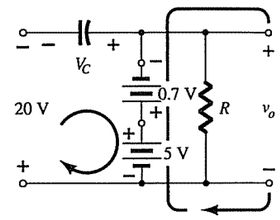


FIG. 2.97
Determining v_o and V_C with the diode in the "on" state.

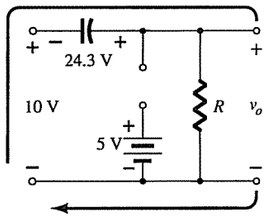


FIG. 2.98
Determining v_o with the diode in the open state.

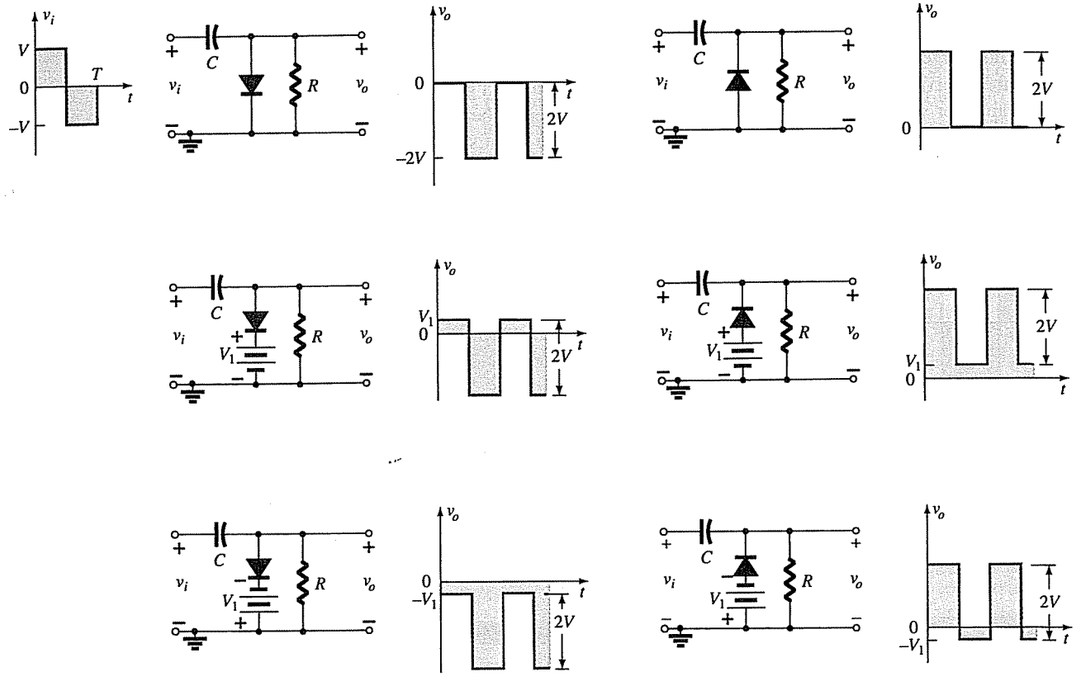


FIG. 2.100

Clamping circuits with ideal diodes ($5\tau = 5RC \gg T/2$).

A number of clamping circuits and their effect on the input signal are shown in Fig. 2.100. Although all the waveforms appearing in Fig. 2.100 are square waves, clamping networks work equally well for sinusoidal signals. In fact, one approach to the analysis of clamping networks with sinusoidal inputs is to replace the sinusoidal signal by a square wave of the same peak values. The resulting output will then form an envelope for the sinusoidal response as shown in Fig. 2.101 for a network appearing in the bottom right of Fig. 2.100.

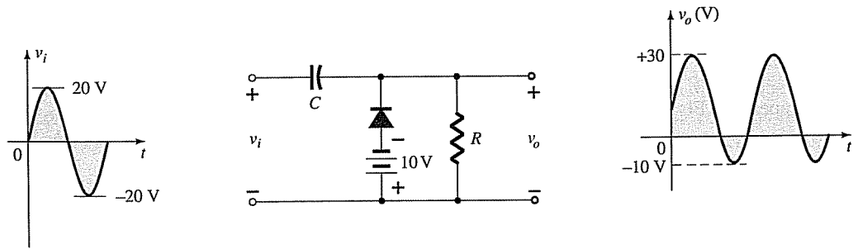


FIG. 2.101

Clamping network with a sinusoidal input.

2.10 ZENER DIODES

The analysis of networks employing Zener diodes is quite similar to the analysis of semiconductor diodes in previous sections. First the state of the diode must be determined, followed by a substitution of the appropriate model and a determination of the other unknown quantities of the network. Figure 2.102 reviews the approximate equivalent circuits for each region of a Zener diode assuming the straight-line approximations at each break point. Note that the forward-bias region is included because occasionally an application will skip into this region also.

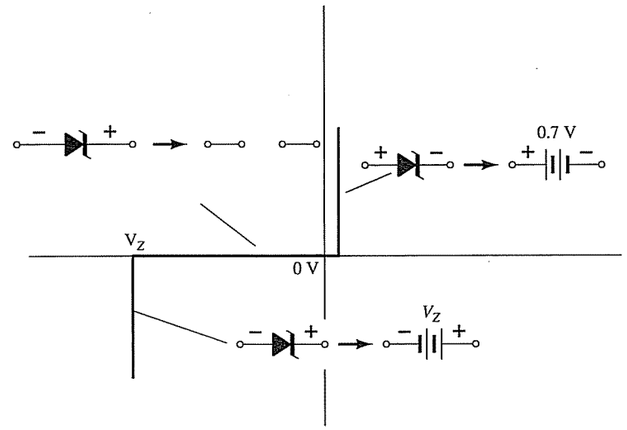


FIG. 2.102

Approximate equivalent circuits for the Zener diode in the three possible regions of application.

The first two examples will demonstrate how a Zener diode can be used to establish reference voltage levels and act as a protection device. The use of a Zener diode as a *regulator* will then be described in detail because it is one of its major areas of application. A regulator is a combination of elements designed to ensure that the output voltage of a supply remains fairly constant.

EXAMPLE 2.24 Determine the reference voltages provided by the network of Fig. 2.103, which uses a white LED to indicate that the power is on. What is the level of current through the LED and the power delivered by the supply? How does the power absorbed by the LED compare to that of the 6-V Zener diode?

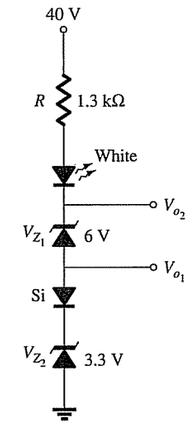


FIG. 2.103

Reference setting circuit for Example 2.24.

Solution: First we have to check that there is sufficient applied voltage to turn on all the series diode elements. The white LED will have a drop of about 4 V across it, the 6-V and 3.3-V Zener diodes have a total of 9.3 V, and the forward-biased silicon diode has 0.7 V, for a total of 14 V. The applied 40 V is then sufficient to turn on all the elements and, one hopes, establish a proper operating current.

Note that the silicon diode was used to create a reference voltage of 4 V because

$$V_{o_1} = V_{Z_2} + V_K = 3.3\text{ V} + 0.7\text{ V} = \mathbf{4.0\text{ V}}$$

Combining the voltage of the 6-V Zener diode with the 4 V results in

$$V_{o_2} = V_{o_1} + V_{Z_1} = 4\text{ V} + 6\text{ V} = \mathbf{10\text{ V}}$$

Finally, the 4 V across the white LED will leave a voltage of 40 V – 14 V = 26 V across the resistor, and

$$I_R = I_{\text{LED}} = \frac{V_R}{R} = \frac{40\text{ V} - V_{o_2} - V_{\text{LED}}}{1.3\text{ k}\Omega} = \frac{40\text{ V} - 10\text{ V} - 4\text{ V}}{1.3\text{ k}\Omega} = \frac{26\text{ V}}{1.3\text{ k}\Omega} = \mathbf{20\text{ mA}}$$

that will establish the proper brightness for the LED.

The power delivered by the supply is simply the product of the supply voltage and current drain as follows:

$$P_s = EI_s = EI_R = (40\text{ V})(20\text{ mA}) = \mathbf{800\text{ mW}}$$

The power absorbed by the LED is

$$P_{\text{LED}} = V_{\text{LED}}I_{\text{LED}} = (4\text{ V})(20\text{ mA}) = \mathbf{80\text{ mW}}$$

and the power absorbed by the 6-V Zener diode is

$$P_Z = V_Z I_Z = (6\text{ V})(20\text{ mA}) = \mathbf{120\text{ mW}}$$

The power absorbed by the Zener diode exceeds that of the LED by 40 mW.

EXAMPLE 2.25 The network of Fig. 2.104 is designed to limit the voltage to 20 V during the positive portion of the applied voltage and to 0 V for a negative excursion of the applied voltage. Check its operation and plot the waveform of the voltage across the system for the applied signal. Assume the system has a very high input resistance so it will not affect the behavior of the network.

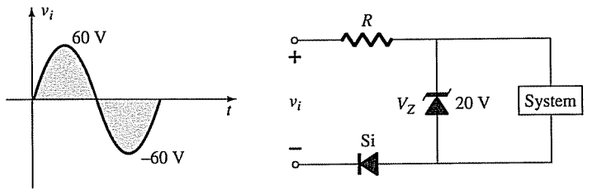


FIG. 2.104
Controlling network for Example 2.25.

Solution: For positive applied voltages less than the Zener potential of 20 V the Zener diode will be in its approximate open-circuit state, and the input signal will simply distribute itself across the elements, with the majority going to the system because it has such a high resistance level.

Once the voltage across the Zener diode reaches 20 V the Zener diode will turn on as shown in Fig. 2.105a and the voltage across the system will lock in at 20 V. Further increases in the applied voltage will simply appear across the series resistor with the voltage across the system and the forward-biased diode remaining fixed at 20 V and 0.7 V, respectively. The voltage across the system is fixed at 20 V, as shown in Fig. 2.105a, because the 0.7 V of the diode is not between the defined output terminals. The system is therefore safe from any further increases in applied voltage.

For the negative region of the applied signal the silicon diode is reverse biased and presents an open circuit to the series combination of elements. The result is that the full

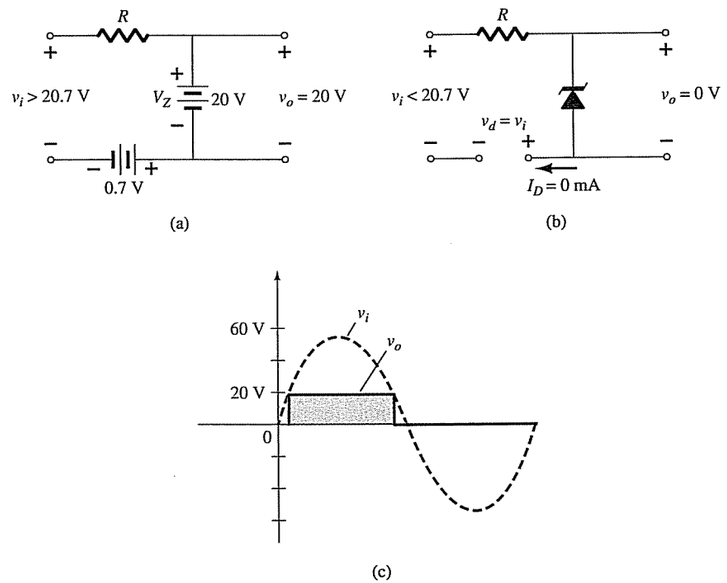


FIG. 2.105
Response of the network of Fig. 2.104 to the application of a 60-V sinusoidal signal.

negatively applied signal will appear across the open-circuited diode and the negative voltage across the system locked in at 0 V, as shown in Fig. 2.104b.

The voltage across the system will therefore appear as shown in Fig. 2.105c.

The use of the Zener diode as a regulator is so common that three conditions surrounding the analysis of the basic Zener regulator are considered. The analysis provides an excellent opportunity to become better acquainted with the response of the Zener diode to different operating conditions. The basic configuration appears in Fig. 2.106. The analysis is first for fixed quantities, followed by a fixed supply voltage and a variable load, and finally a fixed load and a variable supply.

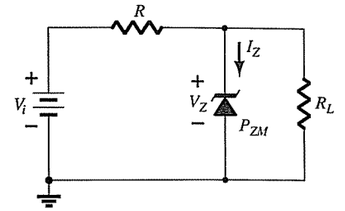


FIG. 2.106
Basic Zener regulator.

V_i and R Fixed

The simplest of Zener diode regulator networks appears in Fig. 2.106. The applied dc voltage is fixed, as is the load resistor. The analysis can fundamentally be broken down into two steps.

1. ***Determine the state of the Zener diode by removing it from the network and calculating the voltage across the resulting open circuit.***

Applying step 1 to the network of Fig. 2.106 results in the network of Fig. 2.107, where an application of the voltage divider rule results in

$$V = V_L = \frac{R_L V_i}{R + R_L} \tag{2.16}$$

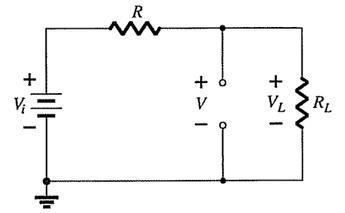


FIG. 2.107
Determining the state of the Zener diode.

If $V \geq V_Z$, the Zener diode is on, and the appropriate equivalent model can be substituted.
If $V < V_Z$, the diode is off, and the open-circuit equivalence is substituted.

2. ***Substitute the appropriate equivalent circuit and solve for the desired unknowns.***

For the network of Fig. 2.106, the "on" state will result in the equivalent network of Fig. 2.108. Since voltages across parallel elements must be the same, we find that

$$V_L = V_Z \tag{2.17}$$

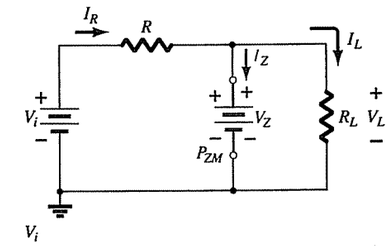


FIG. 2.108
Substituting the Zener equivalent for the "on" situation.

The Zener diode current must be determined by an application of Kirchhoff's current law. That is,

$$I_R = I_Z + I_L$$

and

$$I_Z = I_R - I_L \tag{2.18}$$

where

$$I_L = \frac{V_L}{R_L} \quad \text{and} \quad I_R = \frac{V_R}{R} = \frac{V_i - V_L}{R}$$

The power dissipated by the Zener diode is determined by

$$P_Z = V_Z I_Z \tag{2.19}$$

that must be less than the P_{ZM} specified for the device.

Before continuing, it is particularly important to realize that the first step was employed only to determine the *state of the Zener diode.* If the Zener diode is in the "on" state, the voltage across the diode is not V volts. When the system is turned on, the Zener diode will turn on as soon as the voltage across the Zener diode is V_Z volts. It will then "lock in" at this level and never reach the higher level of V volts.



EXAMPLE 2.26

a. For the Zener diode network of Fig. 2.109, determine V_L, V_R, I_Z, and P_Z.
b. Repeat part (a) with $R_L = 3\,\text{k}\Omega$.

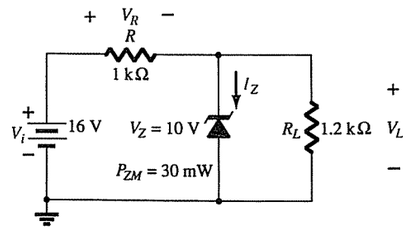


FIG. 2.109
Zener diode regulator for Example 2.26.

Solution:

a. Following the suggested procedure, we redraw the network as shown in Fig. 2.110.

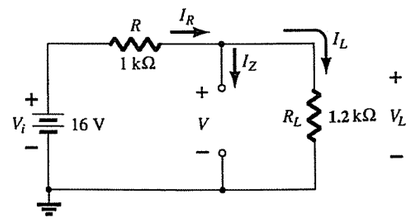


FIG. 2.110
Determining V for the regulator of Fig. 2.109.

Applying Eq. (2.16) gives

$$V = \frac{R_L V_i}{R + R_L} = \frac{1.2\,\text{k}\Omega(16\,\text{V})}{1\,\text{k}\Omega + 1.2\,\text{k}\Omega} = 8.73\,\text{V}$$

Since $V = 8.73$ V is less than $V_Z = 10$ V, the diode is in the "off" state, as shown on the characteristics of Fig. 2.111. Substituting the open-circuit equivalent results in the same network as in Fig. 2.110, where we find that

$$V_L = V = \mathbf{8.73\,V}$$
$$V_R = V_i - V_L = 16\,\text{V} - 8.73\,\text{V} = \mathbf{7.27\,V}$$
$$I_Z = \mathbf{0\,A}$$

and $$P_Z = V_Z I_Z = V_Z(0\,\text{A}) = \mathbf{0\,W}$$

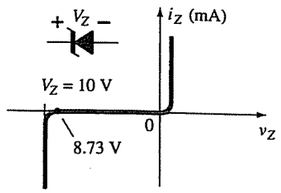


FIG. 2.111
Resulting operating point for the network of Fig. 2.109.

b. Applying Eq. (2.16) results in

$$V = \frac{R_L V_i}{R + R_L} = \\frac{3\,\text{k}\Omega(16\,\text{V})}{1\,\text{k}\Omega + 3\,\text{k}\Omega} = 12\,\text{V}$$

Since $V = 12$ V is greater than $V_Z = 10$ V, the diode is in the "on" state and the network of Fig. 2.112 results. Applying Eq. (2.17) yields

$$V_L = V_Z = \mathbf{10\,V}$$

and $$V_R = V_i - V_L = 16\,\text{V} - 10\,\text{V} = \mathbf{6\,V}$$

with $$I_L = \frac{V_L}{R_L} = \frac{10\,\text{V}}{3\,\text{k}\Omega} = 3.33\,\text{mA}$$

and $$I_R = \frac{V_R}{R} = \frac{6\,\text{V}}{1\,\text{k}\Omega} = 6\,\text{mA}$$

so that $$I_Z = I_R - I_L\,[\text{Eq. (2.18)}]$$
$$= 6\,\text{mA} - 3.33\,\text{mA}$$
$$= \mathbf{2.67\,mA}$$

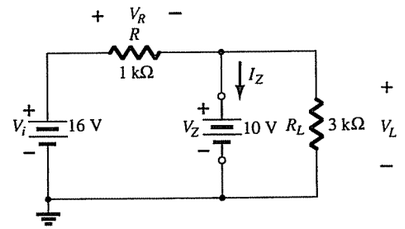


FIG. 2.112
Network of Fig. 2.109 in the "on" state.

The power dissipated is

$$P_Z = V_Z I_Z = (10\,\text{V})(2.67\,\text{mA}) = \mathbf{26.7\,mW}$$

which is less than the specified $P_{ZM} = 30$ mW.

Fixed V_i, Variable R_L

Due to the offset voltage V_Z, there is a specific range of resistor values (and therefore load current) that will ensure that the Zener is in the "on" state. Too small a load resistance R_L will result in a voltage V_L across the load resistor less than V_Z, and the Zener device will be in the "off" state.

To determine the minimum load resistance of Fig. 2.106 that will turn the Zener diode on, simply calculate the value of R_L that will result in a load voltage $V_L = V_Z$. That is,

$$V_L = V_Z = \frac{R_L V_i}{R_L + R}$$

Solving for R_L, we have

$$R_{L_{\text{min}}} = \frac{RV_Z}{V_i - V_Z} \tag{2.20}$$

Any load resistance value greater than the R_L obtained from Eq. (2.20) will ensure that the Zener diode is in the "on" state and the diode can be replaced by its V_Z source equivalent.

The condition defined by Eq. (2.20) establishes the minimum R_L, but in turn specifies the maximum I_L as

$$I_{L_{\text{max}}} = \frac{V_L}{R_L} = \frac{V_Z}{R_{L_{\text{min}}}} \tag{2.21}$$

Once the diode is in the "on" state, the voltage across R remains fixed at

$$V_R = V_i - V_Z \tag{2.22}$$

and I_R remains fixed at

$$I_R = \frac{V_R}{R} \tag{2.23}$$

The Zener current

$$I_Z = I_R - I_L \tag{2.24}$$

resulting in a minimum I_Z when I_L is a maximum and a maximum I_Z when I_L is a minimum value, since I_R is constant.

Since I_Z is limited to I_{ZM} as provided on the data sheet, it does affect the range of R_L and therefore I_L. Substituting I_{ZM} for I_Z establishes the minimum I_L as

$$I_{L_{min}} = I_R - I_{ZM} \tag{2.25}$$

and the maximum load resistance as

$$R_{L_{max}} = \frac{V_Z}{I_{L_{min}}} \tag{2.26}$$

EXAMPLE 2.27

a. For the network of Fig. 2.113, determine the range of R_L and I_L that will result in V_{RL} being maintained at 10 V.
b. Determine the maximum wattage rating of the diode.

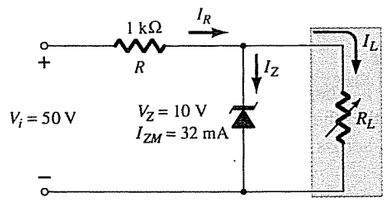


FIG. 2.113
Voltage regulator for Example 2.27.

Solution:

a. To determine the value of R_L that will turn the Zener diode on, apply Eq. (2.20):

$$R_{L_{min}} = \frac{RV_Z}{V_i - V_Z} = \frac{(1\,\text{k}\Omega)(10\,\text{V})}{50\,\text{V} - 10\,\text{V}} = \frac{10\,\text{k}\Omega}{40} = \mathbf{250\ \Omega}$$

The voltage across the resistor R is then determined by Eq. (2.22):

$$V_R = V_i - V_Z = 50\,\text{V} - 10\,\text{V} = \mathbf{40\ V}$$

and Eq. (2.23) provides the magnitude of I_R:

$$I_R = \frac{V_R}{R} = \frac{40\,\text{V}}{1\,\text{k}\Omega} = \mathbf{40\ mA}$$

The minimum level of I_L is then determined by Eq. (2.25):

$$I_{L_{min}} = I_R - I_{ZM} = 40\,\text{mA} - 32\,\text{mA} = \mathbf{8\ mA}$$

with Eq. (2.26) determining the maximum value of R_L:

$$R_{L_{max}} = \frac{V_Z}{I_{L_{min}}} = \frac{10\,\text{V}}{8\,\text{mA}} = \mathbf{1.25\ k\Omega}$$

A plot of V_L versus R_L appears in Fig. 2.114a and for V_L versus I_L in Fig. 2.114b.

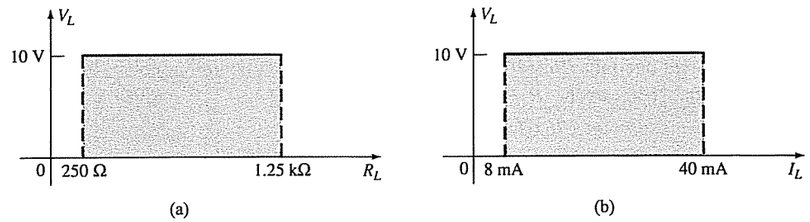


FIG. 2.114
V_L versus R_L and I_L for the regulator of Fig. 2.113.

b. $P_{max} = V_Z I_{ZM}$
$= (10\,\text{V})(32\,\text{mA}) = \mathbf{320\ mW}$

Fixed R_L, Variable V_i

For fixed values of R_L in Fig. 2.106, the voltage V_i must be sufficiently large to turn the Zener diode on. The minimum turn-on voltage $V_i = V_{i_{min}}$ is determined by

$$V_L = V_Z = \frac{R_L V_i}{R_L + R}$$

and

$$V_{i_{min}} = \frac{(R_L + R)V_Z}{R_L} \tag{2.27}$$

The maximum value of V_i is limited by the maximum Zener current I_{ZM}. Since $I_{ZM} = I_R - I_L$,

$$I_{R_{max}} = I_{ZM} + I_L \tag{2.28}$$

Since I_L is fixed at V_Z/R_L and I_{ZM} is the maximum value of I_Z, the maximum V_i is defined by

$$V_{i_{max}} = V_{R_{max}} + V_Z$$

$$V_{i_{max}} = I_{R_{max}} R + V_Z \tag{2.29}$$

EXAMPLE 2.28 Determine the range of values of V_i that will maintain the Zener diode of Fig. 2.115 in the "on" state.

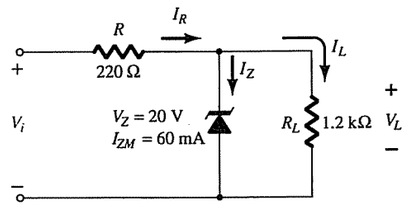


FIG. 2.115
Regulator for Example 2.28.

Solution:

Eq. (2.27):
$$V_{i_{min}} = \frac{(R_L + R)V_Z}{R_L} = \frac{(1200\,\Omega + 220\,\Omega)(20\,\text{V})}{1200\,\Omega} = \mathbf{23.67\ V}$$
$$I_L = \frac{V_L}{R_L} = \frac{V_Z}{R_L} = \frac{20\,\text{V}}{1.2\,\text{k}\Omega} = 16.67\,\text{mA}$$

Eq. (2.28):
$$I_{R_{max}} = I_{ZM} + I_L = 60\,\text{mA} + 16.67\,\text{mA}$$
$$= 76.67\,\text{mA}$$

Eq. (2.29):
$$V_{i_{max}} = I_{R_{max}}R + V_Z$$
$$= (76.67\,\text{mA})(0.22\,\text{k}\Omega) + 20\,\text{V}$$
$$= 16.87\,\text{V} + 20\,\text{V}$$
$$= \mathbf{36.87\ V}$$

A plot of V_L versus V_i is provided in Fig. 2.116.

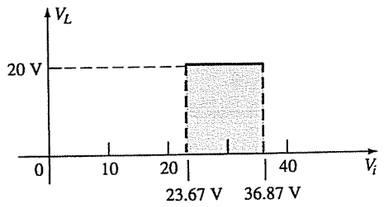


FIG. 2.116
V_L versus V_i for the regulator of Fig. 2.115.

The results of Example 2.28 reveal that for the network of Fig. 2.115 with a fixed R_L, the output voltage will remain fixed at 20 V for a range of input voltage that extends from 23.67 V to 36.87 V.

In fact, the input could appear as shown in Fig. 2.117 and the output would remain constant at 20 V, as shown in Fig. 2.116. The waveform appearing in Fig. 2.117 is obtained by *filtering* a half-wave- or full-wave-rectified output—a process described in detail in a later chapter. The net effect, however, is to establish a steady dc voltage (for a defined range of V_i) such as that shown in Fig. 2.116 from a sinusoidal source with 0 average value.

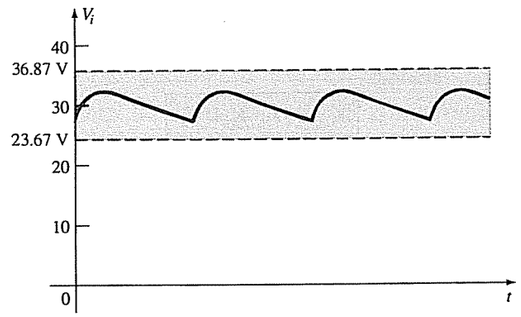


FIG. 2.117
Waveform generated by a filtered rectified signal.

2.11 VOLTAGE-MULTIPLIER CIRCUITS

Voltage-multiplier circuits are employed to maintain a relatively low transformer peak voltage while stepping up the peak output voltage to two, three, four, or more times the peak rectified voltage.

Voltage Doubler

The network of Fig. 2.118 is a half-wave voltage doubler. During the positive voltage half-cycle across the transformer, secondary diode D_1 conducts (and diode D_2 is cut off), charging capacitor C_1 up to the peak rectified voltage (V_m). Diode D_1 is ideally a short during this half-cycle, and the input voltage charges capacitor C_1 to V_m with the polarity shown in Fig. 2.119a. During the negative half-cycle of the secondary voltage, diode D_1 is cut off and diode D_2 conducts charging capacitor C_2. Since diode D_2 acts as a short during the negative half-cycle (and diode D_1 is open), we can sum the voltages around the outside loop (see Fig. 2.119b):

$$-V_m - V_{C_1} + V_{C_2} = 0$$
$$-V_m - V_m + V_{C_2} = 0$$

from which we obtain

$$V_{C_2} = 2V_m$$

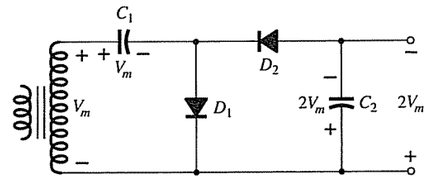


FIG. 2.118
Half-wave voltage doubler.

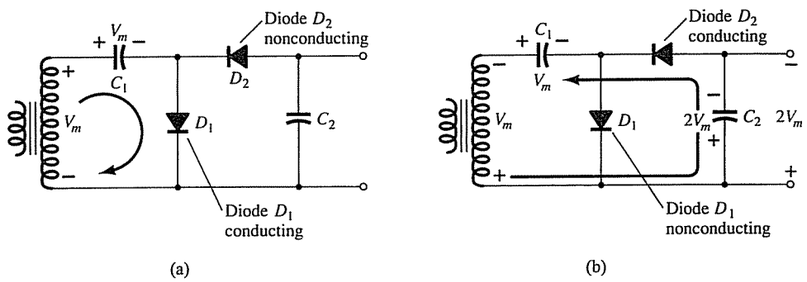


FIG. 2.119
Double operation, showing each half-cycle of operation: (a) positive half-cycle; (b) negative half-cycle.

On the next positive half-cycle, diode D_2 is nonconducting and capacitor C_2 will discharge through the load. If no load is connected across capacitor C_2, both capacitors stay charged—C_1 to V_m and C_2 to $2V_m$. If, as would be expected, there is a load connected to the output of the voltage doubler, the voltage across capacitor C_2 drops during the positive half-cycle (at the input) and the capacitor is recharged up to $2V_m$ during the negative half-cycle. The output waveform across capacitor C_2 is that of a half-wave signal filtered by a capacitor filter. The peak inverse voltage across each diode is $2V_m$.

Another doubler circuit is the full-wave doubler of Fig. 2.120. During the positive half-cycle of transformer secondary voltage (see Fig. 2.121a) diode D_1 conducts, charging capacitor C_1 to a peak voltage V_m. Diode D_2 is nonconducting at this time.

During the negative half-cycle (see Fig. 2.121b) diode D_2 conducts, charging capacitor C_2, while diode D_1 is nonconducting. If no load current is drawn from the circuit, the voltage across capacitors C_1 and C_2 is $2V_m$. If load current is drawn from the circuit, the voltage across capacitors C_1 and C_2 is the same as that across a capacitor fed by a full-wave rectifier circuit. One difference is that the effective capacitance is that of C_1 and C_2 in series, which is less than the capacitance of either C_1 or C_2 alone. The lower capacitor value will provide poorer filtering action than the single-capacitor filter circuit.

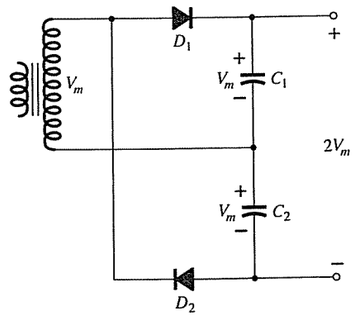


FIG. 2.120
Full-wave voltage doubler.

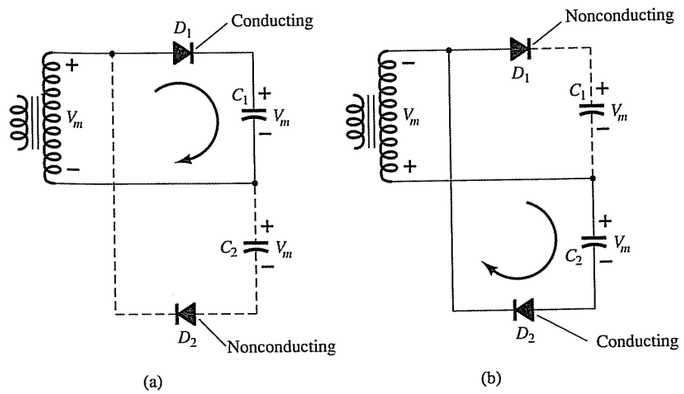


FIG. 2.121
Alternate half-cycles of operation for full-wave voltage doubler.

The peak inverse voltage across each diode is $2V_m$, as it is for the filter capacitor circuit. In summary, the half-wave or full-wave voltage-doubler circuits provide twice the peak voltage of the transformer secondary while requiring no center-tapped transformer and only $2V_m$ PIV rating for the diodes.

Voltage Tripler and Quadrupler

Figure 2.122 shows an extension of the half-wave voltage doubler, which develops three and four times the peak input voltage. It should be obvious from the pattern of the circuit

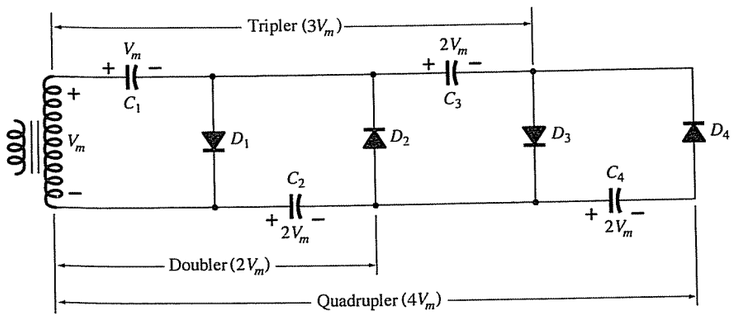


FIG. 2.122
Voltage tripler and quadrupler.

connection how additional diodes and capacitors may be connected so that the output voltage may also be five, six, seven, and so on, times the basic peak voltage (V_m).

In operation, capacitor C_1 charges through diode D_1 to a peak voltage V_m during the positive half-cycle of the transformer secondary voltage. Capacitor C_2 charges to twice the peak voltage, $2V_m$, developed by the sum of the voltages across capacitor C_1 and the transformer during the negative half-cycle of the transformer secondary voltage.

During the positive half-cycle, diode D_3 conducts and the voltage across capacitor C_2 charges capacitor C_3 to the same $2V_m$ peak voltage. On the negative half-cycle, diodes D_2 and D_4 conduct with capacitor C_3, charging C_4 to $2V_m$.

The voltage across capacitor C_2 is $2V_m$, across C_1 and C_3 it is $3V_m$, and across C_2 and C_4 it is $4V_m$. If additional sections of diode and capacitor are used, each capacitor will be charged to $2V_m$. Measuring from the top of the transformer winding (Fig. 2.122) will provide odd multiples of V_m at the output, whereas measuring the output voltage from the bottom of the transformer will provide even multiples of the peak voltage V_m.

The transformer rating is only V_m, maximum, and each diode in the circuit must be rated at $2V_m$ PIV. If the load is small and the capacitors have little leakage, extremely high dc voltages may be developed by this type of circuit, using many sections to step up the dc voltage.

2.12 PRACTICAL APPLICATIONS

The range of practical applications for diodes is so broad that it would be virtually impossible to consider all the options in one section. However, to develop some feeling for the use of the device in everyday networks, a number of the more common areas of application are introduced below. In particular, note that the use of diodes extends well beyond the important switching characteristic that was introduced earlier in this chapter.

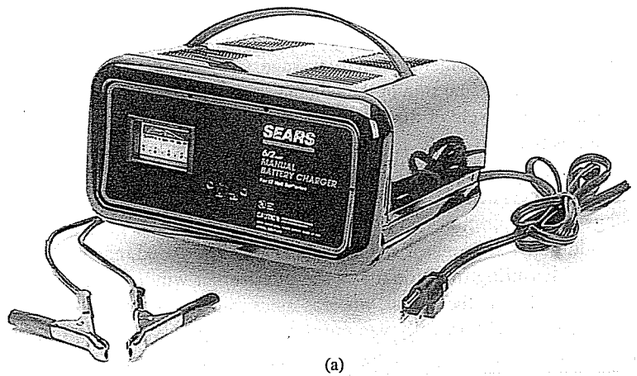
Rectification

Battery chargers are a common household piece of equipment used to charge everything from small flashlight batteries to heavy-duty, marine, lead-acid batteries. Since all are plugged into a 120-V ac outlet such as found in the home, the basic construction of each is quite similar. In every charging system a *transformer* must be included to cut the ac voltage to a level appropriate for the dc level to be established. A *diode* (also called *rectifier*) arrangement must be included to convert the ac voltage, which varies with time, to a fixed dc level such as described in this chapter. Some dc chargers also include a *regulator* to provide an improved dc level (one that varies less with time or load). Since the car battery charger is one of the most common, it will be described in the next few paragraphs.

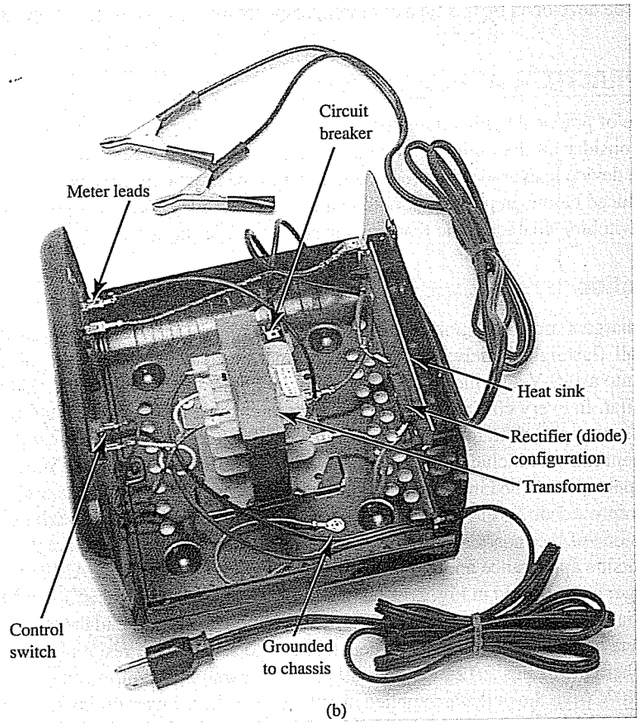
The outside appearance and the internal construction of a Sears 6/2 AMP Manual Battery Charger are provided in Fig. 2.123. Note in Fig. 2.123b that the transformer (as in most chargers) takes up most of the internal space. The additional air space and the holes in the casing are there to ensure an outlet for the heat that develops due to the resulting current levels.

The schematic of Fig. 2.124 includes all the basic components of the charger. Note first that the 120 V from the outlet are applied directly across the primary of the transformer. The charging rate of 6 A or 2 A is determined by the switch, which simply controls how many windings of the primary will be in the circuit for the chosen charging rate. If the battery is charging at the 2-A level, the full primary will be in the circuit, and the ratio of the turns in the primary to the turns in the secondary will be a maximum. If it is charging at the 6-A level, fewer turns of the primary are in the circuit, and the ratio drops. When you study transformers, you will find that the voltage at the primary and secondary is directly related to the *turns ratio*. If the ratio from primary to secondary drops, then the voltage drops also. The reverse effect occurs if the turns on the secondary exceed those on the primary.

The general appearance of the waveforms appears in Fig. 2.124 for the 6-A charging level. Note that so far, the ac voltage has the same wave shape across the primary and the secondary. The only difference is in the peak value of the waveforms. Now the diodes take over and convert the ac waveform, which has zero average value (the waveform above equals the waveform below), to one that has an average value (all above the axis) as shown in the same figure. For the moment simply recognize that diodes are semiconductor electronic devices that permit only conventional current to flow through them in the direction indicated by the arrow in the symbol. Even though the waveform resulting from the diode



(a)



(b)

FIG. 2.123
Battery charger: (a) external appearance; (b) internal construction.

action has a pulsing appearance with a peak value of about 18 V, it will charge the 12-V battery whenever its voltage is greater than that of the battery, as shown by the shaded area. Below the 12-V level the battery cannot discharge back into the charging network because the diodes permit current flow in only one direction.

In particular, note in Fig. 2.123b the large plate that carries the current from the rectifier (diode) configuration to the positive terminal of the battery. Its primary purpose is to provide a *heat sink* (a place for the heat to be distributed to the surrounding air) for the diode configuration. Otherwise the diodes would eventually melt down and self-destruct due to the resulting current levels. Each component of Fig. 2.124 has been carefully labeled in Fig. 2.123b for reference.

When current is first applied to a battery at the 6-A charge rate, the current demand, as indicated by the meter on the face of the instrument, may rise to 7 A or almost 8 A. However,

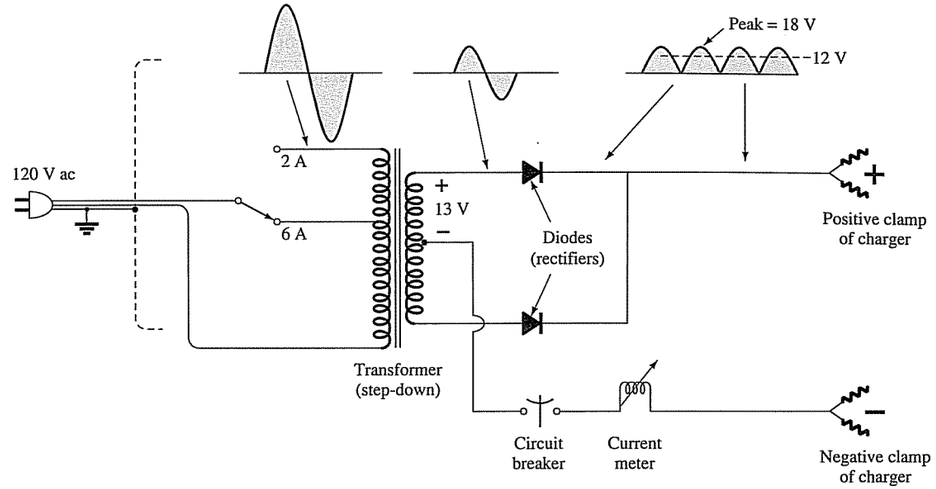


FIG. 2.124
Electrical schematic for the battery charger of Fig. 2.123.

the level of current will decrease as the battery charges until it drops to a level of 2 A or 3 A. For units such as this that do not have an automatic shutoff, it is important to disconnect the charger when the current drops to the fully charged level; otherwise, the battery will become overcharged and may be damaged. A battery that is at its 50% level can take as long as 10 hours to charge, so one should not expect it to be a 10-minute operation. In addition, if a battery is in very bad shape, with a lower than normal voltage, the initial charging current may be too high for the design. To protect against such situations, the circuit breaker will open and stop the charging process. Because of the high current levels, it is important that the directions provided with the charger be carefully read and applied.

In an effort to compare the theoretical world with the real world, a load (in the form of a headlight) was applied to the charger to permit a viewing of the actual output waveform. It is important to note and remember that **a diode with zero current through it will not display its rectifying capabilities**. In other words, the output from the charger of Fig. 2.123 will not be a rectified signal unless a load is applied to the system to draw current through the diode. Recall from the diode characteristics that when $I_D = 0$ A, $V_D = 0$ V.

By applying the headlamp as a load, however, sufficient current is drawn through the diode for it to behave like a switch and convert the ac waveform to a pulsating one as shown in Fig. 2.125 for the 6-A setting. First note that the waveform is slightly distorted by the nonlinear characteristics of the transformer and the nonlinear characteristics of the diode at low currents. The waveform, however, is certainly close to what is expected when we compare it to the theoretical patterns of Fig. 2.123. The peak value is determined from the vertical sensitivity as

$$V_{\text{peak}} = (3.3 \text{ divisions})(5 \text{ V/division}) = 16.5 \text{ V}$$

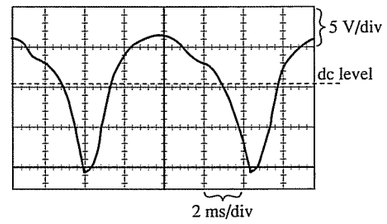


FIG. 2.125
Pulsating response of the charger of Fig. 2.124 to the application of a headlamp as a load.

with a dc level of

$$V_{dc} = 0.636V_{peak} = 0.636(16.5\text{ V}) = 10.49\text{ V}$$

A dc meter connected across the load registered 10.41 V, which is very close to the theoretical average (dc) level of 10.49 V.

One may wonder how a charger having a dc level of 10.49 V can charge a 12-V battery to a typical level of 14 V. It is simply a matter of realizing that (as shown in Fig. 2.125) for a good deal of each pulse, the voltage across the battery will be greater than 12 V and the battery will be charging—a process referred to as **trickle charging**. In other words, charging does not occur during the entire cycle, but only when the charging voltage is more than the voltage of the battery.

Protective Configurations

Diodes are used in a variety of ways to protect elements and systems from excessive voltages or currents, polarity reversals, arcing, and shorting, to name a few. In Fig. 2.126a, the switch on a simple *RL* circuit has been closed, and the current will rise to a level determined by the applied voltage and series resistor R as shown on the plot. Problems arise when the switch is quickly opened as in Fig. 2.126b to essentially tell the circuit that the current must drop to zero almost instantaneously. You will remember from your basic circuits courses, however, that the inductor will not permit an instantaneous change in current through the coil. A conflict results, which will establish arcing across the contacts of the switch as the coil tries to find a path for discharge. Recall also that the voltage across an inductor is directly related to the rate of change in current through the coil ($v_L = L\,di_L/dt$). When the switch is opened, it is trying to dictate that the current change almost instantaneously, causing a very high voltage to develop across the coil that will then appear across the contacts to establish this arcing current. Levels in the thousands of volts will develop across the contacts, which will soon, if not immediately, damage the contacts and thereby the switch. The effect is referred to as an "inductive kick." Note also that the polarity of the voltage across the coil during the "build-up" phase is opposite to that during the "release" phase. This is due to the fact that the current must maintain the same direction before and after the switch is opened. During the "build-up" phase, the coil appears as a load, whereas during the release phase, it has the characteristics of a source. In general, therefore, always keep in mind that

Trying to change the current through an inductive element too quickly may result in an inductive kick that could damage surrounding elements or the system itself.

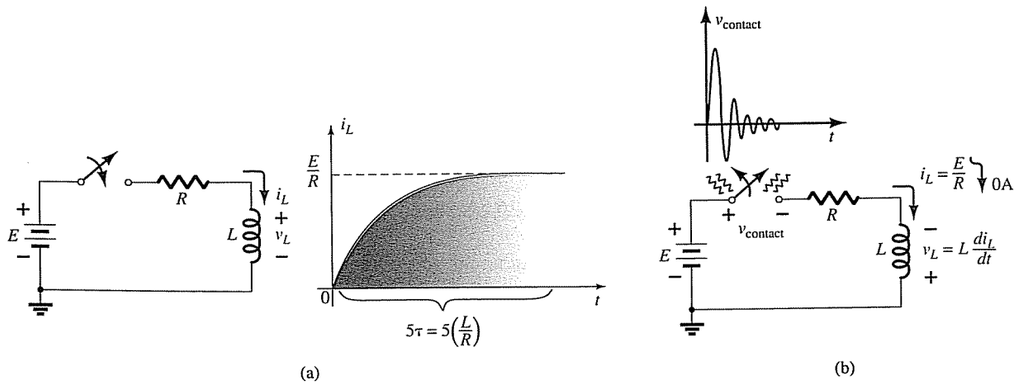


FIG. 2.126

(a) Transient phase of a simple RL circuit; (b) arcing that results across a switch when opened in series with an RL circuit.

In Fig. 2.127a the simple network above may be controlling the action of a relay. When the switch is closed, the coil will be energized, and steady-state current levels will be established. However, when the switch is opened to deenergize the network, we have the

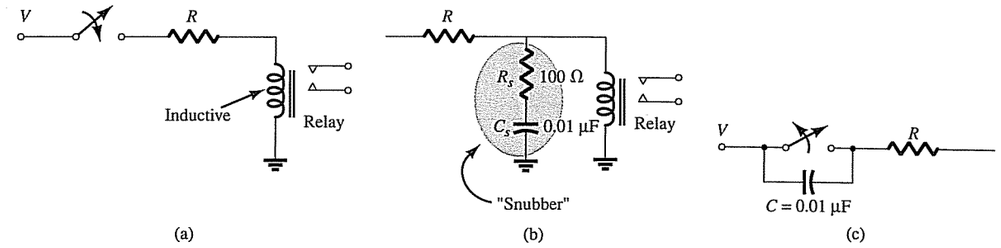


FIG. 2.127

(a) Inductive characteristics of a relay; (b) snubber protection for the configuration of part (a); (c) capacitive protection for a switch.

problem introduced above because the electromagnet controlling the relay action will appear as a coil to the energizing network. One of the cheapest but most effective ways to protect the switching system is to place a capacitor (called a "snubber") across the terminals of the coil. When the switch is opened, the capacitor will initially appear as a short to the coil and will provide a current path that will bypass the dc supply and switch. The capacitor has the characteristics of a short (very low resistance) because of the high-frequency characteristics of the surge voltage, as shown in Fig. 2.126b. Recall that the reactance of a capacitor is determined by $X_C = 1/2\pi fC$, so the higher the frequency, the less is the resistance. Normally, because of the high surge voltages and relatively low cost, ceramic capacitors of about 0.01 μF are used. You don't want to use large capacitors because the voltage across the capacitor will build up too slowly and will essentially slow down the performance of the system. The resistor of 100 Ω in series with the capacitor is introduced solely to limit the surge current that will result when a change in state is called for. Often, the resistor does not appear because of the internal resistance of the coil as established by many turns of fine wire. On occasion, you may find the capacitor across the switch as shown in Fig. 2.127c. In this case, the shorting characteristics of the capacitor at high frequencies will bypass the contacts with the switch and extend its life. Recall that the voltage across a capacitor cannot change instantaneously. In general, therefore,

Capacitors in parallel with inductive elements or across switches are often there to act as protective elements, not as typical network capacitive elements.

Finally, the diode is often used as a protective device for situations such as above. In Fig. 2.128, a diode has been placed in parallel with the inductive element of the relay configuration. When the switch is opened or the voltage source quickly disengaged, the polarity of the voltage across the coil is such as to turn the diode on and conduct in the direction indicated. The inductor now has a conduction path through the diode rather than through the supply and switch, thereby saving both. Since the current established through the coil must now switch directly to the diode, the diode must be able to carry **the same level of current** that was passing through the coil before the switch was opened. The rate at which the current collapses will be controlled by the resistance of the coil and the diode. It can be reduced by placing an additional resistor in series with the diode. The advantage of the diode configuration over that of the snubber is that the diode reaction and behavior are not frequency dependent. However, the protection offered by the diode will not work if the applied voltage is an alternating one such as ac or a square wave since the diode will conduct for one of the applied polarities. For such alternating systems, the "snubber" arrangement would be the best option.

In the next chapter we will find that the base-to-emitter junction of a transistor is forward-biased. That is, the voltage V_{BE} of Fig. 2.129a will be about 0.7 V positive. To prevent a situation where the emitter terminal would be made more positive than the base terminal by a voltage that could damage the transistor, the diode shown in Fig. 2.129a is added. The diode will prevent the reverse-bias voltage V_{EB} from exceeding 0.7 V. On occasion, you may also find a diode in series with the collector terminal of a transistor as shown in Fig. 2.129b. Normal transistor action requires that the collector be more positive than the base or emitter terminal to establish a collector current in the direction shown. However, if a situation arises where the emitter or base terminal is at a higher potential

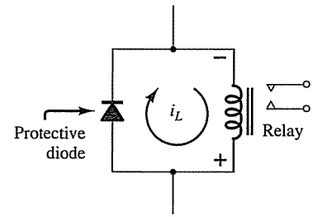


FIG. 2.128

Diode protection for an RL circuit.

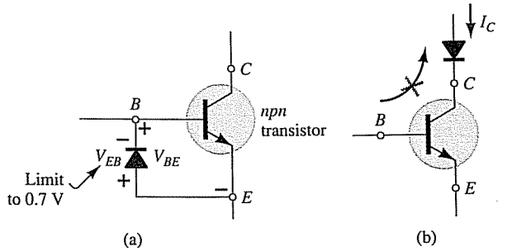


FIG. 2.129
(a) Diode protection to limit the emitter-to-base voltage of a transistor; (b) diode protection to prevent a reversal in collector current.

than the collector terminal, the diode will prevent conduction in the opposite direction. In general, therefore,

Diodes are often used to prevent the voltage between two points from exceeding 0.7 V or to prevent conduction in a particular direction.

As shown in Fig. 2.130, diodes are often used at the input terminals of systems such as op-amps to limit the swing of the applied voltage. For the 400-mV level the signal will pass undisturbed to the input terminals of the op-amp. However, if the voltage jumps to a level of 1 V, the top and bottom peaks will be clipped off before appearing at the input terminals of the op-amp. Any clipped-off voltage will appear across the series resistor R_1.

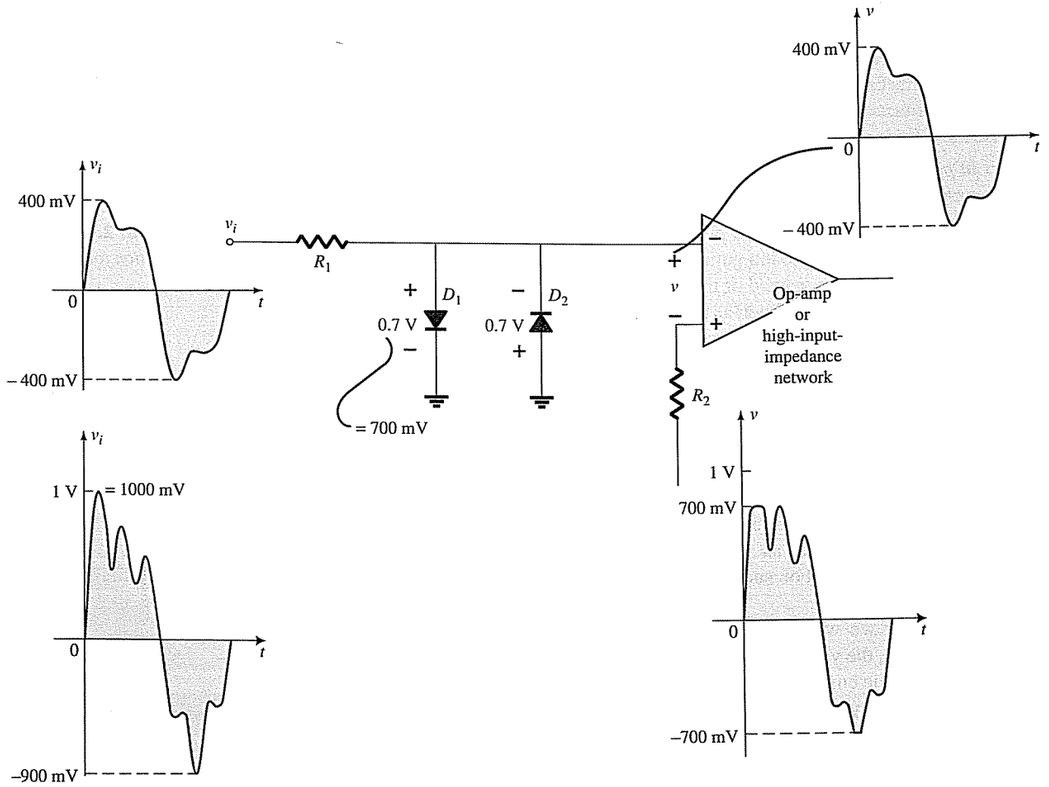


FIG. 2.130
Diode control of the input swing to an op-amp or a high-input-impedance network.

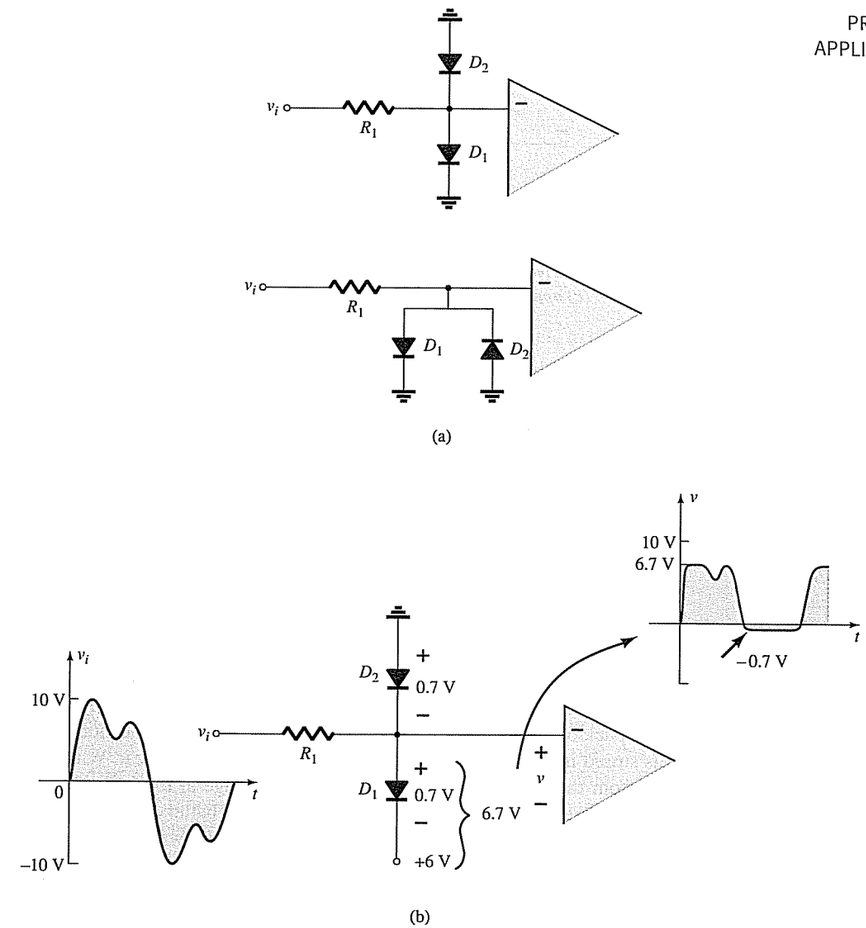


FIG. 2.131
(a) Alternate appearances for the network of Fig. 2.130; (b) establishing random levels of control with separate dc supplies.

The controlling diodes of Fig. 2.130 may also be drawn as shown in Fig. 2.131 to control the signal appearing at the input terminals of the op-amp. In this example, the diodes are acting more like shaping elements than as limiters as in Fig. 2.130. However, the point is that

The placement of elements may change, but their function may still be the same. Do not expect every network to appear exactly as you studied it for the first time.

In general, therefore, don't always assume that diodes are used simply as switches. There is a wide variety of uses for diodes as protective and limiting devices.

Polarity Insurance

There are numerous systems that are very sensitive to the polarity of the applied voltage. For instance, in Fig. 2.132a, assume for the moment that there is a very expensive piece of equipment that would be damaged by an incorrectly applied bias. In Fig. 2.132b the correct applied bias is shown on the left. As a result, the diode is reverse-biased, but the system works just fine—the diode has no effect. However, if the wrong polarity is applied as shown in Fig. 2.132c, the diode will conduct and ensure that no more than 0.7 V will appear across the terminals of the system, protecting it from excessive voltages of the wrong polarity. For

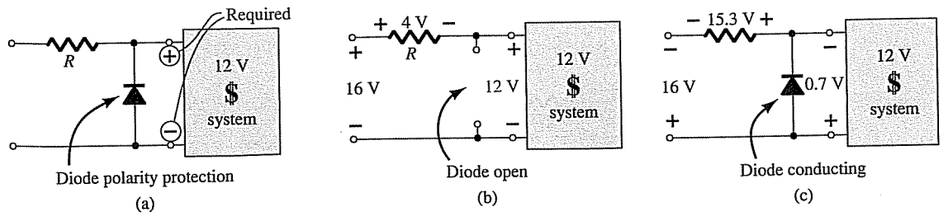


FIG. 2.132

(a) Polarity protection for an expensive, sensitive piece of equipment; (b) correctly applied polarity; (c) application of the wrong polarity.

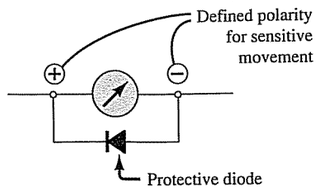


FIG. 2.133

Protection for a sensitive meter movement.

either polarity, the difference between the applied voltage and the load or diode voltage will appear across the series source or network resistance.

In Fig. 2.133 a sensitive measuring movement cannot withstand voltages greater than 1 V of the wrong polarity. With this simple design the sensitive movement is protected from voltages of the wrong polarity of more than 0.7 V.

Controlled Battery-Powered Backup

In numerous situations a system should have a backup power source to ensure that the system will still be operational in case of a loss of power. This is especially true of security systems and lighting systems that must turn on during a power failure. It is also important when a system such as a computer or a radio is disconnected from its ac-to-dc power conversion source to a portable mode for traveling. In Fig. 2.134 the 12-V car radio operating off the 12-V dc power source has a 9-V battery backup system in a small compartment in the back of the radio ready to take over the role of saving the clock mode and the channels stored in memory when the radio is removed from the car. With the full 12 V available from the car, D_1 is conducting, and the voltage at the radio is about 11.3 V. D_2 is reverse-biased (an open circuit), and the reserve 9-V battery inside the radio is disengaged. However, when the radio is removed from the car, D_1 will no longer be conducting because the 12-V source is no longer available to forward-bias the diode. However, D_2 will be forward-biased by the 9-V battery, and the radio will continue to receive about 8.3 V to maintain the memory that has been set for components such as the clock and the channel selections.

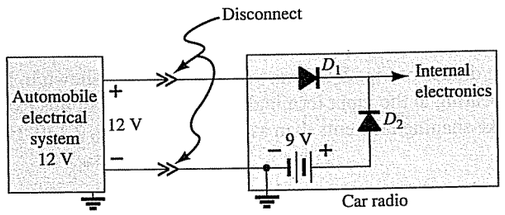


FIG. 2.134

Backup system designed to prevent the loss of memory in a car radio when the radio is removed from the car.

Polarity Detector

Through the use of LEDs of different colors, the simple network of Fig. 2.135 can be used to check the polarity at any point in a dc network. When the polarity is as indicated for the applied 6 V, the top terminal is positive, D_1 will conduct along with LED1, and a green light will result. Both D_2 and LED2 will be back-biased for the above polarity. However, if the polarity at the input is reversed, D_2 and LED2 will conduct, and a red light will appear, defining the top lead as the lead at the negative potential. It would appear that the network

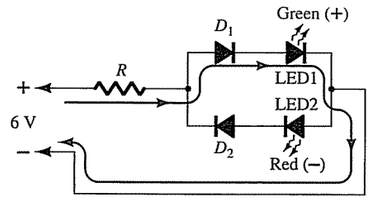


FIG. 2.135

Polarity dector using diodes and LEDs.

would work without diodes D_1 and D_2. However, in general, LEDs do not like to be reverse-biased because of sensitivity built in during the doping process. Diodes D_1 and D_2 offer a series open-circuit condition that provides some protection to the LEDs. In the forward-bias state, the additional diodes D_1 and D_2 reduce the voltage across the LEDs to more common operating levels.

Offering Longer Life and Durability

Some of the primary concerns of using electric light bulbs in exit signs are their limited lifetime (requiring frequent replacement); their sensitivity to heat, fire, and so on; their durability factor when catastrophic accidents occur; and their high voltage and power requirements. For this reason LEDs are often used to provide the longer life span, higher durability levels, and lower demand voltage and power levels (especially when the reserve dc battery system has to take over).

In Fig. 2.136 a control network determines when the EXIT light should be on. When it is on, all the LEDs in series will be on, and the EXIT sign will be fully lit. Obviously, if one of the LEDs should burn out and open up, the entire section will turn off. However, this situation can be improved by simply placing parallel LEDs between every two points. Lose one, and you will still have the other parallel path. Parallel diodes will, of course, reduce the current through each LED, but two at a lower level of current can have a luminescence similar to one at twice the current. Even though the applied voltage is ac, which means that the diodes will turn on and off as the 60-Hz voltage swings positive and negative, the persistence of the LEDs will provide a steady light for the sign.

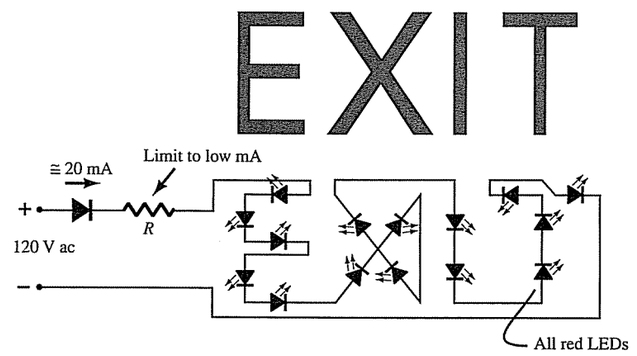


FIG. 2.136

EXIT sign using LEDs.

Setting Voltage Reference Levels

Diodes and Zeners can be used to set reference levels as shown in Fig. 2.137. The network, through the use of two diodes and one Zener diode, is providing three different voltage levels.

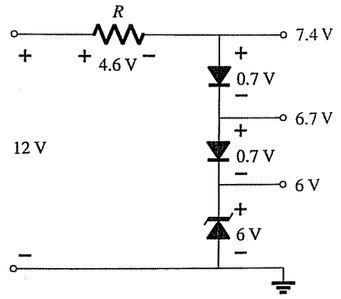


FIG. 2.137

Providing different reference levels using diodes.

Establishing a Voltage Level Insensitive to the Load Current

As an example that clearly demonstrates the difference between a resistor and a diode in a voltage-divider network, consider the situation of Fig. 2.138a, where a load requires about 6 V to operate properly but a 9-V battery is all that is available. For the moment let us assume that operating conditions are such that the load has an internal resistance of 1 kΩ. Using the voltage-divider rule, we can easily determine that the series resistor should be 470 Ω (commercially available value) as shown in Fig. 2.138b. The result is a voltage across the load of 6.1 V, an acceptable situation for most 6-V loads. However, if the operating conditions of the load change and the load now has an internal resistance of only 600 Ω, the load voltage will drop to about 4.9 V, and the system will not operate correctly. This sensitivity to the load resistance can be eliminated by connecting four diodes in series with the load as shown in Fig. 2.138c. When all four diodes conduct, the load voltage will be about 6.2 V, irrespective of the load impedance (within device limits, of course)—the sensitivity to the changing load characteristics has been removed.

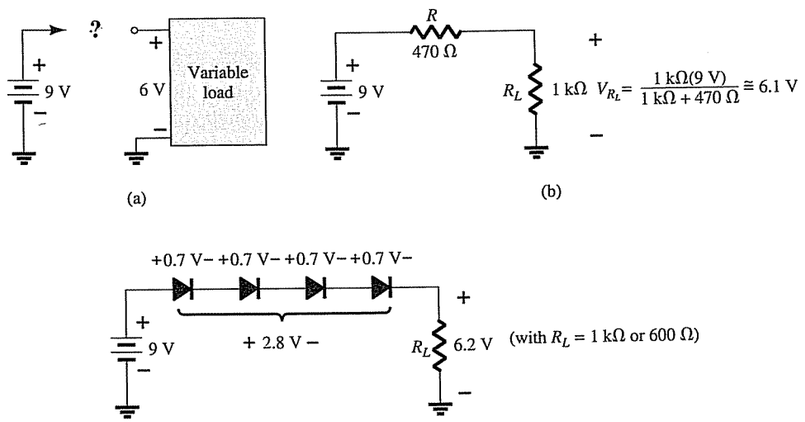


FIG. 2.138
(a) How to drive a 6-V load with a 9-V supply (b) using a fixed resistor value. (c) Using a series combination of diodes.

AC Regulator and Square-Wave Generator

Two back-to-back Zeners can also be used as an ac regulator as shown in Fig. 2.139a. For the sinusoidal signal v_i the circuit will appear as shown in Fig. 2.139b at the instant $v_i = 10$ V. The region of operation for each diode is indicated in the adjoining figure. Note that Z_1 is in a low-impedance region, whereas the impedance of Z_2 is quite large, corresponding to the open-circuit representation. The result is that $v_o = v_i$ when $v_i = 10$ V. The input and the output will continue to duplicate each other until v_i reaches 20 V. Then Z_2 will "turn on" (as a Zener diode), whereas Z_1 will be in a region of conduction with a resistance level sufficiently small compared to the series 5-kΩ resistor to be considered a short circuit. The resulting output for the full range of v_i is provided in Fig. 2.139a. Note that the waveform is not purely sinusoidal, but its root mean square (rms) value is lower than that associated with a full 22-V peak signal. The network is effectively limiting the rms value of the available voltage. The network of Fig. 2.139a can be extended to that of a simple square-wave generator (due to the clipping action) if the signal v_i is increased to perhaps a 50-V peak with 10-V Zeners as shown in Fig. 2.140 with the resulting output waveform.

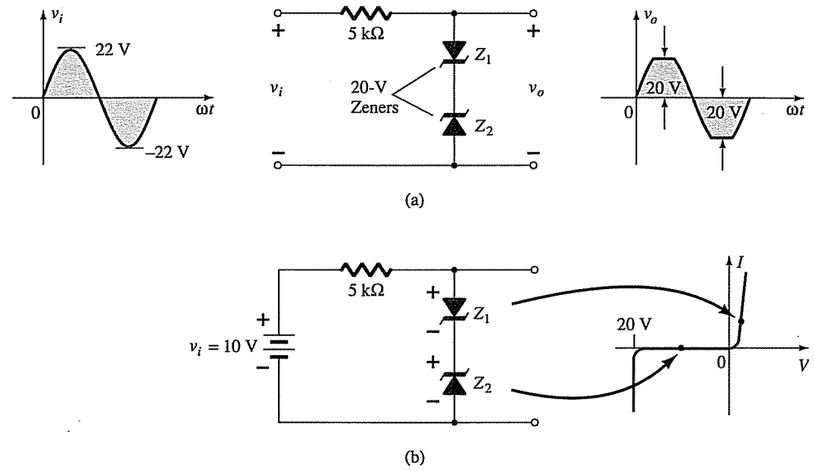


FIG. 2.139
Sinusoidal ac regulation: (a) 40-V peak-to-peak sinusoidal ac regulator; (b) circuit operation at $v_i = 10$ V.

PSpice

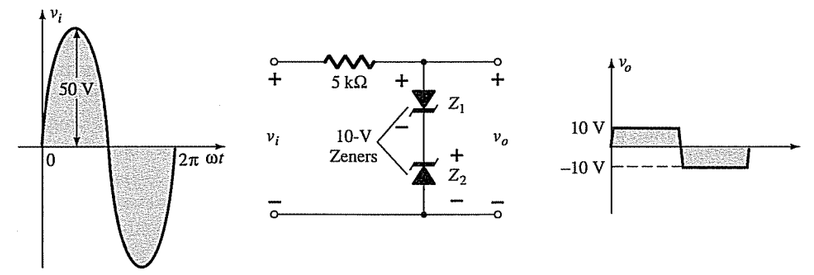


FIG. 2.140
Simple square-wave generator.

2.13 SUMMARY

Important Conclusions and Concepts

1. The characteristics of a device are **unaltered** by the network in which it is employed. The network simply determines the point of operation of the device.
2. The operating point of a network is determined by the **intersection** of the network equation and an equation defining the characteristics of the device.
3. For most applications, the characteristics of a diode can be defined simply by the **threshold voltage in the forward-bias region** and an open circuit for applied voltages less than the threshold value.
4. To determine the state of a diode, simply **think of it initially as a resistor**, and find the polarity of the voltage across it and the direction of conventional current through it. If the voltage across it has a forward-bias polarity and the **current has a direction that matches the arrow in the symbol**, the diode is conducting.
5. To determine the state of diodes used in a logic gate, first make an **educated guess** about the state of the diodes, and then **test your assumptions**. If your estimate is incorrect, refine your guess and try again until the analysis verifies the conclusions.
6. Rectification is a process whereby an applied waveform of **zero average value** is changed to one that **has a dc level**. For applied signals of more than a few volts, the ideal diode approximations can normally be applied.

7. It is very important that the PIV rating of a diode be checked when choosing a diode for a particular application. Simply determine the **maximum voltage** across the diode under **reverse-bias conditions**, and compare it to the nameplate rating. For the typical half-wave and full-wave bridge rectifiers, it is the peak value of the applied signal. For the CT transformer full-wave rectifier, it is twice the peak value (which can get quite high).
8. Clippers are networks that "**clip**" away part of the applied signal either to create a specific type of signal or to limit the voltage that can be applied to a network.
9. Clampers are networks that "**clamp**" the input signal to a different dc level. In any event, the peak-to-peak swing of the applied signal will remain the same.
10. Zener diodes are diodes that make effective use of the **Zener breakdown potential** of an ordinary *p–n* junction characteristic to provide a device of wide importance and application. For Zener conduction, the direction of conventional flow is **opposite to the arrow in the symbol**. The polarity under conduction is also **opposite to that of the conventional diode**.
11. To determine the state of a Zener diode in a dc network, simply remove the Zener from the network, and determine the **open-circuit voltage** between the two points where the Zener diode was originally connected. If it is **more than the Zener potential** and has the correct polarity, the Zener diode is in the "on" state.
12. A half-wave or full-wave voltage doubler employs two capacitors; a tripler, three capacitors; and a quadrupler, four capacitors. In fact, for each, the number of diodes equals the number of capacitors.

Equations

Approximate:

Silicon: $V_K = 0.7\text{ V}$; I_D is determined by network.

Germanium: $V_K = 0.3\text{ V}$; I_D is determined by network.

Gallium arsenide: $V_K = 1.2\text{ V}$; I_D is determined by network.

Ideal:

$$V_K = 0\text{ V}; \qquad I_D \text{ is determined by network.}$$

For conduction:

$$V_D \geq V_K$$

Half-wave rectifier:

$$V_{dc} = 0.318V_m$$

Full-wave rectifier:

$$V_{dc} = 0.636V_m$$

2.14 COMPUTER ANALYSIS

PSpice Windows

Series Diode Configuration In the previous chapter the PSpice folder was established as the location for our projects. This section will define the name of our project, set up the software for the analysis to be performed, describe how to build a simple circuit, and, finally, perform the analysis. The coverage will be quite extensive since this will be the first true exposure to the mechanics associated with using the software package. In the chapters to follow you will find the analysis can be performed quite rapidly to obtain results that confirm the long-hand solutions.

Our first project can now be initiated by double-clicking on the **Orcad Lite Edition** icon on the screen, or you can use the sequence **Start-Programs-Orcad Family Release 9.2 Lite Edition**. The resulting screen has only a few active keys on the top toolbar. The first at the top left is the **Create new document** key (or you can use the sequence **File-New Project**). Selecting the key will result in a **New Project** dialog box, in which the **Name** of the project must be entered. For our purposes we will choose **Bias** (dc levels) as shown in the heading of Fig. 2.141, and select **Analog or Mixed A/D** (to be used for all the analyses of this text). Note at the bottom of the dialog box that the **Location** appears as **C:\PSpice** as set earlier. Click **OK**, and another dialog box will appear titled **Create PSpice Project**. Select **Create a blank**

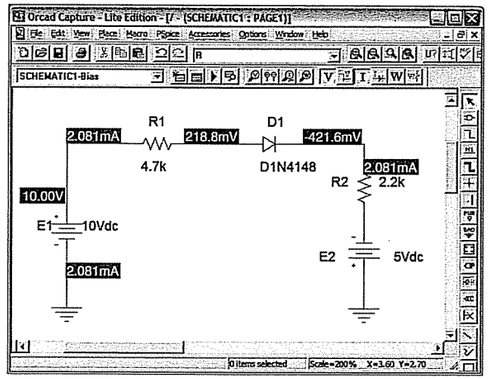


FIG. 2.141

PSpice Windows analysis of a series diode configuration.

project (again, for all the analyses to be performed in this text). Click **OK**, and a third toolbar will appear at the top of the screen with some of the keys enabled. A **Project Manager Window** will appear with **Ohmslaw** as its heading. The new project listing will appear with an icon and an associated + sign in a small square. Clicking on the + sign will take the listing a step further to **SCHEMATIC1**. Click + again (to the left of SCHEMATIC1), and **PAGE1** will appear; clicking on a − sign will reverse the process. Double-clicking on **PAGE1** will create a working window titled **SCHEMATIC1: PAGE1**, revealing that a project can have more than one schematic file and more than one associated page. The width and the height of the window can be adjusted by grabbing an edge to obtain a double-headed arrow and dragging the border to the desired location. Either window on the screen can be moved by clicking on the top heading to make it dark blue and then dragging it to any location.

Now we are ready to build the simple circuit of Fig. 2.141. Select the **Place a part** key (the second key from the top of the toolbar on the right) to obtain the **Place Part** dialog box. Since this is the first circuit to be constructed, we must ensure that the parts appear in the list of active libraries. Select **Add Library-Browse File**, and select **analog.olb**. When it appears under the **File name** heading, select **Open**. Then repeat the process for **eval.olb**, and **source.olb** starting with **Add Library**. All three files will be required to build the networks appearing in this text. However, it is important to realize that:

Once the library files have been selected, they will appear in the active listing for each new project without having to add them each time—a step, such as the* Folder *step above, that does not have to be repeated with each similar project.

Click **OK**, and we can now place components on the screen. For the dc voltage source, first select the **Place a part** key and then select **SOURCE** in the library listing. Under **Part List**, a list of available sources will appear; select **VDC** for this project. Once **VDC** has been selected, its symbol, label, and value will appear on the picture window at the bottom right of the dialog box. Click **OK**, and the **VDC** source will follow the cursor across the screen. Move it to a convenient location, left-click the mouse, and it will be set in place as shown in Fig. 2.141.

Since a second source is present in Fig. 2.141, move the cursor to the general area of the second source and click it in place. Since this is the last source to appear in the network, execute a right click of the mouse and select **End Mode**. Choosing this option will end the procedure, leaving the last source in a red dashed box. The fact that it is red indicates that it is still in the active mode and can be operated on. One more click of the mouse, and the second source will be in place and the red active status removed. The second source can be rotated 180° to match Fig. 2.141 by first clicking the source to make it red (active) and selecting **Rotate**. Since each rotation only turns it 90°, two rotations will be required. The rotations can also be accomplished using the sequence **Ctrl-R**.

One of the most important steps in the procedure is to ensure that a 0-V ground potential is defined for the network so that voltages at any point in the network have a reference point. *The result is a requirement that every network must have a ground defined.* For our purposes, the **0/SOURCE** option will be our choice when the **GND** key is selected. It will

ensure that one side of the source is defined as 0 V. Unfortunately, when the **GND** key is selected, **0/SOURCE** is not listed as an option. This is corrected by selecting **Add Library** in the **Place Ground** dialog box and then choosing **PSpice** followed by **source.olb**. A new library **SOURCE** will now appear in the **Place Ground** library list. When selected, a **0** option will appear. The symbol associated with this choice includes a **0** to indicate that this ground connection will establish the 0-V level for the network. In this way, the voltages displayed at various points of the network will have a reference point.

The next step will be to place the resistors of the network of Fig. 2.141. This is accomplished by selecting the **Place a part** key again and then selecting the **ANALOG** library. Scrolling the options, note that **R** will appear and should be selected. Click **OK**, and the resistor will appear next to the cursor on the screen. Move it to the desired location and click it in place. The second resistor can be placed by simply moving to the general area of its location in Fig. 2.141 and clicking it in place. Since there are only two resistors, the process can be ended by making a right click of the mouse and selecting **End Mode**. The second resistor will have to be rotated to the vertical position using the same procedure described for the second voltage source.

The last element to be placed is the diode. Selecting the **Place a part** keypad will again result in the **Place Part** dialog box, in which the **EVAL** library is chosen from the **Libraries** listing. Then type **D** under **Part** heading and select **D14148** under **Part List** followed by **OK** to place on the screen in the same manner described for the source and resistors.

Now that all the components are on the screen you may want to move them to positions corresponding directly with Fig. 2.141. This is accomplished by simply clicking on the element and holding the left-click down as you move the element.

All the required elements are on the screen, but they need to be connected. This is accomplished by selecting the **Place a wire** key, which looks like a step, in the right toolbar. The result is a crosshair with a center that should be placed at the point to be connected. Place the crosshair at the top of the voltage source, and left-click it once to connect it to that point. Then draw a line to the end of the next element, and click the mouse again when the crosshair is at the correct point. A red line will result with a square at each end to confirm that the connection has been made. Then move the crosshair to the other elements, and build the circuit. Once everything is connected, a right click will provide the **End Mode** option. Don't forget to connect the source to ground as shown in Fig. 2.141.

Now we have all the elements in place, but their labels and values are wrong. To change any parameter, simply double-click on the parameter (the label or the value) to obtain the **Display Properties** dialog box. Type in the correct label or value, click **OK**, and the quantity is changed on the screen. The labels and values can be moved by simply clicking on the center of the parameter until it is closely surrounded by the four small squares and then dragging it to the new location. Another left click, and it is deposited in its new location.

Finally, we can initiate the analysis process, called **Simulation**, by selecting the **Create a new simulation profile** key near the top left of the display—it resembles a data page with a star in the top left corner. A **New Simulation** dialog box will result that first asks for the **Name** of the simulation. **Bias** is entered, and **none** is left in the **Inherit From** request. Then select **Create**, and a **Simulation Setting** dialog box will appear in which **Analysis-Analysis Type-Bias Point** is sequentially selected. Click **OK**, and select the **Run** key (which looks like an isolated blue arrowhead) or choose **PSpice-Run** from the menu bar. An **Output Window** will result that appears to be somewhat inactive. It will not be used in the current analysis, so close (X) the window, and the circuit of Fig. 2.141 will appear with the voltage and current levels of the network. The voltage, current, or power levels can be removed (or replaced) from the display by simply selecting the **V**, **I**, or **W** in the third toolbar from the top. Individual values can be removed by simply selecting the value and pressing the **Delete** key or the scissors key in the top menu bar. Resulting values can be moved by simply left-clicking the value and dragging it to the desired location.

The results of Fig. 2.141 show that the current through the series configuration is 2.081 mA through each element, compared to the 2.072 mA of Example 2.9. The voltage across the diode is 218.8 mV − (−421.6 mV) ≅ 0.64 V, compared to the 0.7 V applied in the long-hand solution of Example 2.9. The voltage across R_1 is 10 V − 0.219 V ≅ 9.78 V, compared to 9.74 V in the long-hand solution. The voltage across the resistor R_2 is 5 V − 0.422 V ≅ 4.58 V, compared to 4.56 V in Example 2.9.

To understand the differences between the two solutions, one must be aware that the diode has internal characteristics that affect its behavior such as the reverse saturation

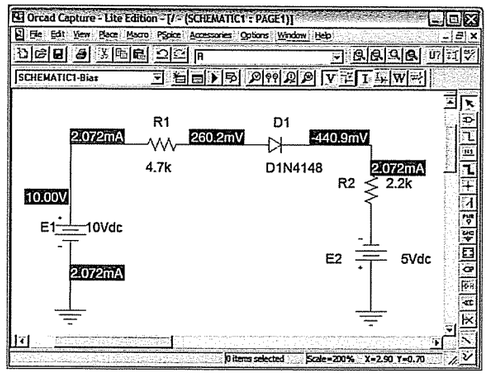


FIG. 2.142

The circuit of Fig. 2.141 reexamined with I_s set at 3.5E-15A.

current and its resistance levels at different current levels. Those characteristics can be viewed through the sequence **Edit-PSpice Model** resulting in the **PSpice Model Editor Lite** dialog box. You will find that the default value of the reverse saturation current is 2.682 nA—a quantity that can have an important effect on the characteristics of the device. If we choose I_s = 3.5E-15A (a value determined by trial and error) and delete the other parameters for the device, a new simulation of the network will result in the response of Fig. 2.142. Now the current through the circuit is 2.072 mA, which is an exact match with the result of Example 2.9. The voltage across the diode is 0.701 V, or essentially 0.7 V, and the voltage across each resistor is exactly as obtained in the long-hand solution. In other words, by choosing this value of reverse saturation current, we created a diode with characteristics that permitted the approximation that V_D = 0.7 V when in the "on" state.

The results can also be viewed in tabulated form by selecting **PSpice** at the head of the screen followed by **View Output File**. The result is the listing of Fig. 2.143 (modified to conserve space), which includes the **CIRCUIT DESCRIPTION** with all the components of the network, the **Diode MODEL PARAMETERS** with the chosen **Is** value, the **SMALL SIGNAL BIAS SOLUTION** with the dc voltage levels, current levels, and total power dissipation, and finally the **OPERATING POINT INFORMATION** for the diode.

The analysis is now complete for the diode circuit of interest. Granted, there was a wealth of information provided to establish and investigate this rather simple network. However, the vast majority of this material will not be repeated in the PSpice examples to follow, which will have a dramatic effect on the length of the descriptions. For practice purposes, it is suggested that other examples in this chapter be checked using PSpice and that the exercises at the end of the chapter be investigated to develop confidence in applying the software package.

Diode Characteristics The characteristics of the D1N4148 diode used in the above analysis will now be obtained using a few maneuvers somewhat more sophisticated than those employed in the first example. The process begins by first building the network of Fig. 2.144 using the procedures just described. Note in particular that the source is labeled **E** and set at **0V** (its initial value). Next the **New Simulation Profile** icon is selected from the toolbar to obtain the **New Simulation** dialog box. For the **Name**, **Fig. 2-145** is entered since it is the location of the graph to be obtained. **Create** is then selected and the **Simulation Settings** dialog box will appear. Under **Analysis Type**, **DC Sweep** is chosen because we want to sweep through a range of values for the source voltage. When **DC Sweep** is selected a list of options will simultaneously appear in the right-hand region of the dialog box, requiring that some choices be made. Since we plan to sweep through a range of voltages, the **Sweep variable** is a **Voltage source**. Its name must be entered as **E** as appearing in Fig. 2.144. The sweep will be **Linear** (equal space between data points) with a **Start value** of 0 V, **End Value** of 10 V, and an **Increment** of 0.01 V. After making all the entries, click **OK** and the **RUN PSpice** option can be selected. The analysis will be performed with the source voltage changing from 0 V to 10 V in 1000 steps (as resulting from the division of 10 V/0.01 V). The result, however, is simply a graph with a horizontal scale from 0 V to 10 V.

```
****     CIRCUIT DESCRIPTION

******************************************************************************

SCHEMATIC1.net
R_R1       N00258 N00288  4.7k
R_R2       N00345 N00315  2.2k
V_E2       0 N00345 5Vdc
V_E1       N00258 0 10Vdc
D_D1       N00288 N00315 D1N4148

****     Diode MODEL PARAMETERS
******************************************************************************

         D1N4148
      IS  3.500000E-15

****     SMALL SIGNAL BIAS SOLUTION       TEMPERATURE =   27.000 DEG C

******************************************************************************

NODE     VOLTAGE
(N00258)  10.0000
(N00288)   .2602
(N00315)  -.4409
(N00345)  -5.0000


VOLTAGE SOURCE CURRENTS

  NAME       CURRENT
  V_E2      -2.072E-03
  V_E1      -2.072E-03

TOTAL POWER DISSIPATION   3.11E-02  WATTS

****     OPERATING POINT INFORMATION      TEMPERATURE =   27.000 DEG C

******************************************************************************

**** DIODES

NAME       D_D1
MODEL      D1N4148
ID         2.07E-03
VD         7.01E-01
REQ        1.25E+01
CAP        0.00E+00
```

FIG. 2.143

Output file for PSpice Windows analysis of the circuit of Fig. 2.142.

Since the plot we want is of I_D versus V_D, we must change the horizontal (x-axis) to V_D. This is accomplished by selecting **Plot** and then **Axis Settings**. An **Axis Settings** dialog box will appear, in which choices have to be made. If **Axis Variables** is selected, an **X-Axis Variable** dialog box will appear with a list of variables that can be chosen for the x-axis. **V1(D1)** will be selected since it represents the voltage across the diode. If we then select **OK**, the **Axis Settings** dialog box will return, where **User Defined** is selected under the

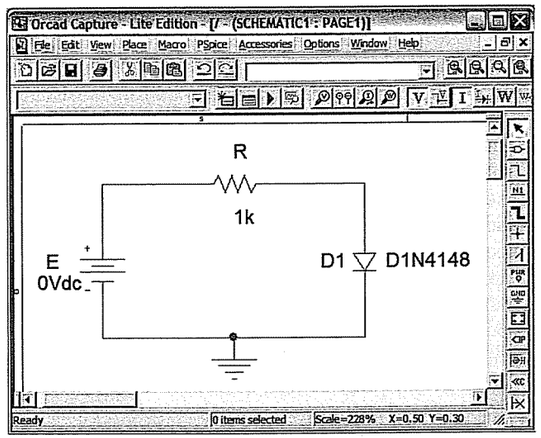


FIG. 2.144

Network for obtaining the characteristics of the D1N4148 diode.

Data Range heading. **User Defined** is chosen because it will allow us to limit the graph to a range of 0 V to 1 V since the "on" voltage of the diode should be around 0.7 V. After entering the 0–1 V range, selecting **OK** will result in a graph with **V1(D1)** as the x variable with a range of 0 V to 1 V. The horizontal axis now seems to be set for the desired plot.

We must now turn our attention to the vertical axis, which should be the diode current. Choosing **Trace** followed by **Add Trace** will result in an **Add Trace** dialog box in which **I(D1)** will appear as one of the possibilities. Selecting **I(D1)** will also cause it to appear as the **Trace Expression** at the bottom of the dialog box. Selecting **OK** will then result in the diode characteristics of Fig. 2.145, clearly showing a steep rise around 0.7 V.

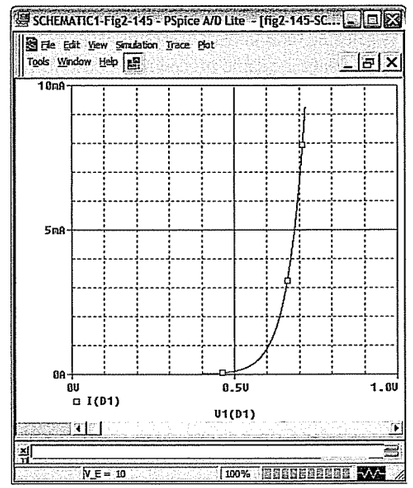


FIG. 2.145

Characteristics of the D1N4148 diode.

If we turn back to the **PSpice Model Editor** for the diode and change I_s to 3.5E-15A as in the previous example, the curve will shift to the right. Similar procedures will be used to obtain the characteristic curves for a variety of elements to be introduced in later chapters.

Multisim 7

The procedure for entering a circuit into Multisim will now be described by checking the results of Example 2.13, which contained two diodes in a series-parallel configuration.

For a network of this type we have two options—to use the "real" list of components represented by the first vertical toolbar or the "virtual" list represented by the second vertical toolbar. Since all the elements of the network are readily available commercial values, the real list will be used. In fact, since the diode is specified, we must use the real option for this component. The resistors and the source could be entered using either approach. Recall that using the virtual list requires that all the parameters of the component be specified, whereas the real list is an actual commercial list from which a component is selected.

The construction begins by placing the voltage source in a convenient place on the screen. This is accomplished by first selecting the top keypad of the first vertical toolbar, which looks like a dc source. When the cursor is placed at the perimeter of the keypad it displays the word **Source**. Selecting this option results in a **Select a Component** dialog box, in which **POWER SOURCES** is selected under the **Family heading**. Under the **Component** heading **DC Power** is selected followed by **OK**, and the supply can be placed anywhere on a screen with a simple left click of the mouse. Of course, it should be placed in a position that will leave room for the remaining components of the circuit. It appears as **V1** with a value of **12V**. Once it is clicked in place the **Select a Component** dialog box disappears.

The resistors are placed by first selecting the resistor symbol, which appears as the second option down in the first vertical toolbar—a keypad titled **BASIC**. When it is selected, a **Select a Component** dialog box again appears, in which **RESISTOR** is selected under the **Family**

listing. For the circuit of interest one of the resistors is 3.3 kΩ, a standard commercial value. Now it is possible to scroll down all the possible values of resistor elements, but this can be a long, tedious process. It is better by far to simply type in 3.3k (no need for the units) in the area just below the **Component** listing, and 3.3kOhm immediately appears at the top of the listing. After selecting this value choose **OK** and the resistor appears on the screen, which can be placed using the same procedure as applied to the source above. It has a 3.3 kΩ value and a label of **R1**. Since this circuit has two resistors, the process has to be repeated for the 5.6 kΩ value, which is also placed in a region of the characteristics that supports the formation of the circuit. It has a value of 5.6 kΩ, but since it is the second resistor placed, it has the label **R2**.

Next, the diodes have to be placed in the correct general area. Returning to the first vertical toolbar, select the diode symbol (third down) to again obtain a **Select a Component** dialog box. Under **Family, DIODE** is selected, and under **Component**, the **1N4009** diode is chosen. An **OK**, and it can also be placed using the same procedure as described above. Since two diodes appear in the configuration, the process has to be repeated until all the elements are in place.

Finally, the ground connection must be established. This is accomplished by returning to the **Source** option; when the **Select a Component** dialog appears, choose **GROUND** under the **Component** heading. An **OK**, and the ground symbol appears on the screen, which can be placed as discussed above.

As demonstrated in Fig. 2.146, a multimeter is used to measure the current through the resistor **R1**. The multimeter option appears at the top of the toolbar to the far right of the screen. When selected it will appear with the heading **XMM1**. Double-clicking the meter will result in the **Multimeter-XMM1** dialog box, in which **A** can be selected to set it as an ammeter. Exit the dialog box and it performs as an ammeter. The current through the diode **D1** is measured with an ammeter obtained from the **Indicator** option appearing as the 10th keypad down in the first vertical toolbar. It looks like number 8 on an IC package. When selected, a **Select a Component** dialog box appears, in which **AMMETER** can be selected under the **Family** heading. Under **Component** there are four options provided to define the orientation of the meter. If **AMMETER H** is selected, the ammeter will appear horizontal with the plus sign on the left. **AMMETER HR** will also result in a horizontal ammeter, but with the plus sign on the right. If **AMMETER V** is selected, the ammeter will be vertical with the plus sign at the top, and if **AMMETER VR** is selected, the ammeter

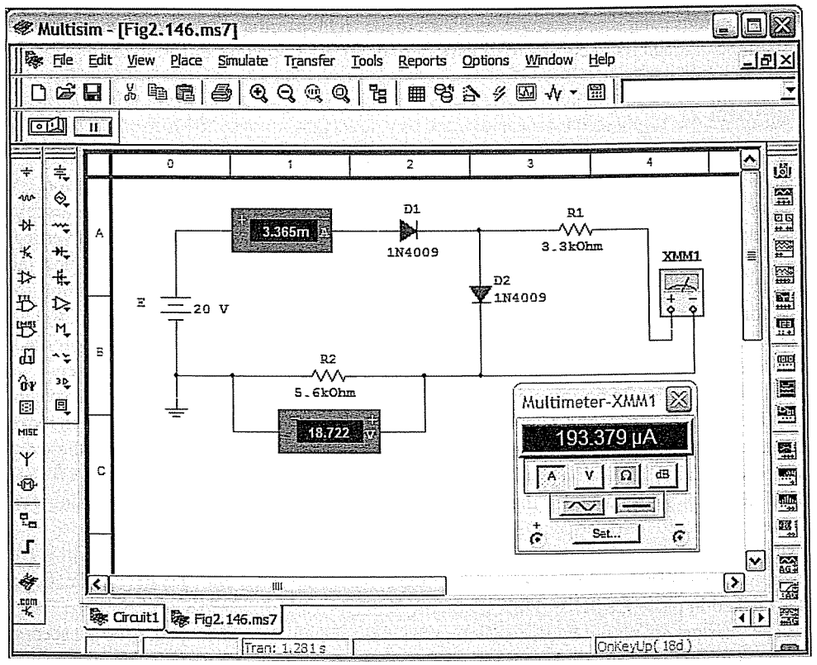


FIG. 2.146
Verifying the results of Example 2.13 using Multisim.

will continue to be vertical, but with the plus sign at the bottom. For our case **AMMETER H** is selected. You will notice a label and other data appearing with the meter when it is placed in the circuit. This can all be removed by double-clicking on the indicator to obtain the **Ammeter** dialog box. Choose **Display** and remove the checks from all the listed possibilities. An **OK**, and the ammeter appears as shown in Fig. 2.146. A voltmeter for the voltage across the resistor **R2** can be obtained from the same **Indicator** option.

Before all the elements are connected they should be moved to the final position. This is accomplished by simply clicking on the element or meter and holding the clicker down; move the element or meter to the desired position. The presence of four small, dark squares around the element and the associated labels will indicate that they are all ready to be operated on.

To move a label or value, simply click on it to create four small squares around the quantity and move it to the desired position, holding the clicker down through the entire operation.

Changing the label **V1** to **E** requires that the label **V1** be double-clicked to obtain the **POWER_SOURCES** dialog box. Select **Label** and type in the new **Reference ID** as **E**. An **OK** and the **E** will appear on the screen. This same procedure can be used to change any of the labels for any of the elements of the circuit.

To change the voltage from **12 V** to **20 V** requires that the value be double-clicked to obtain the **POWER_SOURCES** dialog box again. Under **Value**, the **Voltage(V)** is set at **20 V**. An **OK**, and the **20 V** will appear next to the voltage source on the screen.

Rotation of any of the elements in the clockwise direction is enacted by the sequence **Ctrl-R**. Each rotation will turn the element 90°.

Connecting the elements is accomplished by simply placing the cursor at the end of an element until a small circle and a set of crosshairs appear to designate the starting point. Once in place, click that location and an **x** will appear at that terminal. Then move to the end of the other element and left-click the mouse again—a red connecting wire will automatically appear with the most direct route between the two elements; the process is called **Automatic Wiring**.

Now that all the components are in place it is time to initiate the analysis of the circuit, an operation that can be performed in one of three ways. One option is to select **Simulate** at the head of the screen followed by **Run**. The next is to select the lightning bolt keypad in the horizontal tool bar at the top of the screen having the label **Run/stop simulation**. The last is to simply toggle the switch at the head of the screen to the **1** position. In each case a solution appears in the indicators after a few seconds that seems to flicker over time. This flickering simply indicates the software package is repeating the analysis over time. To accept the solution and stop the continuing simulation, either toggle the switch to the **0** position or select the lightning bolt keypad again.

The current through the diode is 3.365 mA, which compares well with the 3.32 mA in Example 2.13. The voltage across the resistor R_2 is 18.722 V, which is close to the 18.6 V of the same example. After the simulation, the multimeter can be displayed as shown in Fig. 2.146 by double-clicking on the meter symbol. By clicking anywhere on the meter, the top portion is dark blue, and the meter can be moved to any location by simply clicking on the blue region and dragging it to the desired location. The current of 193.379 μA is very close to the 212 μA of Example 2.13. The differences are primarily due to the fact that each diode voltage is assumed to be 0.7 V, whereas in fact it is different for each diode of Fig. 2.146 since the current through each is different. In all, however, the Multisim solution is a very close match with the approximate solution of Example 2.13.

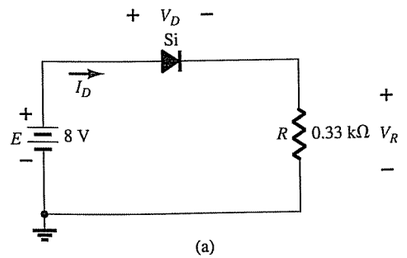
PROBLEMS

**Note:* Asterisks indicate more difficult problems.

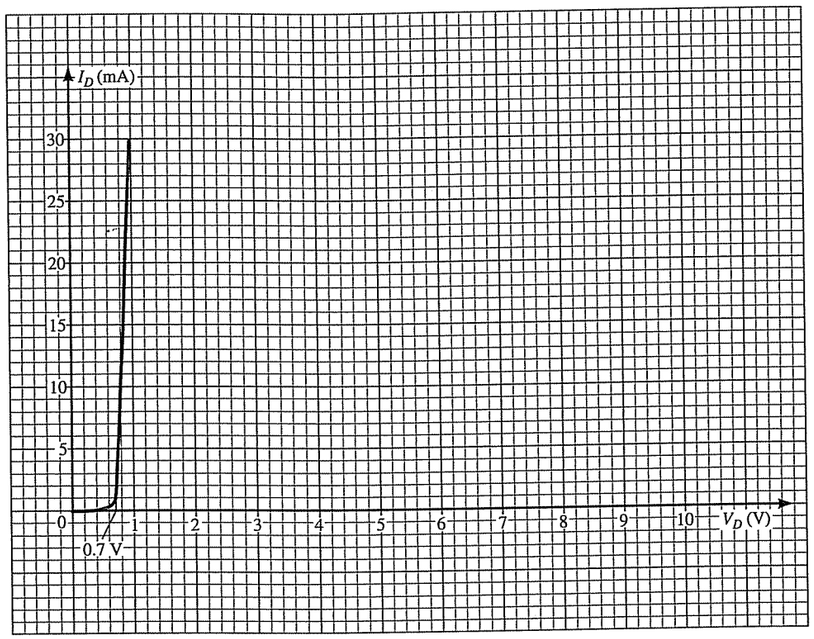
2.2 Load-Line Analysis

1. **a.** Using the characteristics of Fig. 2.147b, determine I_D, V_D, and V_R for the circuit of Fig. 2.147a.
   b. Repeat part (a) using the approximate model for the diode, and compare results.
   c. Repeat part (a) using the ideal model for the diode, and compare results.
2. **a.** Using the characteristics of Fig. 2.147b, determine I_D and V_D for the circuit of Fig. 2.148.
   b. Repeat part (a) with $R = 0.47\,\text{k}\Omega$.
   c. Repeat part (a) with $R = 0.18\,\text{k}\Omega$.
   d. Is the level of V_D relatively close to 0.7 V in each case?

How do the resulting levels of I_D compare? Comment accordingly.



(a)



(b)

FIG. 2.147
Problems 1 and 2.

3. Determine the value of R for the circuit of Fig. 2.148 that will result in a diode current of 10 mA if $E = 7$ V. Use the characteristics of Fig. 2.147b for the diode.

4. **a.** Using the approximate characteristics for the Si diode, determine V_D, I_D, and V_R for the circuit of Fig. 2.149.
   b. Perform the same analysis as part (a) using the ideal model for the diode.
   c. Do the results obtained in parts (a) and (b) suggest that the ideal model can provide a good approximation for the actual response under some conditions?

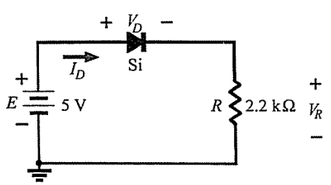


FIG. 2.148
Problems 2 and 3.

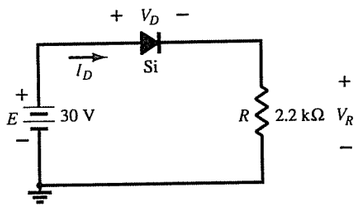
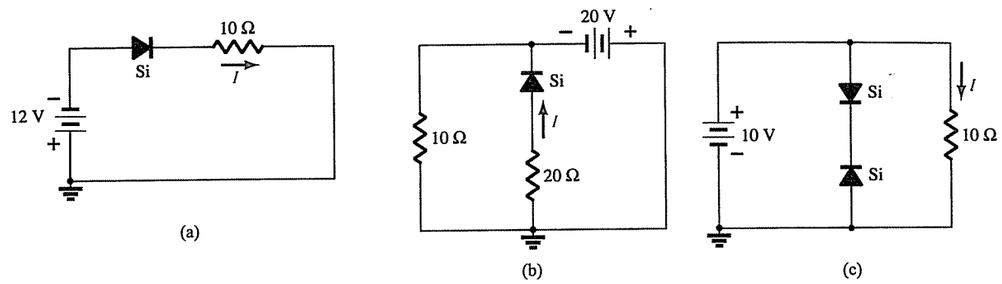


FIG. 2.149
Problem 4.

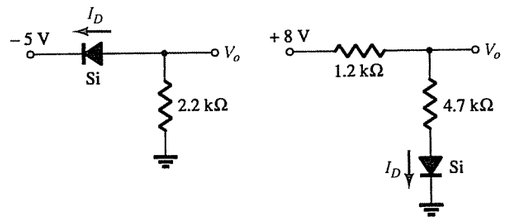
5. Determine the current I for each of the configurations of Fig. 2.150 using the approximate equivalent model for the diode.



(a) (b) (c)

FIG. 2.150
Problem 5.

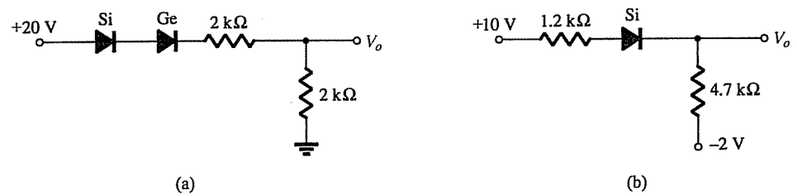
6. Determine V_o and I_D for the networks of Fig. 2.151.



(a) (b)

FIG. 2.151
Problems 6 and 49.

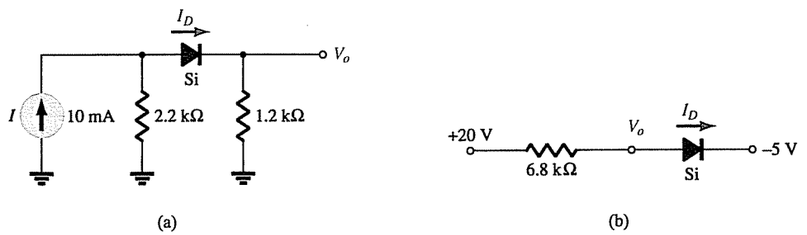
*7. Determine the level of V_o for each network of Fig. 2.152.



(a) (b)

FIG. 2.152
Problem 7.

*8. Determine V_o and I_D for the networks of Fig. 2.153.



(a) (b)

FIG. 2.153
Problem 8.

*9. Determine V_{o_1} and V_{o_2} for the networks of Fig. 2.154.

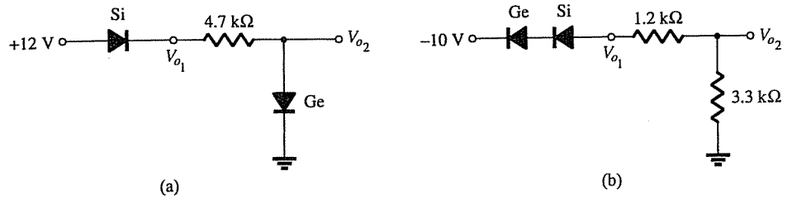


FIG. 2.154
Problem 9.

2.4 Parallel and Series–Parallel Configurations

10. Determine V_o and I_D for the networks of Fig. 2.155.

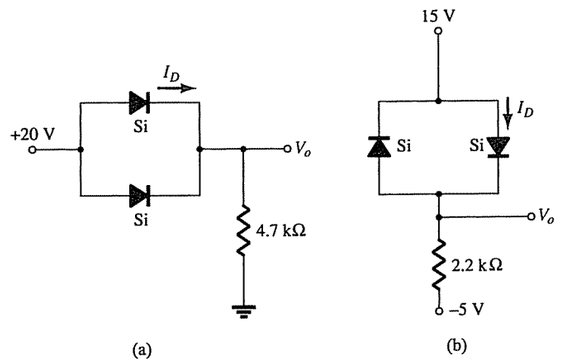


FIG. 2.155
Problems 10 and 50.

*11. Determine V_o and I for the networks of Fig. 2.156.

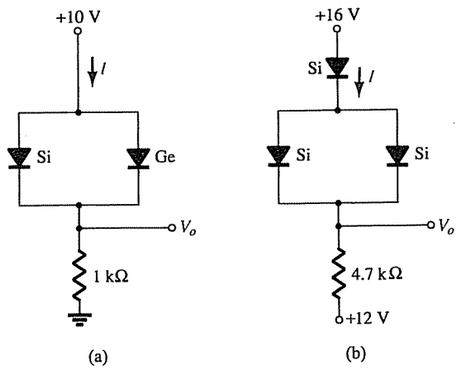


FIG. 2.156
Problem 11.

12. Determine V_{o_1}, V_{o_2}, and I for the network of Fig. 2.157.

*13. Determine V_o and I_D for the network of Fig. 2.158.

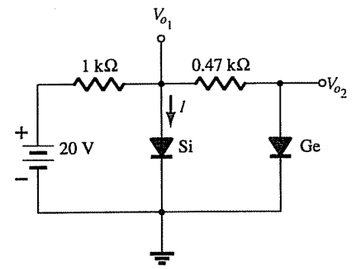


FIG. 2.157
Problem 12.

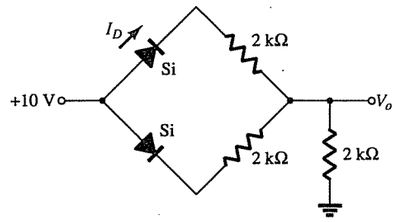


FIG. 2.158
Problems 13 and 51.

2.5 AND/OR Gates

14. Determine V_o for the network of Fig. 2.39 with 0 V on both inputs.
15. Determine V_o for the network of Fig. 2.39 with 10 V on both inputs.
16. Determine V_o for the network of Fig. 2.42 with 0 V on both inputs.
17. Determine V_o for the network of Fig. 2.42 with 10 V on both inputs.
18. Determine V_o for the negative logic OR gate of Fig. 2.159.
19. Determine V_o for the negative logic AND gate of Fig. 2.160.

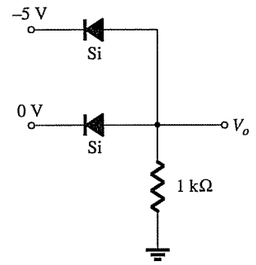


FIG. 2.159
Problem 18.

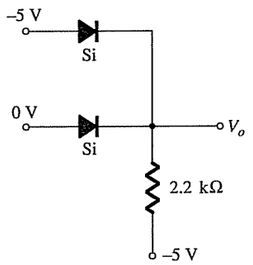


FIG. 2.160
Problem 19.

20. Determine the level of V_o for the gate of Fig. 2.161.
21. Determine V_o for the configuration of Fig. 2.162.

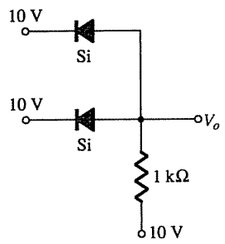


FIG. 2.161
Problem 20.

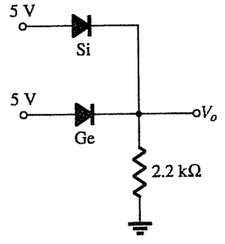


FIG. 2.162
Problem 21.

2.6 Sinusoidal Inputs; Half-Wave Rectification

22. Assuming an ideal diode, sketch v_i, v_d, and i_d for the half-wave rectifier of Fig. 2.163. The input is a sinusoidal waveform with a frequency of 60 Hz.
23. Repeat Problem 22 with a silicon diode ($V_K = 0.7$ V).
24. Repeat Problem 22 with a 6.8-kΩ load applied as shown in Fig. 2.164. Sketch v_L and i_L.

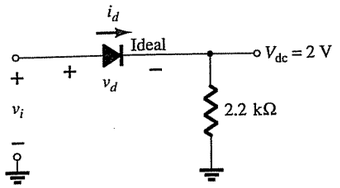


FIG. 2.163
Problems 22 through 24.

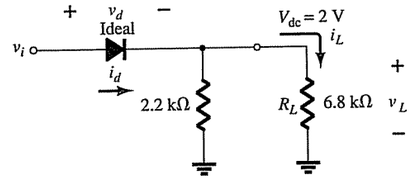


FIG. 2.164
Problem 24.

25. For the network of Fig. 2.165, sketch v_o and determine V_{dc}.

***26.** For the network of Fig. 2.166, sketch v_o and i_R.

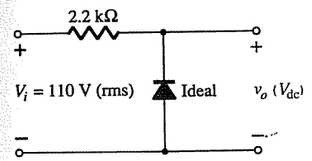


FIG. 2.165
Problem 25.

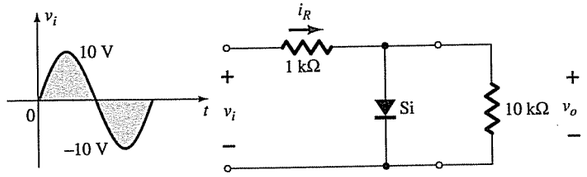


FIG. 2.166
Problem 26.

***27.** **a.** Given $P_{max} = 14$ mW for each diode at Fig. 2.167, determine the maximum current rating of each diode (using the approximate equivalent model).

b. Determine I_{max} for $V_{i_{max}} = 160$ V.

c. Determine the current through each diode at $V_{i_{max}}$ using the results of part (b).

d. If only one diode were present, determine the diode current and compare it to the maximum rating.

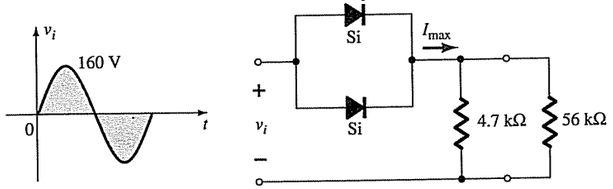


FIG. 2.167
Problem 27.

2.7 Full-Wave Rectification

28. A full-wave bridge rectifier with a 120-V rms sinusoidal input has a load resistor of 1 kΩ.

a. If silicon diodes are employed, what is the dc voltage available at the load?

b. Determine the required PIV rating of each diode.

c. Find the maximum current through each diode during conduction.

d. What is the required power rating of each diode?

29. Determine v_o and the required PIV rating of each diode for the configuration of Fig. 2.168.

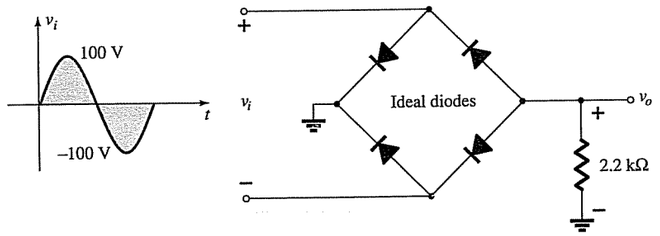


FIG. 2.168
Problem 29.

***30.** Sketch v_o for the network of Fig. 2.169 and determine the dc voltage available.

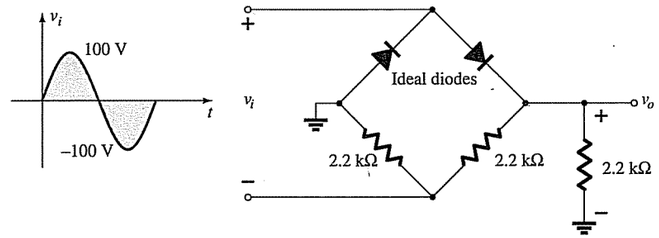


FIG. 2.169
Problem 30.

***31.** Sketch v_o for the network of Fig. 2.170 and determine the dc voltage available.

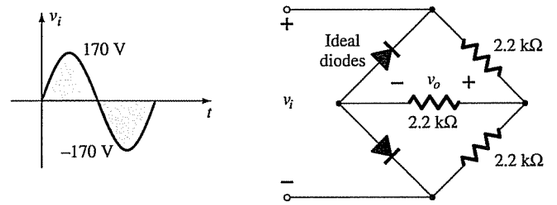


FIG. 2.170
Problem 31.

2.8 Clippers

32. Determine v_o for each network of Fig. 2.171 for the input shown.

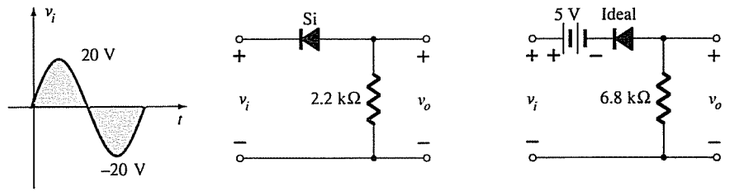


FIG. 2.171
Problem 32.

33. Determine v_o for each network of Fig. 2.172 for the input shown.

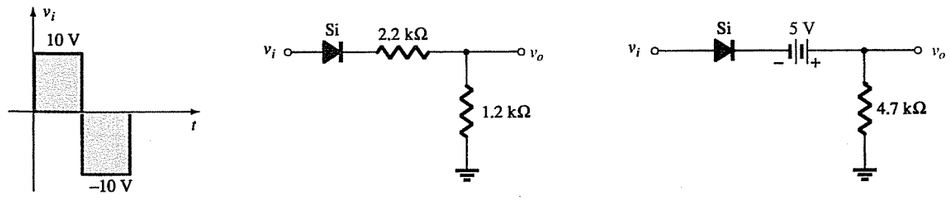


FIG. 2.172
Problem 33.

*34. Determine v_o for each network of Fig. 2.173 for the input shown.

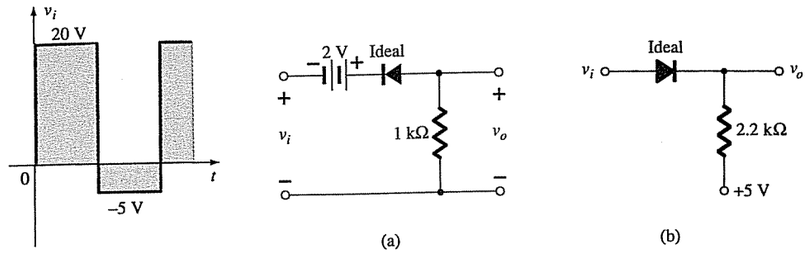


FIG. 2.173
Problem 34.

*35. Determine v_o for each network of Fig. 2.174 for the input shown.

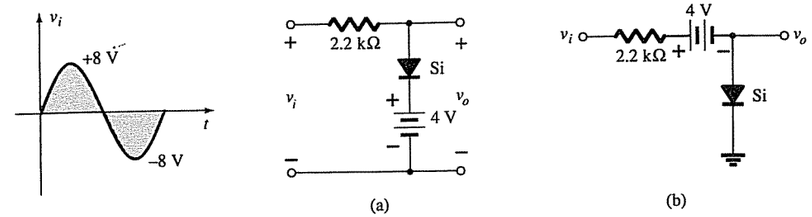


FIG. 2.174
Problem 35.

36. Sketch i_R and v_o for the network of Fig. 2.175 for the input shown.

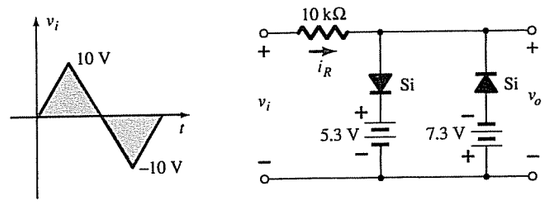


FIG. 2.175
Problem 36.

2.9 Clampers

37. Sketch v_o for each network of Fig. 2.176 for the input shown.

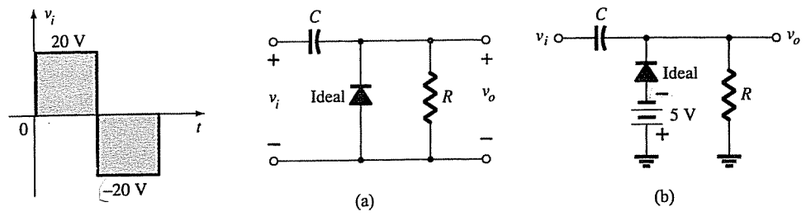


FIG. 2.176
Problem 37.

38. Sketch v_o for each network of Fig. 2.177 for the input shown. Would it be a good approximation to consider the diode to be ideal for both configurations? Why?

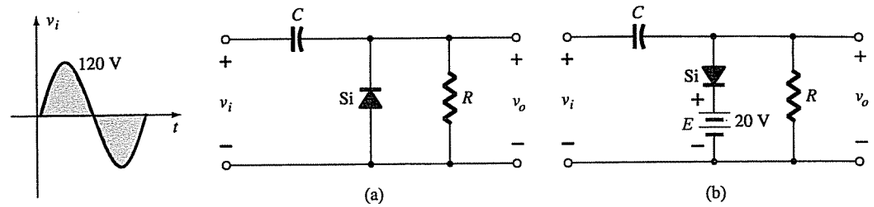


FIG. 2.177
Problem 38.

*39. For the network of Fig. 2.178:
- **a.** Calculate 5τ.
- **b.** Compare 5τ to half the period of the applied signal.
- **c.** Sketch v_o.

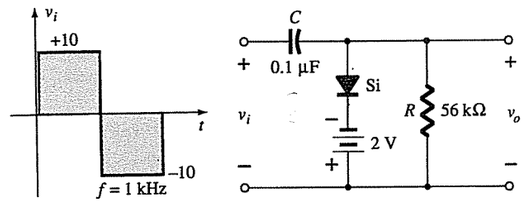


FIG. 2.178
Problem 39.

*40. Design a clamper to perform the function indicated in Fig. 2.179.

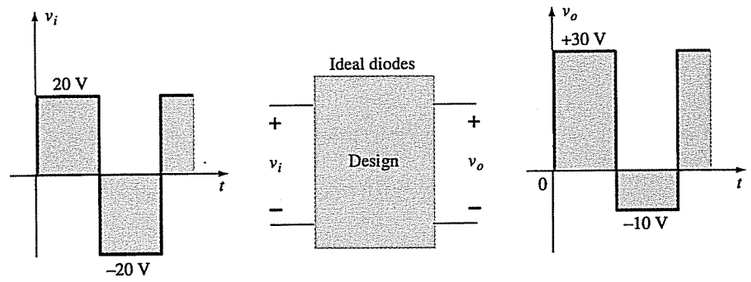


FIG. 2.179
Problem 40.

*41. Design a clamper to perform the function indicated in Fig. 2.180.

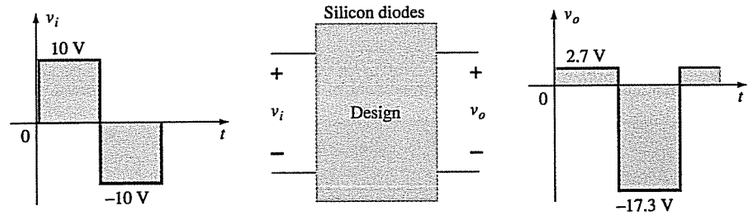


FIG. 2.180
Problem 41.

2.10 Zener Diodes

*42. **a.** Determine V_L, I_L, I_Z, and I_R for the network Fig. 2.181 if $R_L = 180\ \Omega$.
b. Repeat part (a) if $R_L = 470\ \Omega$.
c. Determine the value of R_L that will establish maximum power conditions for the Zener diode.
d. Determine the minimum value of R_L to ensure that the Zener diode is in the "on" state.

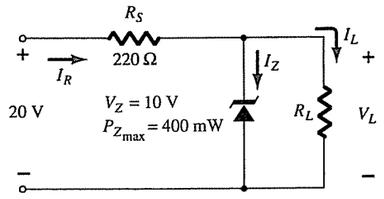


FIG. 2.181
Problem 42.

*43. **a.** Design the network of Fig. 2.182 to maintain V_L at 12 V for a load variation (I_L) from 0 mA to 200 mA. That is, determine R_S and V_Z.
b. Determine $P_{Z_{max}}$ for the Zener diode of part (a).

*44. For the network of Fig. 2.183, determine the range of V_i that will maintain V_L at 8 V and not exceed the maximum power rating of the Zener diode.

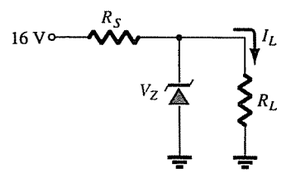


FIG. 2.182
Problem 43.

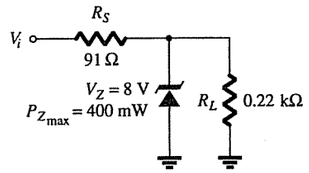


FIG. 2.183
Problems 44 and 52.

45. Design a voltage regulator that will maintain an output voltage of 20 V across a 1-kΩ load with an input that will vary between 30 V and 50 V. That is, determine the proper value of R_S and the maximum current I_{ZM}.

46. Sketch the output of the network of Fig. 2.140 if the input is a 50-V square wave. Repeat for a 5-V square wave.

2.11 Voltage-Multiplier Circuits

47. Determine the voltage available from the voltage doubler of Fig. 2.118 if the secondary voltage of the transformer is 120 V (rms).

48. Determine the required PIV ratings of the diodes of Fig. 2.118 in terms of the peak secondary voltage V_m.

2.14 Computer Analysis

49. Perform an analysis of the network of Fig. 2.151 using PSpice Windows.

50. Perform an analysis of the network of Fig. 2.155 using PSpice Windows.

51. Perform an analysis of the network of Fig. 2.158 using PSpice Windows.

52. Perform a general analysis of the Zener network of Fig. 2.183 using PSpice Windows.

53. Repeat Problem 49 using Multisim.

54. Repeat Problem 50 using Multisim.

55. Repeat Problem 51 using Multisim.

56. Repeat Problem 52 using Multisim.

3 Bipolar Junction Transistors

CHAPTER OUTLINE

3.1 Introduction
3.2 Transistor Construction
3.3 Transistor Operation
3.4 Common-Base Configuration
3.5 Transistor Amplifying Action
3.6 Common-Emitter Configuration
3.7 Common-Collector Configuration
3.8 Limits of Operation
3.9 Transistor Specification Sheet
3.10 Transistor Testing
3.11 Transistor Casing and Terminal Identification
3.12 Summary
3.13 Computer Analysis



Coinventors of the first transistor at Bell Laboratories: Dr. William Shockley (seated); Dr. John Bardeen (left); Dr. Walter H. Brattain. (Courtesy of AT&T Archives.)

Dr. Shockley	Born: London, England, 1910 PhD Harvard, 1936
Dr. Bardeen	Born: Madison, Wisconsin, 1908 PhD Princeton, 1936
Dr. Brattain	Born: Amoy, China, 1902 PhD University of Minnesota, 1928

All shared the Nobel Prize in 1956 for this contribution.

3.1 INTRODUCTION

During 1904 to1947, the vacuum tube was undoubtedly the electronic device of interest and development. In 1904, the vacuum -tube diode was introduced by J. A. Fleming. Shortly thereafter, in 1906, Lee De Forest added a third element, called the *control grid*, to the vacuum diode, resulting in the first amplifier, the *triode*. In the following years, radio and television provided great stimulation to the tube industry. Production rose from about 1 million tubes in 1922 to about 100 million in 1937. In the early 1930s the four-element tetrode and the five-element pentode gained prominence in the electron-tube industry. In the years to follow, the industry became one of primary importance, and rapid advances were made in design, manufacturing techniques, high-power and high-frequency applications, and miniaturization.

On December 23, 1947, however, the electronics industry was to experience the advent of a completely new direction of interest and development. It was on the afternoon of this day that Walter H. Brattain and John Bardeen demonstrated the amplifying action of the first transistor at the Bell Telephone Laboratories. The original transistor (a point-contact transistor) is shown in Fig. 3.1. The advantages of this three-terminal solid-state device over the tube were immediately obvious: It was smaller and lightweight; it had no heater requirement or heater loss; it had a rugged construction; it was more efficient since less power was absorbed by the device itself; it was instantly available for use, requiring no warm-up

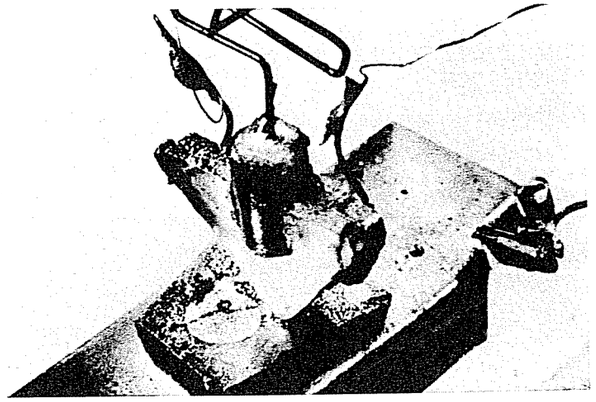
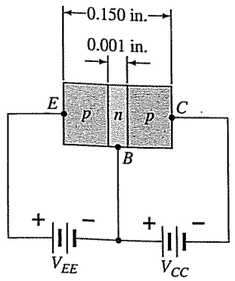
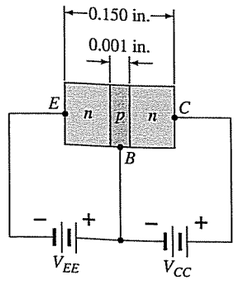


FIG. 3.1
The first transistor. (Courtesy Bell Telephone Laboratories.)



(a)



(b)

FIG. 3.2
Types of transistors: (a) pnp; (b) npn.

period; and lower operating voltages were possible. Note that this chapter is our first discussion of devices with three or more terminals. You will find that all amplifiers (devices that increase the voltage, current, or power level) have at least three terminals, with one controlling the flow between the other two.

3.2 TRANSISTOR CONSTRUCTION

The transistor is a three-layer semiconductor device consisting of either two *n*- and one *p*-type layers of material or two *p*- and one *n*-type layers of material. The former is called an *npn transistor*, and the latter is called a *pnp transistor*. Both are shown in Fig. 3.2 with the proper dc biasing. We will find in Chapter 4 that the dc biasing is necessary to establish the proper region of operation for ac amplification. The emitter layer is heavily doped, the base lightly doped, and the collector only lightly doped. The outer layers have widths much greater than the sandwiched *p*- or *n*-type material. For the transistors shown in Fig. 3.2 the ratio of the total width to that of the center layer is 0.150/0.001 = 150 : 1. The doping of the sandwiched layer is also considerably less than that of the outer layers (typically, 10 : 1 or less). This lower doping level decreases the conductivity (increases the resistance) of this material by limiting the number of "free" carriers.

For the biasing shown in Fig. 3.2 the terminals have been indicated by the capital letters *E* for *emitter*, *C* for *collector*, and *B* for *base*. An appreciation for this choice of notation will develop when we discuss the basic operation of the transistor. The abbreviation BJT, from *bipolar junction transistor*, is often applied to this three-terminal device. The term *bipolar* reflects the fact that holes *and* electrons participate in the injection process into the oppositely polarized material. If only one carrier is employed (electron or hole), it is considered a *unipolar* device. The Schottky diode of Chapter 16 is such a device.

3.3 TRANSISTOR OPERATION

The basic operation of the transistor will now be described using the *pnp* transistor of Fig. 3.2a. The operation of the *npn* transistor is exactly the same if the roles played by the electron and hole are interchanged. In Fig. 3.3 the *pnp* transistor has been redrawn without the base-to-collector bias. Note the similarities between this situation and that of the *forward-biased* diode in Chapter 1. The depletion region has been reduced in width due to the applied bias, resulting in a heavy flow of majority carriers from the *p*- to the *n*-type material.

Let us now remove the base-to-emitter bias of the *pnp* transistor of Fig. 3.2a as shown in Fig. 3.4. Consider the similarities between this situation and that of the *reverse-biased* diode of Section 1.6. Recall that the flow of majority carriers is zero, resulting in only a minority-carrier flow, as indicated in Fig. 3.4. In summary, therefore:

One p–n junction of a transistor is reverse-biased, whereas the other is forward-biased.

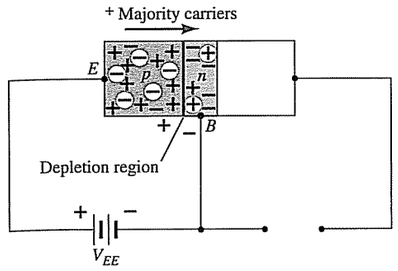


FIG. 3.3
Forward-biased junction of a pnp transistor.

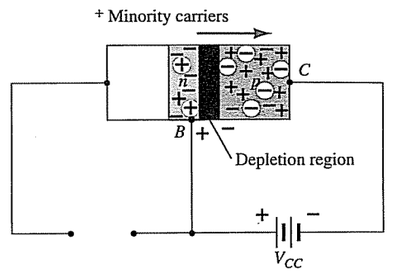


FIG. 3.4
Reverse-biased junction of a pnp transistor.

In Fig. 3.5 both biasing potentials have been applied to a *pnp* transistor, with the resulting majority- and minority-carrier flows indicated. Note in Fig. 3.5 the widths of the depletion regions, indicating clearly which junction is forward-biased and which is reverse-biased. As indicated in Fig. 3.5, a large number of majority carriers will diffuse across the forward-biased *p–n* junction into the *n*-type material. The question then is whether these carriers will contribute directly to the base current I_B or pass directly into the *p*-type material. Since the sandwiched *n*-type material is very thin and has a low conductivity, a very small number of these carriers will take this path of high resistance to the base terminal. The magnitude of the base current is typically on the order of microamperes, as compared to milliamperes for the emitter and collector currents. The larger number of these majority carriers will diffuse across the reverse-biased junction into the *p*-type material connected to the collector terminal as indicated in Fig. 3.5. The reason for the relative ease with which the majority carriers can cross the reverse-biased junction is easily understood if we consider that for the reverse-biased diode the injected majority carriers will appear as minority carriers in the *n*-type material. In other words, there has been an *injection* of minority carriers into the *n*-type base region material. Combining this with the fact that all the minority carriers in the depletion region will cross the reverse-biased junction of a diode accounts for the flow indicated in Fig. 3.5.

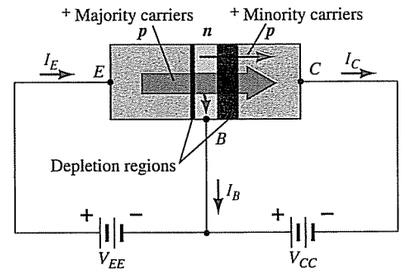


FIG. 3.5
Majority and minority carrier flow of a pnp transistor.

Applying Kirchhoff's current law to the transistor of Fig. 3.5 as if it were a single node, we obtain

$$\boxed{I_E = I_C + I_B} \tag{3.1}$$

and find that the emitter current is the sum of the collector and base currents. The collector current, however, comprises two components—the majority and the minority carriers as indicated in Fig. 3.5. The minority-current component is called the *leakage current* and is given the symbol I_{CO} (I_C current with emitter terminal *O*pen). The collector current, therefore, is determined in total by

$$\boxed{I_C = I_{C_{\text{majority}}} + I_{CO_{\text{minority}}}} \tag{3.2}$$

For general-purpose transistors, I_C is measured in milliamperes and I_{CO} is measured in microamperes or nanoamperes. I_{CO}, like I_s for a reverse-biased diode, is temperature sensitive and must be examined carefully when applications of wide temperature ranges are considered. It can severely affect the stability of a system at high temperature if not considered properly. Improvements in construction techniques have resulted in significantly lower levels of I_{CO}, to the point where its effect can often be ignored.

3.4 COMMON-BASE CONFIGURATION

The notation and symbols used in conjunction with the transistor in the majority of texts and manuals published today are indicated in Fig. 3.6 for the common-base configuration with *pnp* and *npn* transistors. The common-base terminology is derived from the fact that the base is common to both the input and output sides of the configuration. In addition, the base is usually the terminal closest to, or at, ground potential. Throughout this book all current directions will refer to conventional (hole) flow rather than electron flow. This choice was based primarily on the fact that the vast amount of literature available at educational and industrial institutions employs conventional flow, and the arrows in all electronic symbols have a direction defined by this convention. Recall that the arrow in the diode symbol defined the direction of conduction for conventional current. For the transistor:

The arrow in the graphic symbol defines the direction of emitter current (conventional flow) through the device.

All the current directions appearing in Fig. 3.6 are the actual directions as defined by the choice of conventional flow. Note in each case that $I_E = I_C + I_B$. Note also that the applied biasing (voltage sources) are such as to establish current in the direction indicated for each branch. That is, compare the direction of I_E to the polarity of V_{EE} for each configuration and the direction of I_C to the polarity of V_{CC}.

To fully describe the behavior of a three-terminal device such as the common-base amplifiers of Fig. 3.6 requires two sets of characteristics—one for the *driving point* or *input* parameters and the other for the *output* side. The input set for the common-base amplifier as shown in Fig. 3.7 relates an input current (I_E) to an input voltage (V_{BE}) for various levels of output voltage (V_{CB}).

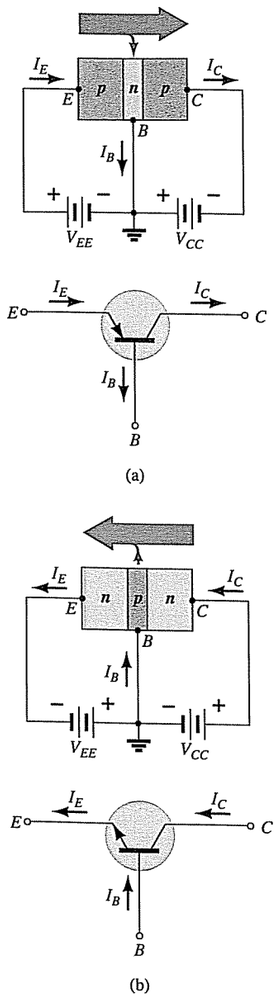


FIG. 3.6
Notation and symbols used with the common-base configuration: (a) pnp transistor; (b) npn transistor.

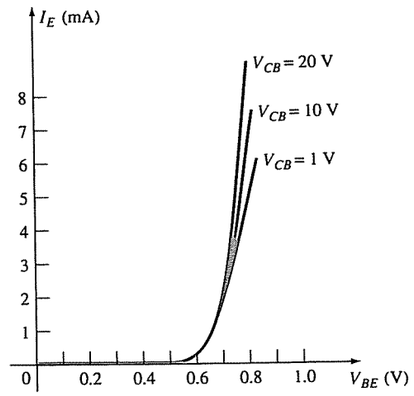


FIG. 3.7
Input or driving point characteristics for a common-base silicon transistor amplifier.

The output set relates an output current (I_C) to an output voltage (V_{CB}) for various levels of input current (I_E) as shown in Fig. 3.8. The output or *collector* set of characteristics has three basic regions of interest, as indicated in Fig. 3.8: the *active*, *cutoff*, and *saturation* regions. The active region is the region normally employed for linear (undistorted) amplifiers. In particular:

In the active region the base–emitter junction is forward-biased, whereas the collector–base junction is reverse-biased.

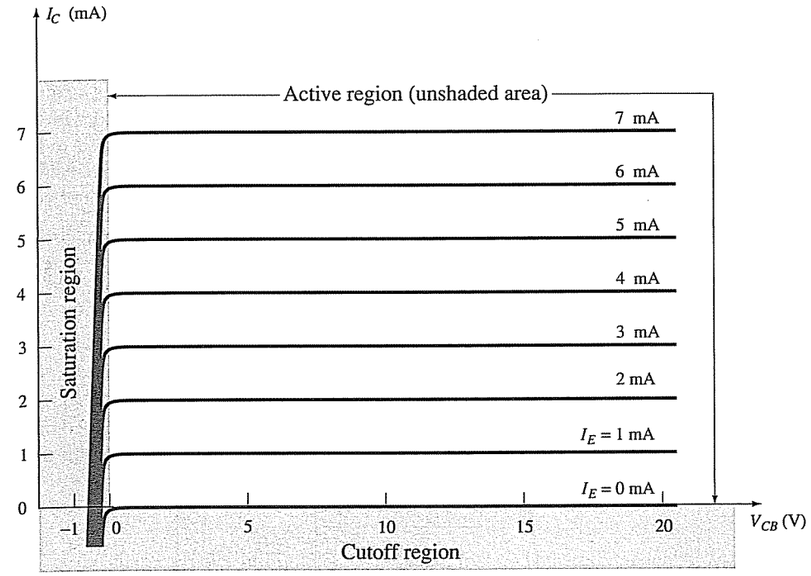


FIG. 3.8
Output or collector characteristics for a common-base transistor amplifier.

The active region is defined by the biasing arrangements of Fig. 3.6. At the lower end of the active region the emitter current (I_E) is zero, and the collector current is simply that due to the reverse saturation current I_{CO}, as indicated in Fig. 3.9. The current I_{CO} is so small (microamperes) in magnitude compared to the vertical scale of I_C (milliamperes) that it appears on virtually the same horizontal line as $I_C = 0$. The circuit conditions that exist when $I_E = 0$ for the common-base configuration are shown in Fig. 3.9. The notation most frequently used for I_{CO} on data and specification sheets is, as indicated in Fig. 3.9, I_{CBO}. Because of improved construction techniques, the level of I_{CBO} for general-purpose transistors (especially silicon) in the low- and mid-power ranges is usually so low that its effect can be ignored. However, for higher power units I_{CBO} will still appear in the microampere range. In addition, keep in mind that I_{CBO}, like I_s, for the diode (both reverse leakage currents) is temperature sensitive. At higher temperatures the effect of I_{CBO} may become an important factor since it increases so rapidly with temperature.

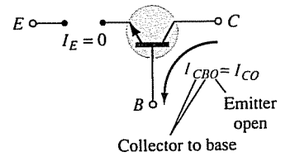


FIG. 3.9
Reverse saturation current.

Note in Fig. 3.8 that as the emitter current increases above zero, the collector current increases to a magnitude essentially equal to that of the emitter current as determined by the basic transistor-current relations. Note also the almost negligible effect of V_{CB} on the collector current for the active region. The curves clearly indicate that *a first approximation to the relationship between I_E and I_C in the active region is given by*

$$I_C \cong I_E \tag{3.3}$$

As inferred by its name, the cutoff region is defined as that region where the collector current is 0 A, as revealed on Fig. 3.8. In addition:

In the cutoff region the base–emitter and collector–base junctions of a transistor are both reverse-biased.

The saturation region is defined as that region of the characteristics to the left of $V_{CB} = 0$ V. The horizontal scale in this region was expanded to clearly show the dramatic change in characteristics in this region. Note the exponential increase in collector current as the voltage V_{CB} increases toward 0 V.

In the saturation region the base–emitter and collector–base junctions are forward-biased.

The input characteristics of Fig. 3.7 reveal that for fixed values of collector voltage (V_{CB}), as the base-to-emitter voltage increases, the emitter current increases in a manner that

closely resembles the diode characteristics. In fact, increasing levels of V_{CB} have such a small effect on the characteristics that as a first approximation the change due to changes in V_{CB} can be ignored and the characteristics drawn as shown in Fig. 3.10a. If we then apply the piecewise-linear approach, the characteristics of Fig. 3.10b result. Taking it a step further and ignoring the slope of the curve and therefore the resistance associated with the forward-biased junction results in the characteristics of Fig. 3.10c. For the analysis to follow in this book the equivalent model of Fig. 3.10c will be employed for all dc analysis of transistor networks. That is, once a transistor is in the "on" state, the base-to-emitter voltage will be assumed to be the following:

$$V_{BE} = 0.7\text{ V} \tag{3.4}$$

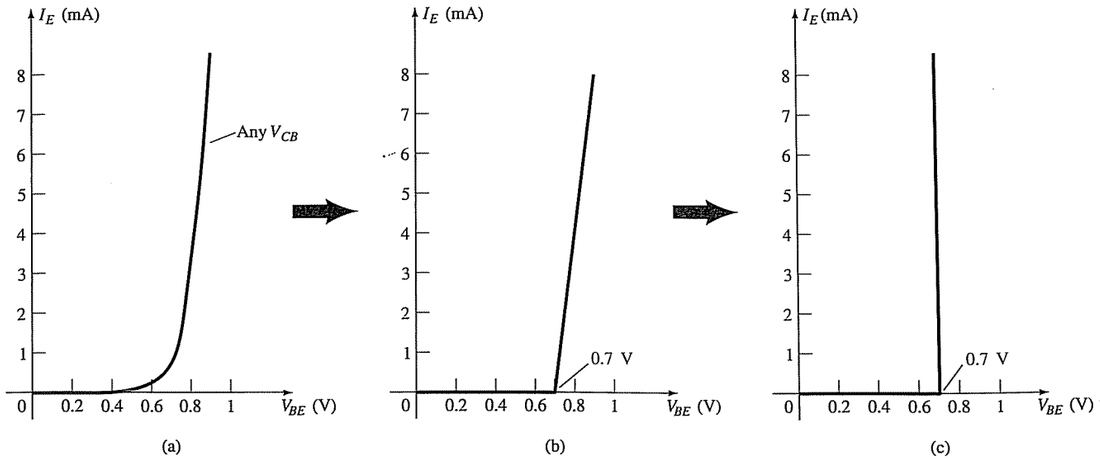


FIG. 3.10

Developing the equivalent model to be employed for the base-to-emitter region of an amplifier in the dc mode.

In other words, the effect of variations due to V_{CB} and the slope of the input characteristics will be ignored as we strive to analyze transistor networks in a manner that will provide a good approximation to the actual response without getting too involved with parameter variations of less importance.

It is important to fully appreciate the statement made by the characteristics of Fig. 3.10c. They specify that with the transistor in the "on" or active state the voltage from base to emitter will be 0.7 V at *any* level of emitter current as controlled by the external network. In fact, at the first encounter of any transistor configuration in the dc mode, one can now immediately specify that the voltage from base to emitter is 0.7 V if the device is in the active region—a very important conclusion for the dc analysis to follow.

EXAMPLE 3.1

a. Using the characteristics of Fig. 3.8, determine the resulting collector current if $I_E = 3$ mA and $V_{CB} = 10$ V.
b. Using the characteristics of Fig. 3.8, determine the resulting collector current if I_E remains at 3 mA but V_{CB} is reduced to 2 V.
c. Using the characteristics of Figs. 3.7 and 3.8, determine V_{BE} if $I_C = 4$ mA and $V_{CB} = 20$ V.
d. Repeat part (c) using the characteristics of Figs. 3.8 and 3.10c.

Solution:

a. The characteristics clearly indicate that $I_C \cong I_E = \mathbf{3\text{ mA}}$.
b. The effect of changing V_{CB} is negligible and I_C continues to be **3 mA**.
c. From Fig. 3.8, $I_E \cong I_C = 4$ mA. On Fig. 3.7 the resulting level of V_{BE} is about **0.74 V**.
d. Again from Fig. 3.8, $I_E \cong I_C = 4$ mA. However, on Fig. 3.10c. V_{BE} is **0.7 V** for any level of emitter current.

Alpha (α)

In the dc mode the levels of I_C and I_E due to the majority carriers are related by a quantity called *alpha* and defined by the following equation:

$$\alpha_{dc} = \frac{I_C}{I_E} \tag{3.5}$$

where I_C and I_E are the levels of current at the point of operation. Even though the characteristics of Fig. 3.8 would suggest that $\alpha = 1$, for practical devices alpha typically extends from 0.90 to 0.998, with most values approaching the high end of the range. Since alpha is defined solely for the majority carriers, Eq. (3.2) becomes

$$I_C = \alpha I_E + I_{CBO} \tag{3.6}$$

For the characteristics of Fig. 3.8 when $I_E = 0$ mA, I_C is therefore equal to I_{CBO}, but as mentioned earlier, the level of I_{CBO} is usually so small that it is virtually undetectable on the graph of Fig. 3.8. In other words, when $I_E = 0$ mA on Fig. 3.8, I_C also appears to be 0 mA for the range of V_{CB} values.

For ac situations where the point of operation moves on the characteristic curve, an ac alpha is defined by

$$\alpha_{ac} = \left.\frac{\Delta I_C}{\Delta I_E}\right|_{V_{CB}=\text{constant}} \tag{3.7}$$

The ac alpha is formally called the *common-base*, *short-circuit*, *amplification factor*, for reasons that will be more obvious when we examine transistor equivalent circuits in Chapter 5. For the moment, recognize that Eq. (3.7) specifies that a relatively small change in collector current is divided by the corresponding change in I_E with the collector-to-base voltage held constant. For most situations the magnitudes of α_{ac} and α_{dc} are quite close, permitting the use of the magnitude of one for the other. The use of an equation such as (3.7) will be demonstrated in Section 3.6.

Biasing

The proper biasing of the common-base configuration in the active region can be determined quickly using the approximation $I_C \cong I_E$ and assuming for the moment that $I_B \cong 0\,\mu$A. The result is the configuration of Fig. 3.11 for the *pnp* transistor. The arrow of

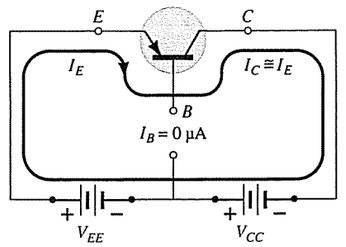


FIG. 3.11

Establishing the proper biasing management for a common-base pnp transistor in the active region.

the symbol defines the direction of conventional flow for $I_E \cong I_C$. The dc supplies are then inserted with a polarity that will support the resulting current direction. For the *npn* transistor the polarities will be reversed.

Some students feel that they can remember whether the arrow of the device symbol is pointing in or out by matching the letters of the transistor type with the appropriate letters of the phrases "pointing in" or "not pointing in." For instance, there is a match between the letters *npn* and the italic letters of *n*ot *p*ointing i*n* and the letters *pnp* with *p*ointing i*n*.

3.5 TRANSISTOR AMPLIFYING ACTION

Now that the relationship between I_C and I_E has been established in Section 3.4, the basic amplifying action of the transistor can be introduced on a surface level using the network of Fig. 3.12. The dc biasing does not appear in the figure since our interest will be limited to the ac response. For the common-base configuration the ac input resistance determined by the characteristics of Fig. 3.7 is quite small and typically varies from 10 Ω to 100 Ω. The output resistance as determined by the curves of Fig. 3.8 is quite high (the more horizontal the curves, the higher is the resistance) and typically varies from 50 kΩ to 1 MΩ (100 kΩ for the transistor of Fig. 3.12). The difference in resistance is due to the forward-biased junction at the input (base to emitter) and the reverse-biased junction at the output (base to collector). Using a common value of 20 Ω for the input resistance, we find that

$$I_i = \frac{V_i}{R_i} = \frac{200\text{ mV}}{20\ \Omega} = \mathbf{10\text{ mA}}$$

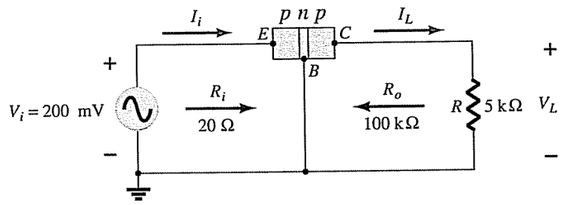


FIG. 3.12
Basic voltage amplification action of the common-base configuration.

If we assume for the moment that $\alpha_{ac} = 1$ ($I_c = I_e$), we obtain

$$I_L = I_i = 10\text{ mA}$$

and

$$V_L = I_L R = (10\text{ mA})(5\text{ k}\Omega) = \mathbf{50\text{ V}}$$

The voltage amplification is

$$A_v = \frac{V_L}{V_i} = \frac{50\text{ V}}{200\text{ mV}} = \mathbf{250}$$

Typical values of voltage amplification for the common-base configuration vary from 50 to 300. The current amplification (I_c/I_e) is always less than 1 for the common-base configuration. This latter characteristic should be obvious since $I_c = \alpha I_e$ and α is always less than 1.

The basic amplifying action was produced by *transferring* a current I from a low- to a high-*resistance* circuit. The combination of the two terms in italics results in the label *transistor*; that is,

*trans*fer + re*sistor* → *transistor*

3.6 COMMON-EMITTER CONFIGURATION

The most frequently encountered transistor configuration appears in Fig. 3.13 for the *pnp* and *npn* transistors. It is called the *common-emitter configuration* because the emitter is common or reference to both the input and output terminals (in this case common to both the base and collector terminals). Two sets of characteristics are again necessary to describe fully the behavior of the common-emitter configuration: one for the *input* or *base–emitter* circuit and one for the *output* or *collector–emitter* circuit. Both are shown in Fig. 3.14.

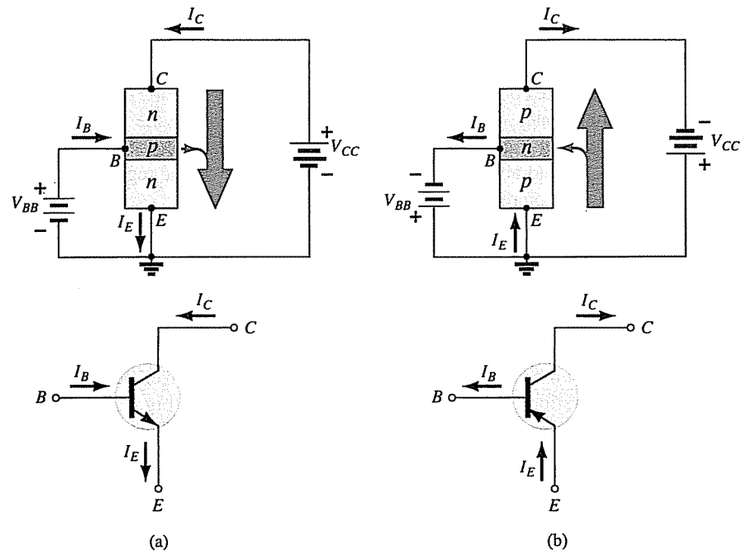


FIG. 3.13
Notation and symbols used with the common-emitter configuration: (a) npn transistor; (b) pnp transistor.

Multisim

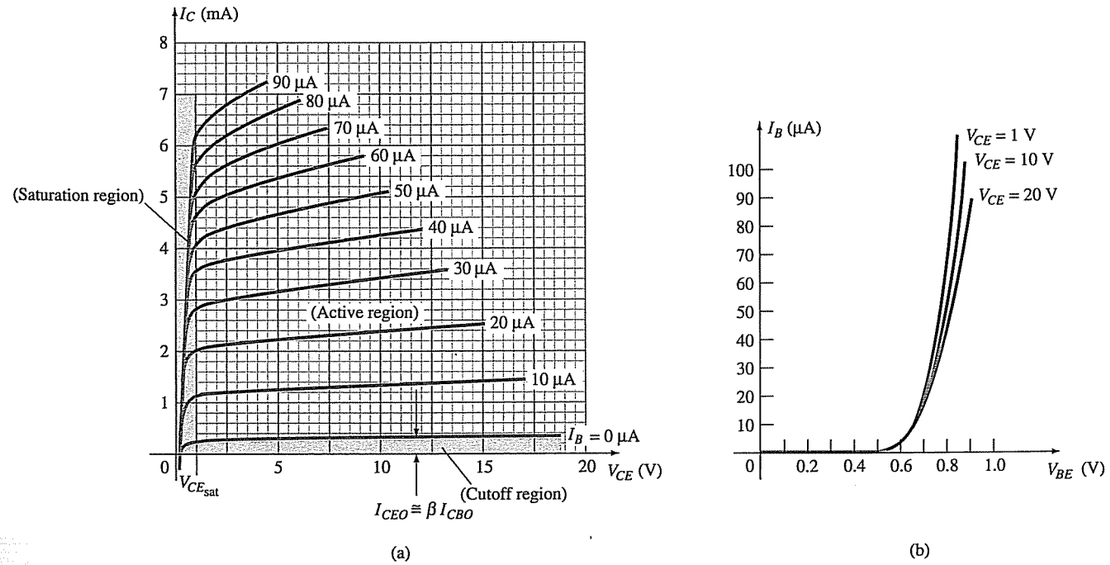


FIG. 3.14
Characteristics of a silicon transistor in the common-emitter configuration: (a) collector characteristics; (b) base characteristics.

The emitter, collector, and base currents are shown in their actual conventional current direction. Even though the transistor configuration has changed, the current relations developed earlier for the common-base configuration are still applicable. That is, $I_E = I_C + I_B$ and $I_C = \alpha I_E$.

For the common-emitter configuration the output characteristics are a plot of the output current (I_C) versus output voltage (V_{CE}) for a range of values of input current (I_B). The input characteristics are a plot of the input current (I_B) versus the input voltage (V_{BE}) for a range of values of output voltage (V_{CE}).

Note that on the characteristics of Fig. 3.14 the magnitude of I_B is in microamperes, compared to milliamperes of I_C. Consider also that the curves of I_B are not as horizontal as those obtained for I_E in the common-base configuration, indicating that the collector-to-emitter voltage will influence the magnitude of the collector current.

The active region for the common-emitter configuration is that portion of the upper-right quadrant that has the greatest linearity, that is, that region in which the curves for I_B are nearly straight and equally spaced. In Fig. 3.14a this region exists to the right of the vertical dashed line at $V_{CE_{sat}}$ and above the curve for I_B equal to zero. The region to the left of $V_{CE_{sat}}$ is called the saturation region.

In the active region of a common-emitter amplifier, the base–emitter junction is forward-biased, whereas the collector–base junction is reverse-biased.

You will recall that these were the same conditions that existed in the active region of the common-base configuration. The active region of the common-emitter configuration can be employed for voltage, current, or power amplification.

The cutoff region for the common-emitter configuration is not as well defined as for the common-base configuration. Note on the collector characteristics of Fig. 3.14 that I_C is not equal to zero when I_B is zero. For the common-base configuration, when the input current I_E was equal to zero, the collector current was equal only to the reverse saturation current I_{CO}, so that the curve $I_E = 0$ and the voltage axis were, for all practical purposes, one.

The reason for this difference in collector characteristics can be derived through the proper manipulation of Eqs. (3.3) and (3.6). That is,

$$\text{Eq. (3.6):} \quad I_C = \alpha I_E + I_{CBO}$$

Substitution gives

$$\text{Eq. (3.3):} \quad I_C = \alpha(I_C + I_B) + I_{CBO}$$

Rearranging yields

$$I_C = \frac{\alpha I_B}{1 - \alpha} + \frac{I_{CBO}}{1 - \alpha} \tag{3.8}$$

If we consider the case discussed above, where $I_B = 0$ A, and substitute a typical value of α such as 0.996, the resulting collector current is the following:

$$I_C = \frac{\alpha(0\text{ A})}{1 - \alpha} + \frac{I_{CBO}}{1 - 0.996}$$

$$= \frac{I_{CBO}}{0.004} = 250 I_{CBO}$$

If I_{CBO} were 1 μA, the resulting collector current with $I_B = 0$ A would be 250(1 μA) = 0.25 mA, as reflected in the characteristics of Fig. 3.14.

For future reference, the collector current defined by the condition $I_B = 0\ \mu$A will be assigned the notation indicated by the following equation:

$$\boxed{I_{CEO} = \left.\frac{I_{CBO}}{1 - \alpha}\right|_{I_B = 0\,\mu\text{A}}} \tag{3.9}$$

In Fig. 3.15 the conditions surrounding this newly defined current are demonstrated with its assigned reference direction.

For linear (least distortion) amplification purposes, cutoff for the common-emitter configuration will be defined by $I_C = I_{CEO}$.

In other words, the region below $I_B = 0\ \mu$A is to be avoided if an undistorted output signal is required.

When employed as a switch in the logic circuitry of a computer, a transistor will have two points of operation of interest: one in the cutoff and one in the saturation region. The

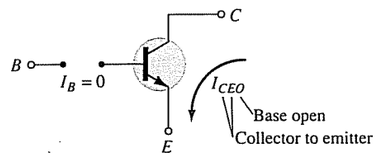


FIG. 3.15
Circuit conditions related to I_{CEO}.

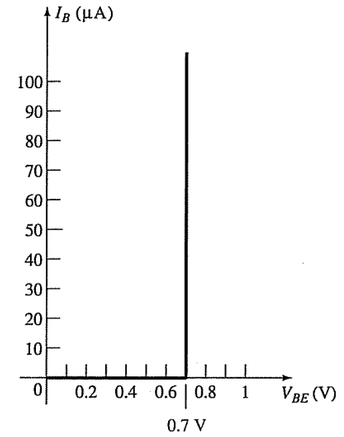


FIG. 3.16
Piecewise-linear equivalent for the diode characteristics of Fig. 3.14b.

cutoff condition should ideally be $I_C = 0$ mA for the chosen V_{CE} voltage. Since I_{CEO} is typically low in magnitude for silicon materials, *cutoff will exist for switching purposes when $I_B = 0\ \mu$A or $I_C = I_{CEO}$ for silicon transistors only. For germanium transistors, however, cutoff for switching purposes will be defined as those conditions that exist when $I_C = I_{CBO}$.* This condition can normally be obtained for germanium transistors by reverse-biasing the base-to-emitter junction a few tenths of a volt.

Recall for the common-base configuration that the input set of characteristics was approximated by a straight-line equivalent that resulted in $V_{BE} = 0.7$ V for any level of I_E greater than 0 mA. For the common-emitter configuration the same approach can be taken, resulting in the approximate equivalent of Fig. 3.16. The result supports our earlier conclusion that for a transistor in the "on" or active region the base-to-emitter voltage is 0.7 V. In this case the voltage is fixed for any level of base current.

EXAMPLE 3.2

a. Using the characteristics of Fig. 3.14, determine I_C at $I_B = 30\ \mu$A and $V_{CE} = 10$ V.
b. Using the characteristics of Fig. 3.14, determine I_C at $V_{BE} = 0.7$ V and $V_{CE} = 15$ V.

Solution:

a. At the intersection of $I_B = 30\ \mu$A and $V_{CE} = 10$ V, $I_C =$ **3.4 mA**.
b. Using Fig. 3.14b, we obtain $I_B = 20\ \mu$A at $V_{BE} = 0.7$ V. From Fig. 3.14a we find that $I_C =$ **2.5 mA** at the intersection of $I_B = 20\ \mu$A and $V_{CE} = 15$ V.

Beta (β)

In the dc mode the levels of I_C and I_B are related by a quantity called *beta* and defined by the following equation:

$$\boxed{\beta_{dc} = \frac{I_C}{I_B}} \tag{3.10}$$

where I_C and I_B are determined at a particular operating point on the characteristics. For practical devices the level of β typically ranges from about 50 to over 400, with most in the midrange. As for α, the parameter β reveals the relative magnitude of one current with respect to the other. For a device with a β of 200, the collector current is 200 times the magnitude of the base current.

On specification sheets β_{dc} is usually included as h_{FE} with the h derived from an ac *h*ybrid equivalent circuit to be introduced in Chapter 5. The subscript *FE* is derived from *f*orward-current amplification and common-*e*mitter configuration, respectively.

For ac situations an ac beta is defined as follows:

$$\beta_{ac} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}=\text{constant}} \tag{3.11}$$

The formal name for β_{ac} is *common-emitter, forward-current, amplification factor*. Since the collector current is usually the output current for a common-emitter configuration and the base current is the input current, the term *amplification* is included in the nomenclature above.

Equation (3.11) is similar in format to the equation for α_{ac} in Section 3.4. The procedure for obtaining α_{ac} from the characteristic curves was not described because of the difficulty of actually measuring changes of I_C and I_E on the characteristics. Equation (3.11), however, can be described with some clarity, and, in fact, the result can be used to find α_{ac} using an equation to be derived shortly.

On specification sheets β_{ac} is normally referred to as h_{fe}. Note that the only difference between the notation used for the dc beta, specifically, $\beta_{dc} = h_{FE}$, is the type of lettering for each subscript quantity. The lowercase letter h continues to refer to the hybrid equivalent circuit to be described in Chapter 5 and the *fe* to the *f*orward current gain in the common-*e*mitter configuration.

The use of Eq. (3.11) is best described by a numerical example using an actual set of characteristics such as appearing in Fig. 3.14a and repeated in Fig. 3.17. Let us determine β_{ac} for a region of the characteristics defined by an operating point of $I_B = 25\ \mu A$ and $V_{CE} = 7.5$ V as indicated on Fig. 3.17. The restriction of $V_{CE} =$ constant requires that a vertical line be drawn through the operating point at $V_{CE} = 7.5$ V. At any location on this vertical line the voltage V_{CE} is 7.5 V, a constant. The change in $I_B(\Delta I_B)$ as appearing in Eq. (3.11) is then defined by choosing two points on either side of the Q-point along the vertical axis of about equal distances to either side of the Q-point. For this situation the $I_B = 20\ \mu A$ and $30\ \mu A$ curves meet the requirement without extending too far from the Q-point. They also define

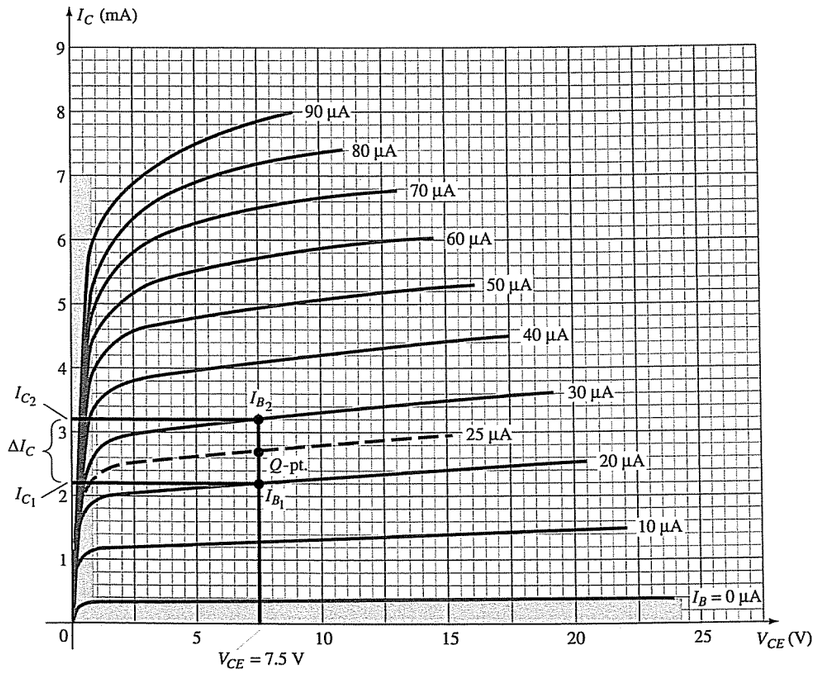


FIG. 3.17
Determining β_{ac} and β_{dc} from the collector characteristics.

levels of I_B that are easily defined rather than require interpolation of the level of I_B between the curves. It should be mentioned that the best determination is usually made by keeping the chosen ΔI_B as small as possible. At the two intersections of I_B and the vertical axis, the two levels of I_C can be determined by drawing a horizontal line over to the vertical axis and reading the resulting values of I_C. The resulting β_{ac} for the region can then be determined by

$$\beta_{ac} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}=\text{constant}} = \frac{I_{C_2} - I_{C_1}}{I_{B_2} - I_{B_1}}$$
$$= \frac{3.2\ \text{mA} - 2.2\ \text{mA}}{30\ \mu A - 20\ \mu A} = \frac{1\ \text{mA}}{10\ \mu A}$$
$$= \mathbf{100}$$

The solution above reveals that for an ac input at the base, the collector current will be about 100 times the magnitude of the base current.

If we determine the dc beta at the Q-point, we obtain

$$\beta_{dc} = \frac{I_C}{I_B} = \frac{2.7\ \text{mA}}{25\ \mu A} = \mathbf{108}$$

Although not exactly equal, the levels of β_{ac} and β_{dc} are usually reasonably close and are often used interchangeably. That is, if β_{ac} is known, it is assumed to be about the same magnitude as β_{dc}, and vice versa. Keep in mind that in the same lot, the value of β_{ac} will vary somewhat from one transistor to the next even though each transistor has the same number code. The variation may not be significant, but for the majority of applications, it is certainly sufficient to validate the approximate approach above. Generally, the smaller the level of I_{CEO}, the closer are the magnitudes of the two betas. Since the trend is toward lower and lower levels of I_{CEO}, the validity of the foregoing approximation is further substantiated.

If the characteristics had the appearance of those appearing in Fig. 3.18, the level of β_{ac} would be the same in every region of the characteristics. Note that the step in I_B is fixed at $10\ \mu A$ and the vertical spacing between curves is the same at every point in the characteristics—namely, 2 mA. Calculating the β_{ac} at the Q-point indicated results in

$$\beta_{ac} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}=\text{constant}} = \frac{9\ \text{mA} - 7\ \text{mA}}{45\ \mu A - 35\ \mu A} = \frac{2\ \text{mA}}{10\ \mu A} = \mathbf{200}$$

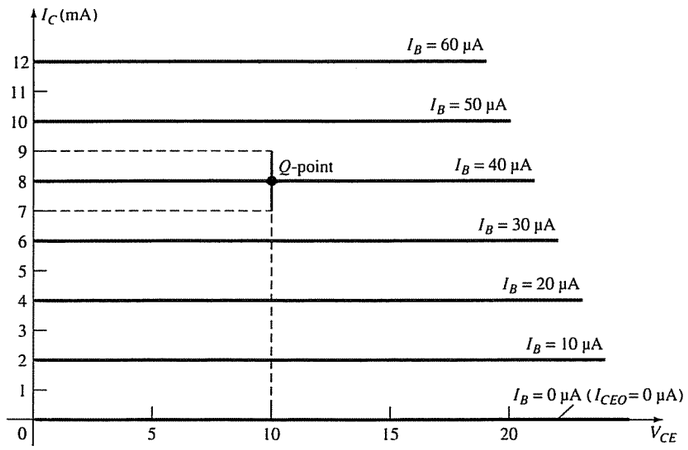


FIG. 3.18
Characteristics in which β_{ac} is the same everywhere and $\beta_{ac} = \beta_{dc}$.

Determining the dc beta at the same Q-point results in

$$\beta_{dc} = \frac{I_C}{I_B} = \frac{8\ \text{mA}}{40\ \mu A} = \mathbf{200}$$

revealing that if the characteristics have the appearance of Fig. 3.18, the magnitudes of β_{ac} and β_{dc} *will be the same* at every point on the characteristics. In particular, note that $I_{CEO} = 0\ \mu A$.

Although a true set of transistor characteristics will never have the exact appearance of Fig. 3.18, it does provide a set of characteristics for comparison with those obtained from a curve tracer (to be described shortly).

For the analysis to follow, the subscript dc or ac will not be included with β to avoid cluttering the expressions with unnecessary labels. For dc situations it will simply be recognized as β_{dc} and for any ac analysis as β_{ac}. If a value of β is specified for a particular transistor configuration, it will normally be used for both the dc and ac calculations.

A relationship can be developed between β and α using the basic relationships introduced thus far. Using $\beta = I_C/I_B$, we have $I_B = I_C/\beta$, and from $\alpha = I_C/I_E$ we have $I_E = I_C/\alpha$. Substituting into

$$I_E = I_C + I_B$$

we have

$$\frac{I_C}{\alpha} = I_C + \frac{I_C}{\beta}$$

and dividing both sides of the equation by I_C results in

$$\frac{1}{\alpha} = 1 + \frac{1}{\beta}$$

or

$$\beta = \alpha\beta + \alpha = (\beta + 1)\alpha$$

so that

$$\boxed{\alpha = \frac{\beta}{\beta + 1}} \tag{3.12a}$$

or

$$\boxed{\beta = \frac{\alpha}{1 - \alpha}} \tag{3.12b}$$

In addition, recall that

$$I_{CEO} = \frac{I_{CBO}}{1 - \alpha}$$

but using an equivalence of

$$\frac{1}{1 - \alpha} = \beta + 1$$

derived from the above, we find that

$$I_{CEO} = (\beta + 1)I_{CBO}$$

or

$$\boxed{I_{CEO} \cong \beta I_{CBO}} \tag{3.13}$$

as indicated on Fig. 3.14a. Beta is a particularly important parameter because it provides a direct link between current levels of the input and output circuits for a common-emitter configuration. That is,

$$\boxed{I_C = \beta I_B} \tag{3.14}$$

and since

$$I_E = I_C + I_B$$
$$= \beta I_B + I_B$$

we have

$$\boxed{I_E = (\beta + 1)I_B} \tag{3.15}$$

Both of the equations above play a major role in the analysis in Chapter 4.

Biasing

The proper biasing of a common-emitter amplifier can be determined in a manner similar to that introduced for the common-base configuration. Let us assume that we are presented with an *npn* transistor such as shown in Fig. 3.19a and asked to apply the proper biasing to place the device in the active region.

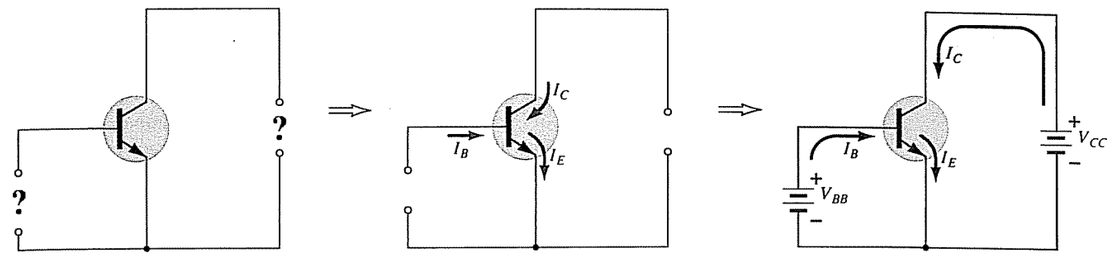


FIG. 3.19
Determining the proper biasing arrangement for a common-emitter npn transistor configuration.

The first step is to indicate the direction of I_E as established by the arrow in the transistor symbol as shown in Fig. 3.19b. Next, the other currents are introduced as shown, keeping in mind Kirchhoff's current law relationship: $I_C + I_B = I_E$. Finally, the supplies are introduced with polarities that will support the resulting directions of I_B and I_C as shown in Fig. 3.19c to complete the picture. The same approach can be applied to *pnp* transistors. If the transistor of Fig. 3.19 was a *pnp* transistor, all the currents and polarities of Fig. 3.19c would be reversed.

3.7 COMMON-COLLECTOR CONFIGURATION

The third and final transistor configuration is the *common-collector configuration*, shown in Fig. 3.20 with the proper current directions and voltage notation. The common-collector configuration is used primarily for impedance-matching purposes since it has a high input impedance and low output impedance, opposite to that of the common-base and common-emitter configurations.

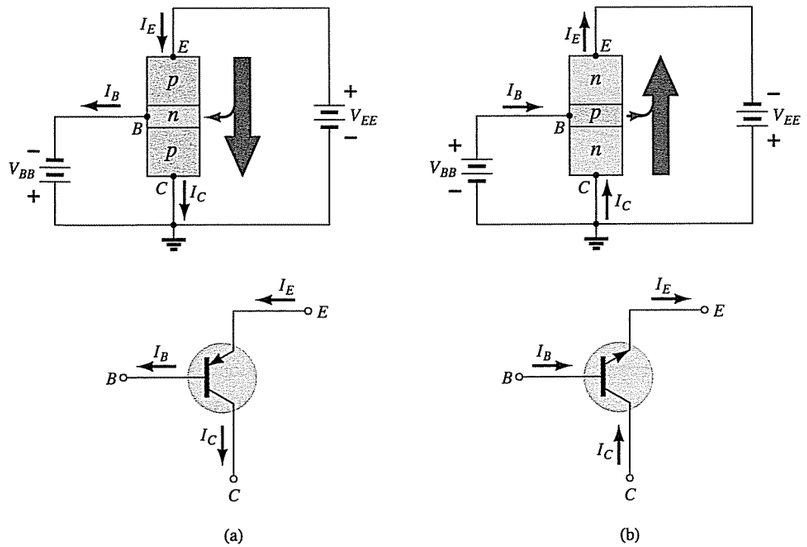


FIG. 3.20
Notation and symbols used with the common-collector configuration: (a) pnp transistor; (b) npn transistor.

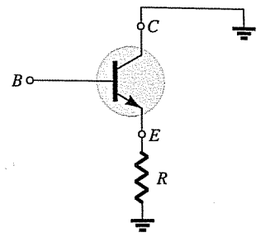


FIG. 3.21
Common-collector configuration used for impedance-matching purposes.

A common-collector circuit configuration is provided in Fig. 3.21 with the load resistor connected from emitter to ground. Note that the collector is tied to ground even though the transistor is connected in a manner similar to the common-emitter configuration. From a design viewpoint, there is no need for a set of common-collector characteristics to choose the parameters of the circuit of Fig. 3.21. It can be designed using the common-emitter characteristics of Section 3.6. For all practical purposes, the output characteristics of the common-collector configuration are the same as for the common-emitter configuration. For the common-collector configuration the output characteristics are a plot of I_E versus V_{CE} for a range of values of I_B. The input current, therefore, is the same for both the common-emitter and common-collector characteristics. The horizontal voltage axis for the common-collector configuration is obtained by simply changing the sign of the collector-to-emitter voltage of the common-emitter characteristics. Finally, there is an almost unnoticeable change in the vertical scale of I_C of the common-emitter characteristics if I_C is replaced by I_E for the common-collector characteristics (since $\alpha \cong 1$). For the input circuit of the common-collector configuration the common-emitter base characteristics are sufficient for obtaining the required information.

3.8 LIMITS OF OPERATION

For each transistor there is a region of operation on the characteristics that will ensure that the maximum ratings are not being exceeded and the output signal exhibits minimum distortion. Such a region has been defined for the transistor characteristics of Fig. 3.22. All of the limits of operation are defined on a typical transistor specification sheet described in Section 3.9.

Some of the limits of operation are self-explanatory, such as maximum collector current (normally referred to on the specification sheet as *continuous* collector current) and maximum collector-to-emitter voltage (often abbreviated as V_{CEO} or $V_{(BR)CEO}$ on the specification sheet). For the transistor of Fig. 3.22, $I_{C_{max}}$ was specified as 50 mA and V_{CEO} as 20 V. The vertical line on the characteristics defined as $V_{CE_{sat}}$ specifies the minimum V_{CE} that can be applied without falling into the nonlinear region labeled the *saturation* region. The level of $V_{CE_{sat}}$ is typically in the neighborhood of the 0.3 V specified for this transistor.

The maximum dissipation level is defined by the following equation:

$$P_{C_{max}} = V_{CE}I_C \tag{3.16}$$

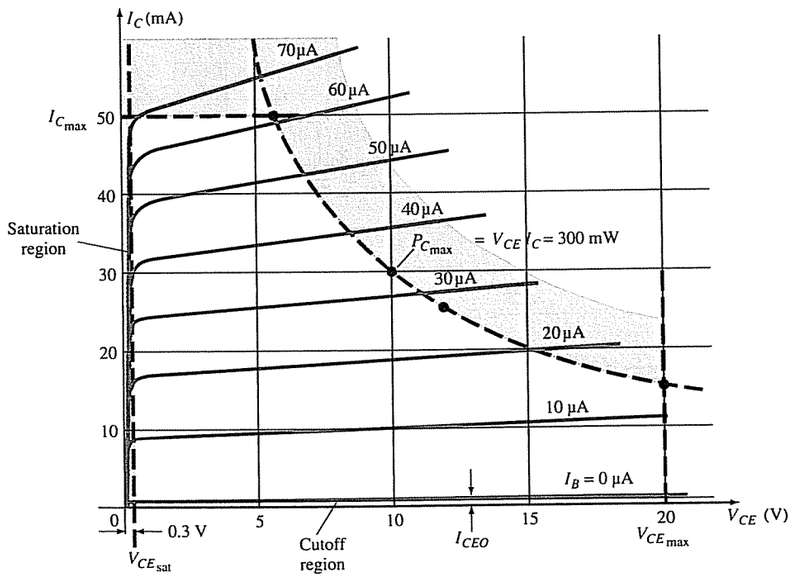


FIG. 3.22
Defining the linear (undistorted) region of operation for a transistor.

For the device of Fig. 3.22, the collector power dissipation was specified as 300 mW. The question then arises of how to plot the collector power dissipation curve specified by the fact that

$$P_{C_{max}} = V_{CE}I_C = 300\text{ mW}$$

or

$$V_{CE}I_C = 300\text{ mW}$$

At any point on the characteristics the product of V_{CE} and I_C must be equal to 300 mW. If we choose I_C to be the maximum value of 50 mA and substitute into the relationship above, we obtain

$$V_{CE}I_C = 300\text{ mW}$$
$$V_{CE}(50\text{ mA}) = 300\text{ mW}$$
$$V_{CE} = \frac{300\text{ mW}}{50\text{ mA}} = \mathbf{6\text{ V}}$$

As a result we find that if $I_C = 50$ mA, then $V_{CE} = 6$ V on the power dissipation curve as indicated in Fig. 3.22. If we now choose V_{CE} to be its maximum value of 20 V, the level of I_C is the following:

$$(20\text{ V})I_C = 300\text{ mW}$$
$$I_C = \frac{300\text{ mW}}{20\text{ V}} = \mathbf{15\text{ mA}}$$

defining a second point on the power curve.

If we now choose a level of I_C in the midrange such as 25 mA and solve for the resulting level of V_{CE}, we obtain

$$V_{CE}(25\text{ mA}) = 300\text{ mW}$$

and

$$V_{CE} = \frac{300\text{ mW}}{25\text{ mA}} = \mathbf{12\text{ V}}$$

as also indicated in Fig. 3.22.

A rough estimate of the actual curve can usually be drawn using the three points defined above. Of course, the more points one has, the more accurate is the curve, but a rough estimate is normally all that is required.

The *cutoff* region is defined as that region below $I_C = I_{CEO}$. This region must also be avoided if the output signal is to have minimum distortion. On some specification sheets only I_{CBO} is provided. One must then use the equation $I_{CEO} = \beta I_{CBO}$ to establish some idea of the cutoff level if the characteristic curves are unavailable. Operation in the resulting region of Fig. 3.22 will ensure minimum distortion of the output signal and current and voltage levels that will not damage the device.

If the characteristic curves are unavailable or do not appear on the specification sheet (as is often the case), one must simply be sure that I_C, V_{CE}, and their product $V_{CE}I_C$ fall into the following range:

$$\begin{gathered} I_{CEO} \leqq I_C \leqq I_{C_{max}} \\ V_{CE_{sat}} \leqq V_{CE} \leqq V_{CE_{max}} \\ V_{CE}I_C \leqq P_{C_{max}} \end{gathered} \tag{3.17}$$

For the common-base characteristics the maximum power curve is defined by the following product of output quantities:

$$P_{C_{max}} = V_{CB}I_C \tag{3.18}$$

3.9 TRANSISTOR SPECIFICATION SHEET

Since the specification sheet is the communication link between the manufacturer and user, it is particularly important that the information provided be recognized and correctly understood. Although all the parameters have not been introduced, a broad number will now

be familiar. The remaining parameters will be introduced in the chapters that follow. Reference will then be made to this specification sheet to review the manner in which the parameter is presented.

The information provided as Fig. 3.23 is taken directly from the *Small-Signal Transistors, FETs, and Diodes* publication prepared by Motorola Inc. The 2N4123 is a general-purpose *npn* transistor with the casing and terminal identification appearing in the top-right corner of Fig. 3.23a. Most specification sheets are broken down into *maximum ratings*, *thermal characteristics*, and *electrical characteristics*. The electrical characteristics are further broken down into "on," "off," and small-signal characteristics. The "on" and "off"

MAXIMUM RATINGS

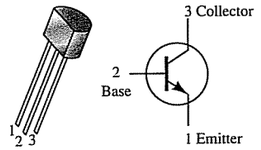
Rating	Symbol	2N4123	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
Collector-Base Voltage	V_{CBO}	40	Vdc
Emitter-Base Voltage	V_{EBO}	5.0	Vdc
Collector Current – Continuous	I_C	200	mAdc
Total Device Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	625 5.0	mW mW°C
Operating and Storage Junction Temperature Range	T_j, T_{stg}	–55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	83.3	°C W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C W

2N4123

CASE 29-04, STYLE 1
TO-92 (TO-226AA)



GENERAL PURPOSE TRANSISTOR
NPN SILICON

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted)

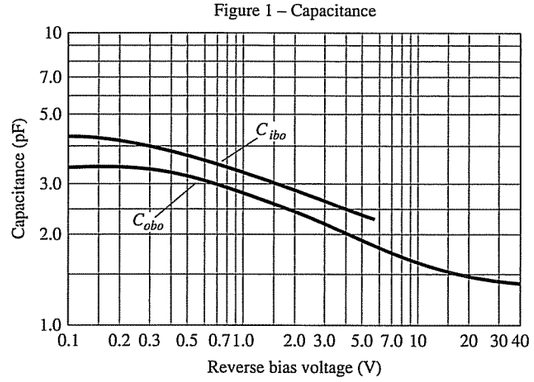
Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (1) ($I_C = 1.0$ mAdc, $I_E = 0$)	$V_{(BR)CEO}$	30		Vdc
Collector-Base Breakdown Voltage ($I_C = 10$ µAdc, $I_E = 0$)	$V_{(BR)CBO}$	40		Vdc
Emitter-Base Breakdown Voltage ($I_E = 10$ µAdc, $I_C = 0$)	$V_{(BR)EBO}$	5.0	–	Vdc
Collector Cutoff Current ($V_{CB} = 20$ Vdc, $I_E = 0$)	I_{CBO}	–	50	nAdc
Emitter Cutoff Current ($V_{BE} = 3.0$ Vdc, $I_C = 0$)	I_{EBO}	–	50	nAdc
ON CHARACTERISTICS				
DC Current Gain(1) ($I_C = 2.0$ mAdc, $V_{CE} = 1.0$ Vdc) ($I_C = 50$ mAdc, $V_{CE} = 1.0$ Vdc)	h_{FE}	50 25	150 –	–
Collector-Emitter Saturation Voltage(1) ($I_C = 50$ mAdc, $I_B = 5.0$ mAdc)	$V_{CE(sat)}$	–	0.3	Vdc
Base-Emitter Saturation Voltage(1) ($I_C = 50$ mAdc, $I_B = 5.0$ mAdc)	$V_{BE(sat)}$	–	0.95	Vdc
SMALL-SIGNAL CHARACTERISTICS				
Current-Gain – Bandwidth Product ($I_C = 10$ mAdc, $V_{CE} = 20$ Vdc, f = 100 MHz)	f_T	250		MHz
Output Capacitance ($V_{CB} = 5.0$ Vdc, $I_E = 0$, f = 100 MHz)	C_{obo}	–	4.0	pF
Input Capacitance ($V_{BE} = 0.5$ Vdc, $I_C = 0$, f = 100 kHz)	C_{ibo}	–	8.0	pF
Collector-Base Capacitance ($I_E = 0$, $V_{CB} = 5.0$ V, f = 100 kHz)	C_{cb}	–	4.0	pF
Small-Signal Current Gain ($I_C = 2.0$ mAdc, $V_{CE} = 10$ Vdc, f = 1.0 kHz)	h_{fe}	50	200	–
Current Gain – High Frequency ($I_C = 10$ mAdc, $V_{CE} = 20$ Vdc, f = 100 MHz) ($I_C = 2.0$ mAdc, $V_{CE} = 10$ V, f = 1.0 kHz)	h_{fe}	2.5 50	– 200	–
Noise Figure ($I_C = 100$ µAdc, $V_{CE} = 5.0$ Vdc, $R_S = 1.0$ k ohm, f = 1.0 kHz)	NF	–	6.0	dB

(1) Pulse Test: Pulse Width = 300 µs. Duty Cycle = 2.0%

(a)

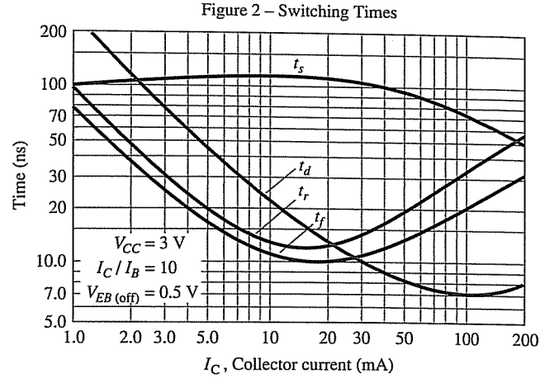
FIG. 3.23
Transistor specification sheet.

Figure 1 – Capacitance



(b)

Figure 2 – Switching Times



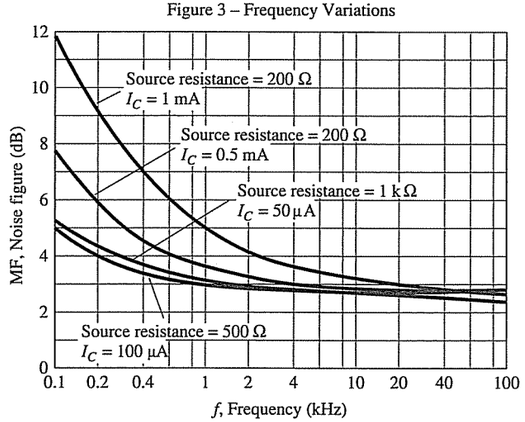
(c)

AUDIO SMALL SIGNAL CHARACTERISTICS

NOISE FIGURE

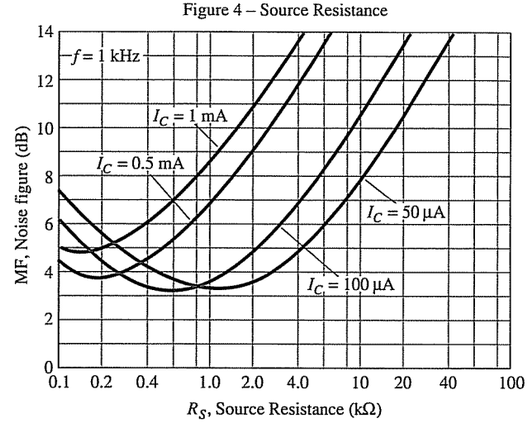
($V_{CE} = 5$ Vdc, $T_A = 25°C$)
Bandwidth = 1.0 Hz

Figure 3 – Frequency Variations



(d)

Figure 4 – Source Resistance

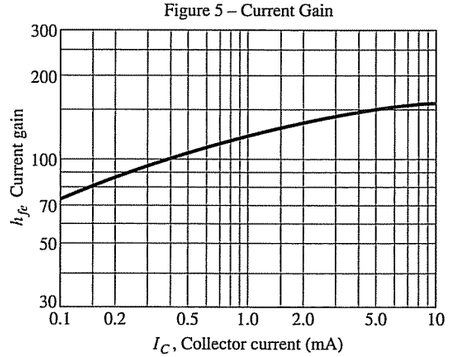


(e)

***h* PARAMETERS**

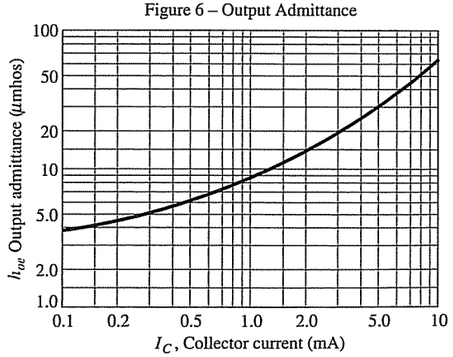
$V_{CE} = 10$ V, $f = 1$ kHz, $T_A = 25°C$

Figure 5 – Current Gain



(f)

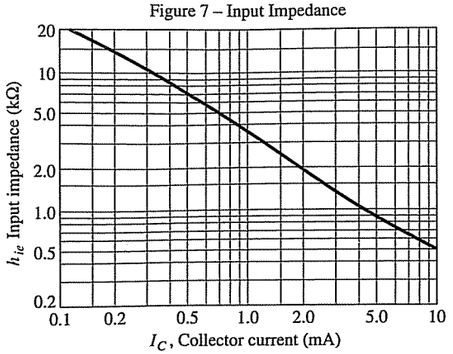
Figure 6 – Output Admittance



(g)

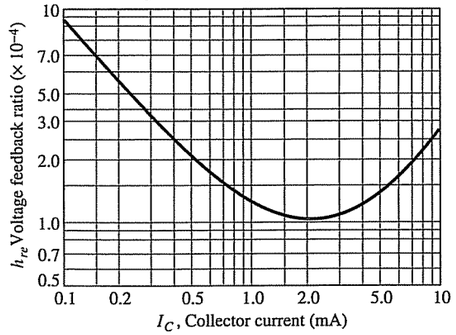
FIG. 3.23
Continued.

Figure 7 – Input Impedance



(h)

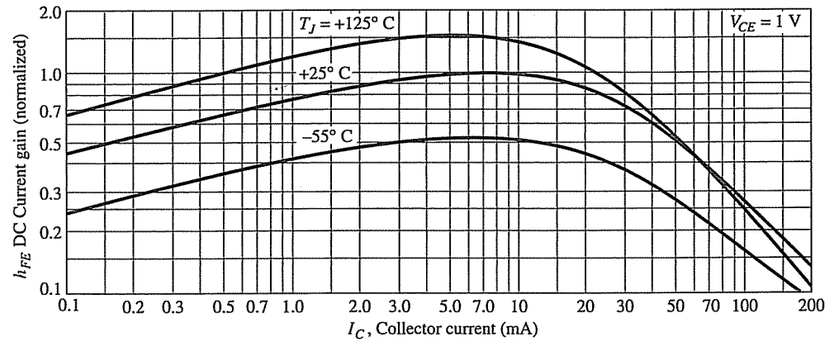
Figure 8 – Voltage Feedback Ratio



(i)

STATIC CHARACTERISTICS

Figure 9 – DC Current Gain



(j)

FIG. 3.23
Continued.

characteristics refer to dc limits, whereas the small-signal characteristics include the parameters of importance to ac operation.

Note in the maximum rating list that $V_{CE_{max}} = V_{CEO} = 30$ V with $I_{C_{max}} = 200$ mA. The maximum collector dissipation $P_{C_{max}} = P_D = 625$ mW. The derating factor under the maximum rating specifies that the maximum rating must be decreased 5 mW for every 1° rise in temperature above 25°C. In the "off" characteristics I_{CBO} is specified as 50 nA and in the "on" characteristics $V_{CE_{sat}} = 0.3$ V. The level of h_{FE} has a range of 50 to 150 at $I_C = 2$ mA and $V_{CE} = 1$ V and a minimum value of 25 at a higher current of 50 mA at the same voltage.

The limits of operation have now been defined for the device and are repeated below in the format of Eq. (3.17) using $h_{FE} = 150$ (the upper limit) and $I_{CEO} \cong \beta I_{CBO} = (150)(50\text{ nA}) = 7.5\ \mu\text{A}$. Certainly, for many applications the 7.5 μA = 0.0075 mA can be considered to be 0 mA on an approximate basis.

Limits of Operation

$$7.5\ \mu\text{A} \leqq I_C \leqq 200\text{ mA}$$
$$0.3\text{ V} \leqq V_{CE} \leqq 30\text{ V}$$
$$V_{CE} I_C \leqq 650\text{ mW}$$

In the small-signal characteristics the level of h_{fe} (β_{ac}) is provided along with a plot of how it varies with collector current in Fig. 3.23f. In Fig. 3.23j the effect of temperature and collector current on the level of h_{FE} (β_{ac}) is demonstrated. At room temperature (25°C), note that h_{FE} (β_{dc}) is a maximum value of 1 in the neighborhood of about 8 mA. As I_C increases beyond this level, h_{FE} drops off to one-half the value with I_C equal to 50 mA. It also drops to this level if I_C decreases to the low level of 0.15 mA. Since this is a *normalized* curve, if we have a transistor with $\beta_{dc} = h_{FE} = 50$ at room temperature, the maximum value at

8 mA is 50. At $I_C = 50$ mA it has dropped to 50/2 = 25. In other words, normalizing reveals that the actual level of h_{FE} at any level of I_C has been divided by the maximum value of h_{FE} at that temperature and $I_C = 8$ mA. Note also that the horizontal scale of Fig. 3.23j is a log scale. Log scales are examined in depth in Chapter 9. You may want to look back at the plots of this section when you find time to review the first few sections of Chapter 9.

Before leaving this description of the characteristics, note that the actual collector characteristics are not provided. In fact, most specification sheets provided by manufacturers fail to provide the full characteristics. It is expected that the data provided are sufficient to use the device effectively in the design process.

As noted in the introduction to this section, all the parameters of the specification sheet have not been defined in the preceding sections or chapters. However, the specification sheet provided in Fig. 3.23 will be referenced continually in the chapters to follow as parameters are introduced. The specification sheet can be a very valuable tool in the design or analysis mode, and every effort should be made to be aware of the importance of each parameter and how it may vary with changing levels of current, temperature, and so on.

3.10 TRANSISTOR TESTING

As with diodes, there are three routes one can take to check a transistor: use of a *curve tracer*, a *digital meter*, and an *ohmmeter.*

Curve Tracer

The curve tracer of Fig. 1.50 will provide the display of Fig. 3.24 once all the controls have been properly set. The smaller displays to the right reveal the scaling to be applied to the characteristics. The vertical sensitivity is 2 mA/div, resulting in the scale shown to the left of the monitor's display. The horizontal sensitivity is 1 V/div, resulting in the scale shown below the characteristics. The step function reveals that the curves are separated by a difference of 10 μA, starting at 0 μA for the bottom curve. The last scale factor provided can be used to quickly determine the β_{ac} for any region of the characteristics. Simply multiply the displayed factor by the number of divisions between I_B curves in the region of interest. For instance, let us determine β_{ac} at a Q-point of $I_C = 7$ mA and $V_{CE} = 5$ V. In this region

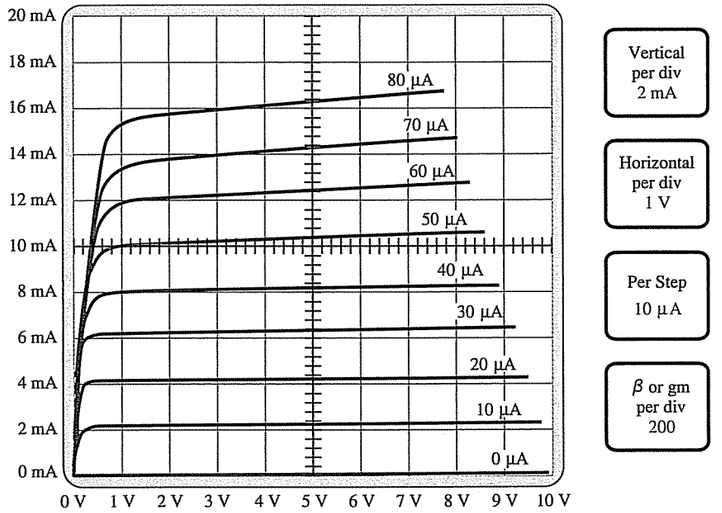


FIG. 3.24
Curve tracer response to 2N3904 npn transistor.

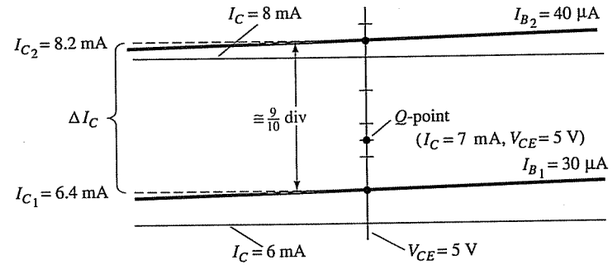


FIG. 3.25
Determining β_{ac} for the transistor characteristics of Fig. 3.24 at $I_C = 7$ mA and $V_{CE} = 5$ V.



FIG. 3.26
Transistor tester. (Courtesy of B+K Precision.)

of the display, the distance between I_B curves is $\frac{9}{10}$ of a division, as indicated on Fig. 3.25. Using the factor specified, we find that

$$\beta_{ac} = \frac{9}{10}\,\text{div}\left(\frac{200}{\text{div}}\right) = \mathbf{180}$$

Using Eq. (3.11) gives

$$\beta_{ac} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}=\text{constant}} = \frac{I_{C_1} - I_{C_1}}{I_{B_2} - I_{B_1}} = \frac{8.2\,\text{mA} - 6.4\,\text{mA}}{40\,\mu\text{A} - 30\,\mu\text{A}}$$
$$= \frac{1.8\,\text{mA}}{10\,\mu\text{A}} = \mathbf{180}$$

verifying the determination above.

Transistor Testers

There is a variety of transistor testers available. Some are simply part of a digital meter that can measure a wide variety elements in a network. Others, such as that in Fig. 3.26, are dedicated to testing a limited number of elements. The meter of Fig. 3.26 can be used to test Transistors, JFETs (Chapter 6) and SCRs (Chapter 17) in and out of the circuit. In all cases the power must first be turned off to the circuit in which the element appears to ensure that the internal battery of the tester is not damaged and to provide a correct reading. Once a transistor is inserted in the holder on the right, the switch on the right can be moved through all the possible combinations until the test light comes on and identifies the terminals of the transistor. The tester will also indicate an OK if the *npn* or *pnp* transistor is operating properly.

Any meter with a diode-checking capability can also be used to check the status of a transistor. With the collector open the base-to-emitter junction should result in a low voltage of about 0.7 V with the red (positive) lead connected to the base and the black (negative) lead connected to the emitter. A reversal of the leads should result in an OL indication to represent the reverse-biased junction. Similarly, with the emitter open, the forward- and reverse-bias states of the base-to-collector junction can be checked.

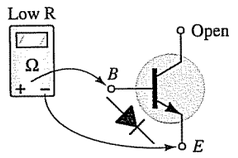


FIG. 3.27
Checking the forward-biased base-to-emitter junction of an npn transistor.

Ohmmeter

An ohmmeter or the resistance scales of a *d*igital *m*ulti*m*eter (DMM) can be used to check the state of a transistor. Recall that for a transistor in the active region the base-to-emitter junction is forward-biased and the base-to-collector junction is reverse-biased. Essentially, therefore, the forward-biased junction should register a relatively low resistance, whereas the reverse-biased junction shows a much higher resistance. For an *npn* transistor, the forward-biased junction (biased by the internal supply in the resistance mode) from base to emitter should be checked as shown in Fig. 3.27 and result in a reading that will typically fall in the range of 100 Ω to a few kilohms. The reverse-biased base-to-collector junction (again reverse-biased by the internal supply) should be checked as shown in Fig. 3.28 with a reading typically exceeding 100 kΩ. For a *pnp* transistor the leads are reversed for each junction. Obviously, a large or small resistance in both directions (reversing the leads) for either junction of an *npn* or *pnp* transistor indicates a faulty device.

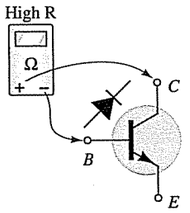


FIG. 3.28
Checking the reverse-biased base-to-collector junction of an npn transistor.

If both junctions of a transistor result in the expected readings, the type of transistor can also be determined by simply noting the polarity of the leads as applied to the base-emitter junction. If the positive (+) lead is connected to the base and the negative lead (−) to the emitter, a low resistance reading would indicate an *npn* transistor. A high resistance reading would indicate a *pnp* transistor. Although an ohmmeter can also be used to determine the leads (base, collector, and emitter) of a transistor, it is assumed that this determination can be made by simply looking at the orientation of the leads on the casing.

3.11 TRANSISTOR CASING AND TERMINAL IDENTIFICATION

After the transistor has been manufactured using one of the techniques described in Appendix A, leads of, typically, gold, aluminum, or nickel are then attached and the entire structure is encapsulated in a container such as that shown in Fig. 3.29. Those with the heavy-duty construction are high-power devices, whereas those with the small can (top hat) or plastic body are low- to medium-power devices.

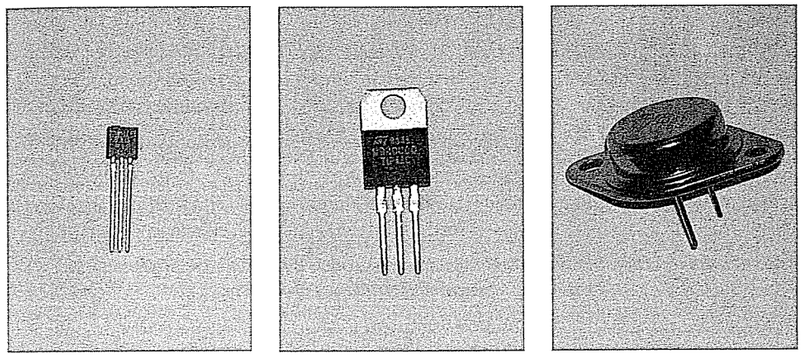


FIG. 3.29
Various types of general-purpose or switching transistors: (a) low power; (b) medium power; (c) medium to high power.

Whenever possible, the transistor casing will have some marking to indicate which leads are connected to the emitter, collector, or base of a transistor. A few of the methods commonly used are indicated in Fig. 3.30.

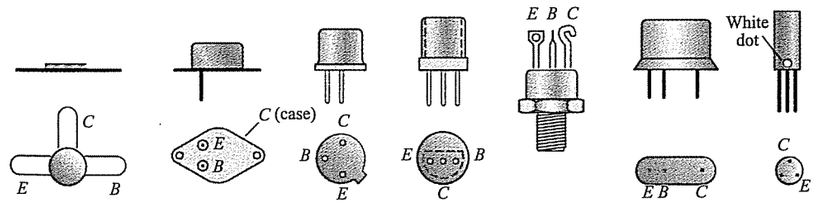


FIG. 3.30
Transistor terminal identification.

The internal construction of a TO-92 package in the Fairchild line appears in Fig. 3.31. Note the very small size of the actual semiconductor device. There are gold bond wires, a copper frame, and an epoxy encapsulation.

Four (quad) individual *pnp* silicon transistors can be housed in the 14-pin plastic dual-in-line package appearing in Fig. 3.32a. The internal pin connections appear in Fig. 3.32b. As with the diode IC package, the indentation in the top surface reveals the number 1 and 14 pins.

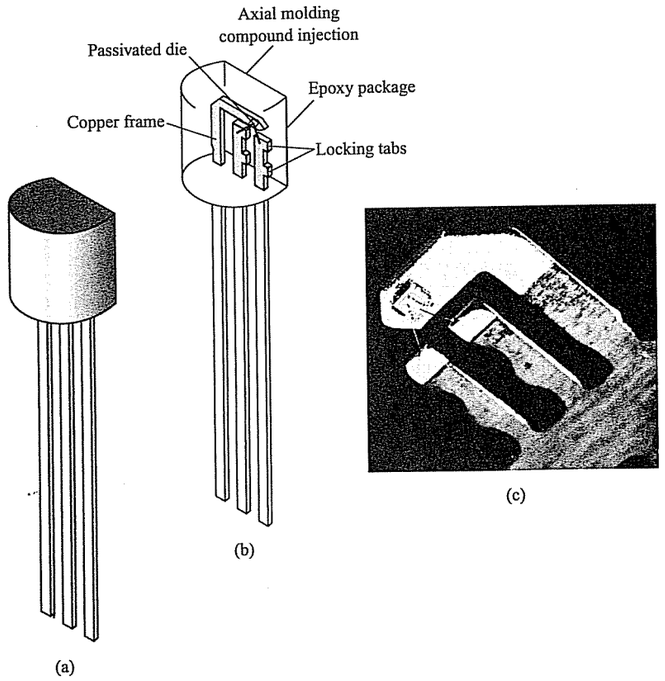


FIG. 3.31
Internal construction of a Fairchild transistor in a TO-92 package. (Courtesy Fairchild Camera and Instrument Corporation.)

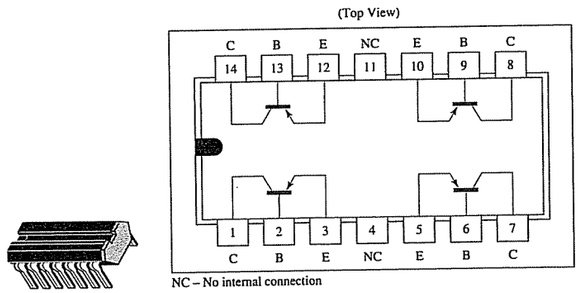


FIG. 3.32
Type Q2T2905 Texas Instruments quad pnp silicon transistor: (a) appearance; (b) pin connections. (Courtesy Texas Instruments Incorporated.)

3.12 SUMMARY

Important Conclusions and Concepts

1. Semiconductor devices have the following advantages over vacuum tubes: They are (1) of **smaller size**, (2) more **lightweight**, (3) more **rugged**, and (4) more **efficient**. In addition, they have (1) **no warm-up period**, (2) **no heater requirement**, and (3) **lower operating voltages**.

2. Transistors are **three-terminal devices** of three semiconductor layers having a base or center layer a great deal **thinner** than the other two layers. The outer two layers are both of either *n*- or *p*-type materials, with the sandwiched layer the opposite type.
3. One *p*–*n* junction of a transistor is **forward-biased**, whereas the other is **reverse-biased**.
4. The dc emitter current is always the **largest current** of a transistor, whereas the base current is always the **smallest**. The emitter current is always the **sum** of the other two.
5. The collector current is made up of **two components**: the **majority component** and the **minority current** (also called the ***leakage* current**).
6. The arrow in the transistor symbol defines the direction of **conventional current flow for the emitter current** and thereby defines the direction for the other currents of the device.
7. A three-terminal device needs **two sets of characteristics** to completely define its characteristics.
8. In the active region of a transistor, the base–emitter junction is **forward-biased**, whereas the collector–base junction is **reverse-biased**.
9. In the cutoff region the base–emitter and collector–base junctions of a transistor are **both reverse-biased**.
10. In the saturation region the base–emitter and collector–base junctions are **forward-biased**.
11. On an average basis, as a first approximation, the base-to-emitter voltage of an operating transistor can be assumed to be **0.7 V**.
12. The quantity alpha (α) relates the collector and emitter currents and is always close to **one**.
13. The impedance between terminals of a forward-biased junction is always relatively **small**, whereas the impedance between terminals of a reverse-biased junction is usually **quite large**.
14. The arrow in the symbol of an *npn* transistor points out of the device (**not** pointing **in**), whereas the arrow points in to the center of the symbol for a *pnp* transistor (pointing **in**).
15. For linear amplification purposes, cutoff for the common-emitter configuration will be defined by $I_C = I_{CEO}$.
16. The quantity beta (β) provides an important relationship between the base and collector currents, and is usually between **50 and 400**.
17. The dc beta is defined by a simple **ratio of dc currents at an operating point**, whereas the ac beta is **sensitive to the characteristics** in the region of interest. For most applications, however, the two are considered equivalent as a first approximation.
18. To ensure that a transistor is operating within its maximum power level rating, simply find the **product of the collector-to-emitter voltage and the collector current**, and compare it to the rated value.

Equations

$$I_E = I_C + I_B, \qquad I_C = I_{C_{\text{majority}}} + I_{CO_{\text{minority}}}, \qquad V_{BE} = 0.7\ \text{V}$$

$$\alpha_{\text{dc}} = \frac{I_C}{I_E}, \qquad \alpha_{\text{ac}} = \left.\frac{\Delta I_C}{\Delta I_E}\right|_{V_{CB}=\text{constant}}, \qquad I_{CEO} = \left.\frac{I_{CBO}}{1-\alpha}\right|_{I_B=0\,\mu\text{A}}$$

$$\beta_{\text{dc}} = \frac{I_C}{I_B}, \qquad \beta_{\text{ac}} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}=\text{constant}}, \qquad \alpha = \frac{\beta}{\beta+1}$$

$$I_C = \beta I_B, \qquad I_E = (\beta+1)I_B, \qquad P_{C_{\max}} = V_{CE}I_C$$

3.13 COMPUTER ANALYSIS

PSpice Windows

Since the transistor characteristics were introduced in this chapter, it seems appropriate that a procedure for obtaining those characteristics using PSpice Windows should be examined. The transistors are listed in the **EVAL** library and start with the letter **Q**. The library includes two *npn* transistors, two *pnp* transistors, and two Darlington configurations. The fact that there is a series of curves defined by the levels of I_B will require that a sweep of I_B values (a *nested sweep*) occur within a sweep of collector-to-emitter voltages. This is unnecessary for the diode, however, since only one curve would result.

First, the network in Fig. 3.33 is established using the same procedure as defined in Chapter 2. The voltage V_{CC} will establish our main sweep, whereas the voltage V_{BB} will determine the nested sweep. For future reference, note the panel at the top right of the menu bar with the scroll control when building networks. This option allows you to retrieve elements that have been used in the past. For instance, if you placed a resistor a few elements ago, simply return to the scroll bar and scroll until the resistor **R** appears. Click the location once, and the resistor will appear on the screen.

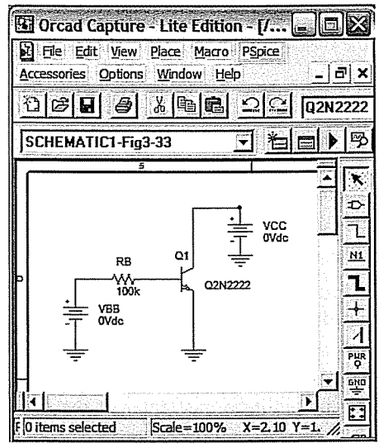


FIG. 3.33
Network employed to obtain the collector characteristics of the Q2N2222 transistor.

PSpice

Once the network is established as appearing in Fig. 3.33, select the **New Simulation Profile** and insert **Fig. 3-33** as the **Name**. Then select **Create** to obtain the **Simulation Settings** dialog box. The **Analysis type** will be **DC Sweep**, with the **Sweep variable** being a **Voltage Source**. Insert VCC as the name for the swept voltage source and select **Linear** for the sweep. The **Start value** is 0 V, the **End value** 10 V, and the **Increment** 0.01 V.

It is important not to select x in the top right corner of the box to leave the settings control. We must first enter the nested sweep variable by selecting **Secondary Sweep** and inserting VBB as the voltage source to be swept. Again, it will be a **Linear** sweep, but now the starting value will be 2.7 V to correspond with an initial current of 20 μA as determined by

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{2.7\,\text{V} - 0.7\,\text{V}}{100\,\text{k}\Omega} = 20\,\mu\text{A}$$

The **End value** is 10.7 V to correspond with a current of 100 μA. The **Increment** is set at 2 V, corresponding to a change in base current of 20 μA. Both sweeps are now set, but before leaving the dialog box **be sure both sweeps are enabled by a check in the box next to each sweep**. Often after entering the second sweep, the user fails to establish the second sweep before leaving the dialog box. Once both are selected, leave the dialog box and select **Initiate the simulation**. The result will be a graph with a voltage **VCC** varying from

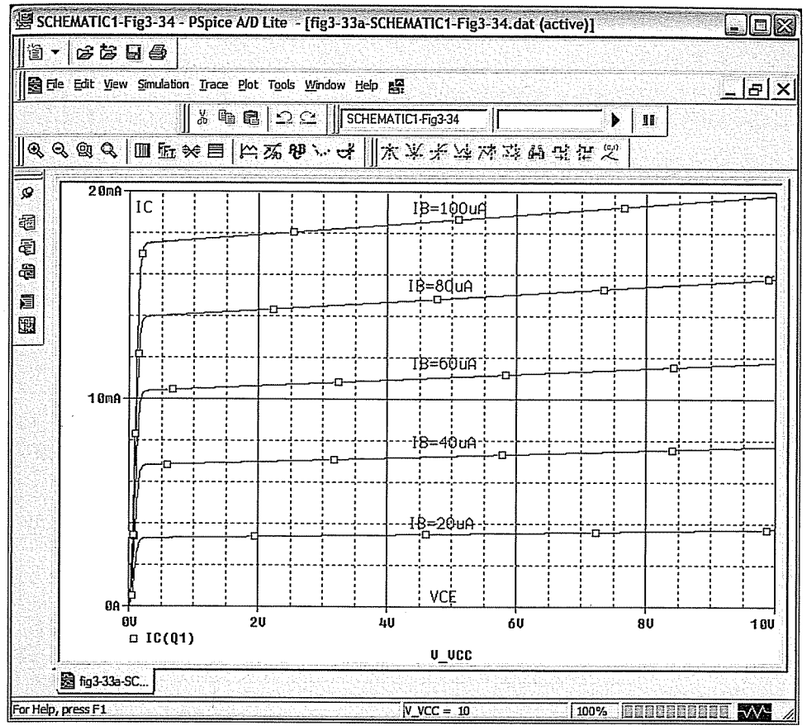


FIG. 3.34
Collector characteristics for the transistor of Fig. 3.33.

0 V to 10 V. To establish the various I curves, apply the sequence **Trace-Add Trace** to obtain the **Add Trace** dialog box. Select **IC(Q1)**, the collector current of the transistor for the vertical axis. An **OK**, and the characteristics will appear. Unfortunately, however, they extend from −10 mA to +20 mA on the vertical axis. This can be corrected by the sequence **Plot-Axis Settings**, which again will result in the **Axis Settings** dialog box. Select **Y-Axis** and under **Data Range** choose **User Defined** and set the range as 0–20 mA. An **OK**, and the plot of Fig. 3.34 will appear. The labels on the plot can be added through the sequence **Plot-Label-Text** to obtain the **Text Label** dialog box. Enter **IB** = 20 μA followed by **OK** and it will appear in red on the screen. Click it in place and click it once more to set it in memory. Repeat for all the other labels of the figure.

If the ac beta is determined in the middle of the graph, you will find that its value is about 190, even though Bf in the list of specifications is 255.9. Again, like the diode, the other parameters of the device will have a noticeable effect on the operating conditions. If we return to the transistor specifications using **Edit-PSpice Model** to obtain the **PSpice Model Editor Lite** dialog box, we can delete all the parameters except the Bf value. Be sure to leave the parentheses surrounding the value of Bf during the deletion process. When you exit the box the **Model Editor/9.2** dialog box will appear asking you to save changes. It was saved as **Fig. 3-33** and the circuit was simulated again to obtain the characteristics of Fig. 3.35 following another adjustment of the range of the vertical axis.

Note first that the curves are all horizontal, meaning the element is void of any resistive characteristics. In addition, the equal spacing of the curves throughout reveals that beta is the same everywhere. Using a difference of 5 mA between any two curves and dividing by the difference in I_B of 20 μA results in a β of 250, which is essentially the same as that specified for the device. The real value of the above procedure is to recognize that even though beta may be provided, the actual performance of the device will be very dependent on its other parameters. Assume an ideal device is always a good starting point, but an actual network provides a different set of results.

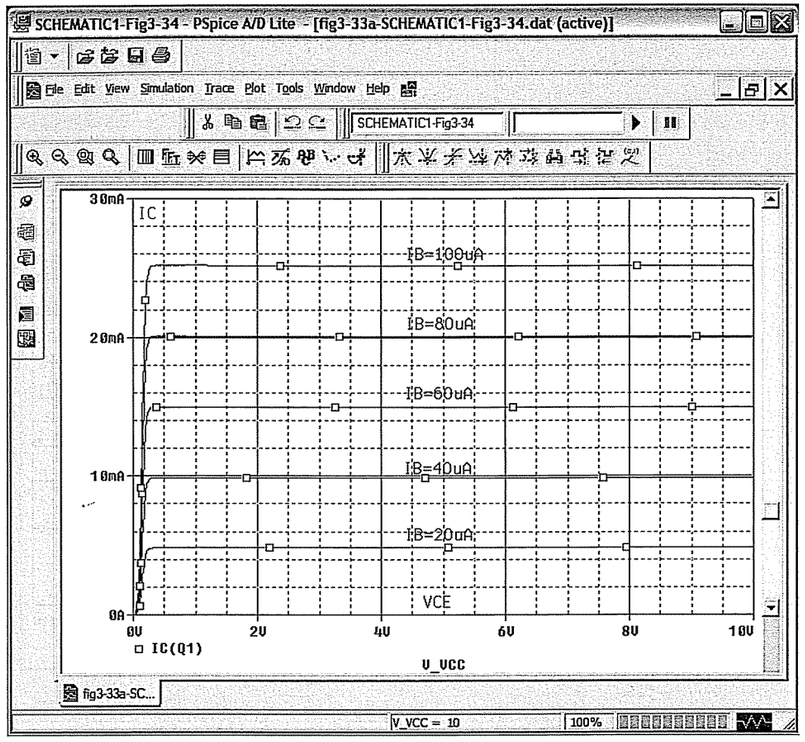


FIG. 3.35

Ideal collector characteristics for the transistor of Fig. 3.33.

PROBLEMS

**Note:* Asterisks indicate more difficult problems.

3.2 Transistor Construction

1. What names are applied to the two types of BJT transistors? Sketch the basic construction of each and label the various minority and majority carriers in each. Draw the graphic symbol next to each. Is any of this information altered by changing from a silicon to a germanium base?
2. What is the major difference between a bipolar and a unipolar device?

3.3 Transistor Operation

3. How must the two transistor junctions be biased for proper transistor amplifier operation?
4. What is the source of the leakage current in a transistor?
5. Sketch a figure similar to Fig. 3.3 for the forward-biased junction of an *npn* transistor. Describe the resulting carrier motion.
6. Sketch a figure similar to Fig. 3.4 for the reverse-biased junction of an *npn* transistor. Describe the resulting carrier motion.
7. Sketch a figure similar to Fig. 3.5 for the majority- and minority-carrier flow of an *npn* transistor. Describe the resulting carrier motion.
8. Which of the transistor currents is always the largest? Which is always the smallest? Which two currents are relatively close in magnitude?
9. If the emitter current of a transistor is 8 mA and I_B is 1/100 of I_C, determine the levels of I_C and I_B.

3.4 Common-Base Configuration

10. From memory, sketch the transistor symbol for a *pnp* and an *npn* transistor, and then insert the conventional flow direction for each current.

11. Using the characteristics of Fig. 3.7, determine V_{BE} at $I_E = 5$ mA for $V_{CB} = 1$, 10, and 20 V. Is it reasonable to assume on an approximate basis that V_{CB} has only a slight effect on the relationship between V_{BE} and I_E?
12. **a.** Determine the average ac resistance for the characteristics of Fig. 3.10b.
    b. For networks in which the magnitude of the resistive elements is typically in kilohms, is the approximation of Fig. 3.10c a valid one [based on the results of part (a)]?
13. **a.** Using the characteristics of Fig. 3.8, determine the resulting collector current if $I_E = 4.5$ mA and $V_{CB} = 4$ V.
    b. Repeat part (a) for $I_E = 4.5$ mA and $V_{CB} = 16$ V.
    c. How have the changes in V_{CB} affected the resulting level of I_C?
    d. On an approximate basis, how are I_E and I_C related based on the results above?
14. **a.** Using the characteristics of Figs. 3.7 and 3.8, determine I_C if $V_{CB} = 10$ V and $V_{BE} = 800$ mV.
    b. Determine V_{BE} if $I_C = 5$ mA and $V_{CB} = 10$ V.
    c. Repeat part (b) using the characteristics of Fig. 3.10b.
    d. Repeat part (b) using the characteristics of Fig. 3.10c.
    e. Compare the solutions for V_{BE} for parts (b) through (d). Can the difference be ignored if voltage levels greater than a few volts are typically encountered?
15. **a.** Given an α_{dc} of 0.998, determine I_C if $I_E = 4$ mA.
    b. Determine α_{dc} if $I_E = 2.8$ mA and $I_B = 20$ μA.
    c. Find I_E if $I_B = 40$ μA and α_{dc} is 0.98.
16. From memory only, sketch the common-base BJT transistor configuration (for *npn* and *pnp*) and indicate the polarity of the applied bias and resulting current directions.

3.5 Transistor Amplifying Action

17. Calculate the voltage gain ($A_v = V_L/V_i$) for the network of Fig. 3.12 if $V_i = 500$ mV and $R = 1$ kΩ. (The other circuit values remain the same.)
18. Calculate the voltage gain ($A_v = V_L/V_i$) for the network of Fig. 3.12 if the source has an internal resistance of 100 Ω in series with V_i.

3.6 Common-Emitter Configuration

19. Define I_{CBO} and I_{CEO}. How are they different? How are they related? Are they typically close in magnitude?
20. Using the characteristics of Fig. 3.14:
    a. Find the value of I_C corresponding to $V_{BE} = +750$ mV and $V_{CE} = +5$ V.
    b. Find the value of V_{CE} and V_{BE} corresponding to $I_C = 3$ mA and $I_B = 30$ μA.

*21. **a.** For the common-emitter characteristics of Fig. 3.14, find the dc beta at an operating point of $V_{CE} = +8$ V and $I_C = 2$ mA.
    b. Find the value of α corresponding to this operating point.
    c. At $V_{CE} = +8$ V, find the corresponding value of I_{CEO}.
    d. Calculate the approximate value of I_{CBO} using the dc beta value obtained in part (a).

*22. **a.** Using the characteristics of Fig. 3.14a, determine I_{CEO} at $V_{CE} = 10$ V.
    b. Determine β_{dc} at $I_B = 10$ μA and $V_{CE} = 10$ V.
    c. Using the β_{dc} determined in part (b), calculate I_{CBO}.

23. **a.** Using the characteristics of Fig. 3.14a, determine β_{dc} at $I_B = 80$ μA and $V_{CE} = 5$ V.
    b. Repeat part (a) at $I_B = 5$ μA and $V_{CE} = 15$ V.
    c. Repeat part (a) at $I_B = 30$ μA and $V_{CE} = 10$ V.
    d. Reviewing the results of parts (a) through (c), does the value of β_{dc} change from point to point on the characteristics? Where were the higher values found? Can you develop any general conclusions about the value of β_{dc} on a set of characteristics such as those provided in Fig. 3.14a?

*24. **a.** Using the characteristics of Fig. 3.14a, determine β_{ac} at $I_B = 80$ μA and $V_{CE} = 5$ V.
    b. Repeat part (a) at $I_B = 5$ μA and $V_{CE} = 15$ V.
    c. Repeat part (a) at $I_B = 30$ μA and $V_{CE} = 10$ V.
    d. Reviewing the results of parts (a) through (c), does the value of β_{ac} change from point to point on the characteristics? Where are the high values located? Can you develop any general conclusions about the value of β_{ac} on a set of collector characteristics?
    e. The chosen points in this exercise are the same as those employed in Problem 23. If Problem 23 was performed, compare the levels of β_{dc} and β_{ac} for each point and comment on the trend in magnitude for each quantity.

25. Using the characteristics of Fig. 3.14a, determine β_{dc} at $I_B = 25$ μA and $V_{CE} = 10$ V. Then calculate α_{dc} and the resulting level of I_E. (Use the level of I_C determined by $I_C = \beta_{dc} I_B$.)

26. **a.** Given that $\alpha_{dc} = 0.987$, determine the corresponding value of β_{dc}.
b. Given $\beta_{dc} = 120$, determine the corresponding value of α.
c. Given that $\beta_{dc} = 180$ and $I_C = 2.0$ mA, find I_E and I_B.

27. From memory only, sketch the common-emitter configuration (for *npn* and *pnp*) and insert the proper biasing arrangement with the resulting current directions for I_B, I_C, and I_E.

3.7 Common-Collector Configuration

28. An input voltage of 2 V rms (measured from base to ground) is applied to the circuit of Fig. 3.21. Assuming that the emitter voltage follows the base voltage exactly and that V_{be} (rms) = 0.1 V, calculate the circuit voltage amplification ($A_v = V_o/V_i$) and emitter current for $R_E = 1\ \text{k}\Omega$.

29. For a transistor having the characteristics of Fig. 3.14, sketch the input and output characteristics of the common-collector configuration.

3.8 Limits of Operation

30. Determine the region of operation for a transistor having the characteristics of Fig. 3.14 if $I_{C_{max}} = 7$ mA, $V_{CE_{max}} = 17$ V, and $P_{C_{max}} = 40$ mW.

31. Determine the region of operation for a transistor having the characteristics of Fig. 3.8 if $I_{C_{max}} = 6$ mA, $V_{CB_{max}} = 15$ V, and $P_{C_{max}} = 30$ mW.

3.9 Transistor Specification Sheet

32. Referring to Fig. 3.23, determine the temperature range for the device in degrees Fahrenheit.

33. Using the information provided in Fig. 3.23 regarding $P_{D_{max}}$, $V_{CE_{max}}$, $I_{C_{max}}$ and $V_{CE_{sat}}$, sketch the boundaries of operation for the device.

34. Based on the data of Fig. 3.23, what is the expected value of I_{CEO} using the average value of β_{dc}?

35. How does the range of h_{FE} (Fig. 3.23j, normalized from $h_{FE} = 100$) compare with the range of h_{fe} (Fig. 3.23f) for the range of I_C from 0.1 to 10 mA?

36. Using the characteristics of Fig. 3.23b, determine whether the input capacitance in the common-base configuration increases or decreases with increasing levels of reverse-bias potential. Can you explain why?

***37.** Using the characteristics of Fig. 3.23f, determine how much the level of h_{fe} has changed from its value at 1 mA to its value at 10 mA. Note that the vertical scale is a log scale that may require reference to Section 11.2. Is the change one that should be considered in a design situation?

***38.** Using the characteristics of Fig. 3.23j, determine the level of β_{dc} at $I_C = 10$ mA at the three levels of temperature appearing in the figure. Is the change significant for the specified temperature range? Is it an element to be concerned about in the design process?

3.10 Transistor Testing

39. **a.** Using the characteristics of Fig. 3.24, determine β_{ac} at $I_C = 14$ mA and $V_{CE} = 3$ V.
b. Determine β_{dc} at $I_C = 1$ mA and $V_{CE} = 8$ V.
c. Determine β_{ac} at $I_C = 14$ mA and $V_{CE} = 3$ V.
d. Determine β_{dc} at $I_C = 1$ mA and $V_{CE} = 8$ V.
e. How does the level of β_{ac} and β_{dc} compare in each region?
f. Is the approximation $\beta_{dc} \cong \beta_{ac}$ a valid one for this set of characteristics?

DC Biasing—BJTs

4

CHAPTER OUTLINE

4.1 Introduction
4.2 Operating Point
4.3 Fixed-Bias Circuit
4.4 Emitter Bias
4.5 Voltage-Divider Bias
4.6 DC Bias with Voltage Feedback
4.7 Miscellaneous Bias Configurations
4.8 Design Operations
4.9 Transistor Switching Networks
4.10 Troubleshooting Techniques
4.11 *pnp* Transistors
4.12 Bias Stabilization
4.13 Practical Applications
4.14 Summary
4.15 Computer Analysis

4.1 INTRODUCTION

The analysis or design of a transistor amplifier requires a knowledge of both the dc and the ac response of the system. Too often it is assumed that the transistor is a magical device that can raise the level of the applied ac input without the assistance of an external energy source. In actuality,

the improved output ac power level is the result of a transfer of energy from the applied dc supplies.

The analysis or design of any electronic amplifier therefore has two components: the dc portion and the ac portion. Fortunately, the superposition theorem is applicable and the investigation of the dc conditions can be totally separated from the ac response. However, one must keep in mind that during the design or synthesis stage the choice of parameters for the required dc levels will affect the ac response, and vice versa.

The dc level of operation of a transistor is controlled by a number of factors, including the range of possible operating points on the device characteristics. In Section 4.2 we specify the range for the bipolar junction transistor (BJT) amplifier. Once the desired dc current and voltage levels have been defined, a network must be constructed that will establish the desired operating point. A number of these networks are analyzed in this chapter. Each

design will also determine the stability of the system, that is, how sensitive the system is to temperature variations, another topic to be investigated in a later section of this chapter.

Although a number of networks are analyzed in this chapter, there is an underlying similarity in the analysis of each configuration due to the recurring use of the following important basic relationships for a transistor:

$$\boxed{V_{BE} = 0.7\,\text{V}} \tag{4.1}$$

$$\boxed{I_E = (\beta + 1)I_B \cong I_C} \tag{4.2}$$

$$\boxed{I_C = \beta I_B} \tag{4.3}$$

In fact, once the analysis of the first few networks is clearly understood, the path toward the solution of the networks to follow will begin to become quite apparent. In most instances the base current I_B is the first quantity to be determined. Once I_B is known, the relationships of Eqs. (4.1) through (4.3) can be applied to find the remaining quantities of interest. The similarities in analysis will be immediately obvious as we progress through the chapter. The equations for I_B are so similar for a number of configurations that one equation can be derived from another simply by dropping or adding a term or two. The primary function of this chapter is to develop a level of familiarity with the BJT transistor that would permit a dc analysis of any system that might employ the BJT amplifier.

4.2 OPERATING POINT

The term *biasing* appearing in the title of this chapter is an all-inclusive term for the application of dc voltages to establish a fixed level of current and voltage. For transistor amplifiers the resulting dc current and voltage establish an *operating point* on the characteristics that define the region that will be employed for amplification of the applied signal. Since the operating point is a fixed point on the characteristics, it is also called the *quiescent point* (abbreviated Q-point). By definition, *quiescent* means quiet, still, inactive. Figure 4.1 shows

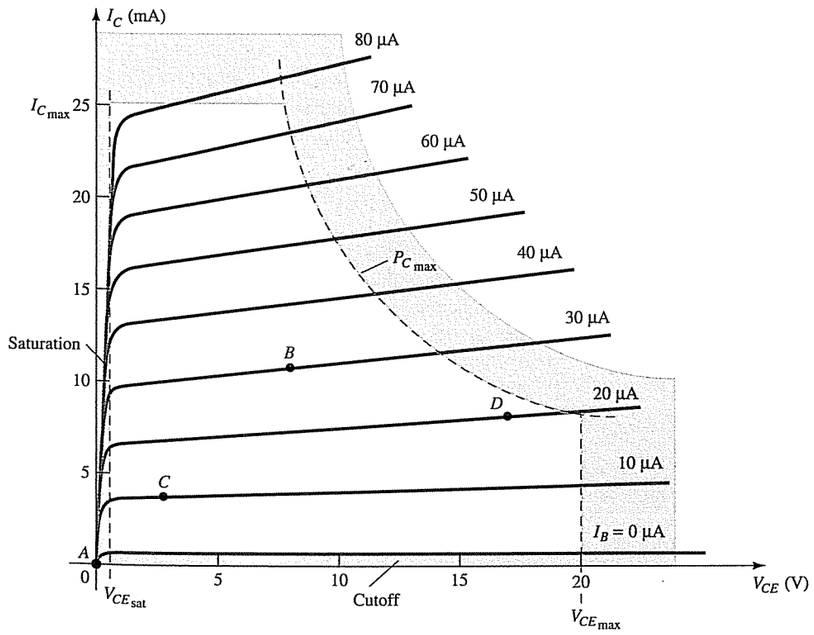


FIG. 4.1
Various operating points within the limits of operation of a transistor.

a general output device characteristic with four operating points indicated. The biasing circuit can be designed to set the device operation at any of these points or others within the *active region.* The maximum ratings are indicated on the characteristics of Fig. 4.1 by a horizontal line for the maximum collector current $I_{C_{max}}$ and a vertical line at the maximum collector-to-emitter voltage $V_{CE_{max}}$. The maximum power constraint is defined by the curve $P_{C_{max}}$ in the same figure. At the lower end of the scales are the *cutoff region*, defined by $I_B \leq 0\,\mu\text{A}$, and the *saturation region*, defined by $V_{CE} \leq V_{CE_{sat}}$.

The BJT device could be biased to operate outside these maximum limits, but the result of such operation would be either a considerable shortening of the lifetime of the device or destruction of the device. Confining ourselves to the *active* region, we can select many different operating areas or points. The chosen Q-point often depends on the intended use of the circuit. Still, we can consider some differences among the various points shown in Fig. 4.1 to present some basic ideas about the operating point and, thereby, the bias circuit.

If no bias were used, the device would initially be completely off, resulting in a Q-point at A—namely, zero current through the device (and zero voltage across it). Since it is necessary to bias a device so that it can respond to the entire range of an input signal, point A would not be suitable. For point B, if a signal is applied to the circuit, the device will vary in current and voltage from the operating point, allowing the device to react to (and possibly amplify) both the positive and negative excursions of the input signal. If the input signal is properly chosen, the voltage and current of the device will vary but not enough to drive the device into *cutoff* or *saturation.* Point C would allow some positive and negative variation of the output signal, but the peak-to-peak value would be limited by the proximity of $V_{CE} = 0\,\text{V}$ and $I_C = 0\,\text{mA}$. Operating at point C also raises some concern about the nonlinearities introduced by the fact that the spacing between I_B curves is rapidly changing in this region. In general, it is preferable to operate where the gain of the device is fairly constant (or linear) to ensure that the amplification over the entire swing of input signal is the same. Point B is a region of more linear spacing and therefore more linear operation, as shown in Fig. 4.1. Point D sets the device operating point near the maximum voltage and power level. The output voltage swing in the positive direction is thus limited if the maximum voltage is not to be exceeded. Point B therefore seems the best operating point in terms of linear gain and largest possible voltage and current swing. This is usually the desired condition for small-signal amplifiers (Chapter 5) but not the case necessarily for power amplifiers, which will be considered in Chapter 12. In this discussion, we will be concentrating primarily on biasing the transistor for *small-signal* amplification operation.

One other very important biasing factor must be considered. Having selected and biased the BJT at a desired operating point, we must also take the effect of temperature into account. Temperature causes the device parameters such as the transistor current gain (β_{ac}) and the transistor leakage current (I_{CEO}) to change. Higher temperatures result in increased leakage currents in the device, thereby changing the operating condition set by the biasing network. The result is that the network design must also provide a degree of *temperature stability* so that temperature changes result in minimum changes in the operating point. This maintenance of the operating point can be specified by a *stability factor S,* which indicates the degree of change in operating point due to a temperature variation. A highly stable circuit is desirable, and the stability of a few basic bias circuits will be compared.

For the BJT to be biased in its linear or active operating region the following must be true:

1. ***The base–emitter junction* must *be forward-biased* (p-*region voltage more* positive), *with a resulting forward-bias voltage of about 0.6 to 0.7 V.***
2. ***The base–collector junction* must *be reverse-biased* (n-*region more* positive), *with the reverse-bias voltage being any value within the maximum limits of the device.***

[Note that for forward bias the voltage across the p–n junction is p-positive, whereas for reverse bias it is opposite (reverse) with n-positive. This emphasis on the initial letter should provide a means of helping memorize the necessary voltage polarity.]

Operation in the cutoff, saturation, and linear regions of the BJT characteristic are provided as follows:

1. *Linear-region operation:*
   Base–emitter junction forward-biased
   Base–collector junction reverse-biased

2. *Cutoff-region operation:*
   Base–emitter junction reverse-biased
   Base–collector junction reverse-biased
3. *Saturation-region operation:*
   Base–emitter junction forward-biased
   Base–collector junction forward-biased

4.3 FIXED-BIAS CIRCUIT

The fixed-bias circuit of Fig. 4.2 is the simplest transistor dc bias configuration. Even though the network employs an *npn* transistor, the equations and calculations apply equally well to a *pnp* transistor configuration merely by changing all current directions and voltage polarities. The current directions of Fig. 4.2 are the *actual* current directions, and the voltages are defined by the standard double-subscript notation. For the dc analysis the network can be isolated from the indicated ac levels by replacing the capacitors with an open-circuit equivalent because the reactance of a capacitor for dc is $X_C = 1/2\pi fC = 1/2\pi(0)C = \infty\ \Omega$. In addition, the dc supply V_{CC} can be separated into two supplies (for analysis purposes only) as shown in Fig. 4.3 to permit a separation of input and output circuits. It also reduces the linkage between the two to the base current I_B. The separation is certainly valid, as we note in Fig. 4.3 that V_{CC} is connected directly to R_B and R_C just as in Fig. 4.2.

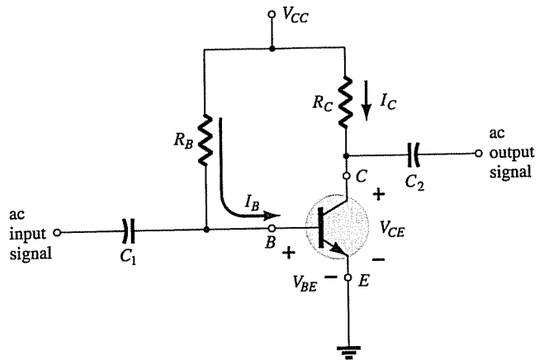


FIG. 4.2
Fixed-bias circuit.

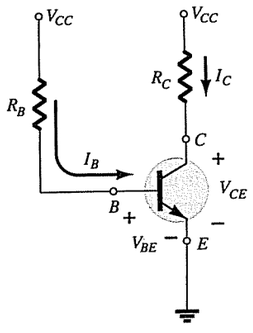


FIG. 4.3
DC equivalent of Fig. 4.2.

Forward Bias of Base–Emitter

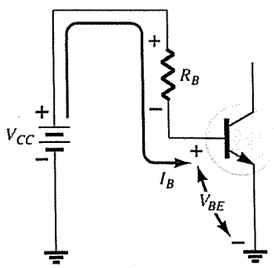


FIG. 4.4
Base–emitter loop.

Consider first the base–emitter circuit loop of Fig. 4.4. Writing Kirchhoff's voltage equation in the clockwise direction for the loop, we obtain

$$+V_{CC} - I_B R_B - V_{BE} = 0$$

Note the polarity of the voltage drop across R_B as established by the indicated direction of I_B. Solving the equation for the current I_B results in the following:

$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B}} \tag{4.4}$$

Equation (4.4) is certainly not a difficult one to remember if one simply keeps in mind that the base current is the current through R_B and by Ohm's law that current is the voltage across R_B divided by the resistance R_B. The voltage across R_B is the applied voltage V_{CC} at one end less the drop across the base-to-emitter junction (V_{BE}). In addition, since the supply voltage V_{CC} and the base–emitter voltage V_{BE} are constants, the selection of a base resistor R_B sets the level of base current for the operating point.

Collector–Emitter Loop

The collector–emitter section of the network appears in Fig. 4.5 with the indicated direction of current I_C and the resulting polarity across R_C. The magnitude of the collector current is related directly to I_B through

$$\boxed{I_C = \beta I_B} \tag{4.5}$$

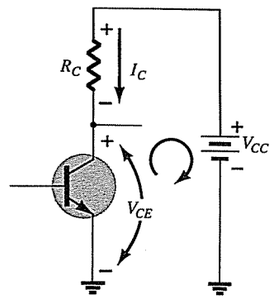


FIG. 4.5
Collector–emitter loop.

It is interesting to note that since the base current is controlled by the level of R_B and I_C is related to I_B by a constant β, the magnitude of I_C is not a function of the resistance R_C. Changing R_C to any level will not affect the level of I_B or I_C as long as we remain in the active region of the device. However, as we shall see, the level of R_C will determine the magnitude of V_{CE}, which is an important parameter.

Applying Kirchhoff's voltage law in the clockwise direction around the indicated closed loop of Fig. 4.5 results in the following:

$$V_{CE} + I_C R_C - V_{CC} = 0$$

and

$$\boxed{V_{CE} = V_{CC} - I_C R_C} \tag{4.6}$$

which states that the voltage across the collector–emitter region of a transistor in the fixed-bias configuration is the supply voltage less the drop across R_C.

As a brief review of single- and double-subscript notation recall that

$$\boxed{V_{CE} = V_C - V_E} \tag{4.7}$$

where V_{CE} is the voltage from collector to emitter and V_C and V_E are the voltages from collector and emitter to ground, respectively. *In this case,* since $V_E = 0$ V, we have

$$\boxed{V_{CE} = V_C} \tag{4.8}$$

In addition, since

$$\boxed{V_{BE} = V_B - V_E} \tag{4.9}$$

and $V_E = 0$ V, then

$$\boxed{V_{BE} = V_B} \tag{4.10}$$

Keep in mind that voltage levels such as V_{CE} are determined by placing the red (positive) lead of the voltmeter at the collector terminal with the black (negative) lead at the emitter terminal as shown in Fig. 4.6. V_C is the voltage from collector to ground and is measured as shown in the same figure. In this case the two readings are identical, but in the networks to follow the two can be quite different. Clearly understanding the difference between the two measurements can prove to be quite important in the troubleshooting of transistor networks.

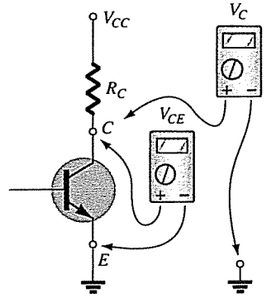


FIG. 4.6
Measuring V_{CE} and V_C.

EXAMPLE 4.1 Determine the following for the fixed-bias configuration of Fig. 4.7.

a. I_{B_Q} and I_{C_Q}.
b. V_{CE_Q}.
c. V_B and V_C.
d. V_{BC}.

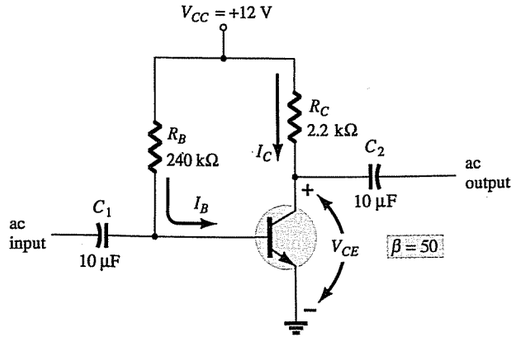


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Solution:

a. Eq. (4.4): $$I_{B_Q} = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12\text{ V} - 0.7\text{ V}}{240\text{ k}\Omega} = \mathbf{47.08\ \mu A}$$

Eq. (4.5): $$I_{C_Q} = \beta I_{B_Q} = (50)(47.08\ \mu\text{A}) = \mathbf{2.35\ mA}$$



Multisim

FIG. 4.7
DC fixed-bias circuit for Example 4.1.

b. Eq. (4.6): $V_{CE_Q} = V_{CC} - I_C R_C$
$= 12\text{ V} - (2.35\text{ mA})(2.2\text{ k}\Omega)$
$= \mathbf{6.83\text{ V}}$

c. $V_B = V_{BE} = \mathbf{0.7\text{ V}}$
$V_C = V_{CE} = \mathbf{6.83\text{ V}}$

d. Using double-subscript notation yields
$V_{BC} = V_B - V_C = 0.7\text{ V} - 6.83\text{ V}$
$= \mathbf{-6.13\text{ V}}$
with the negative sign revealing that the junction is reversed-biased, as it should be for linear amplification.

Transistor Saturation

The term *saturation* is applied to any system where levels have reached their maximum values. A saturated sponge is one that cannot hold another drop of liquid. For a transistor operating in the saturation region, the current is a maximum value *for the particular design.* Change the design and the corresponding saturation level may rise or drop. Of course, the highest saturation level is defined by the maximum collector current as provided by the specification sheet.

Saturation conditions are normally avoided because the base–collector junction is no longer reverse-biased and the output amplified signal will be distorted. An operating point in the saturation region is depicted in Fig. 4.8a. Note that it is in a region where the characteristic curves join and the collector-to-emitter voltage is at or below $V_{CE_{sat}}$. In addition, the collector current is relatively high on the characteristics.

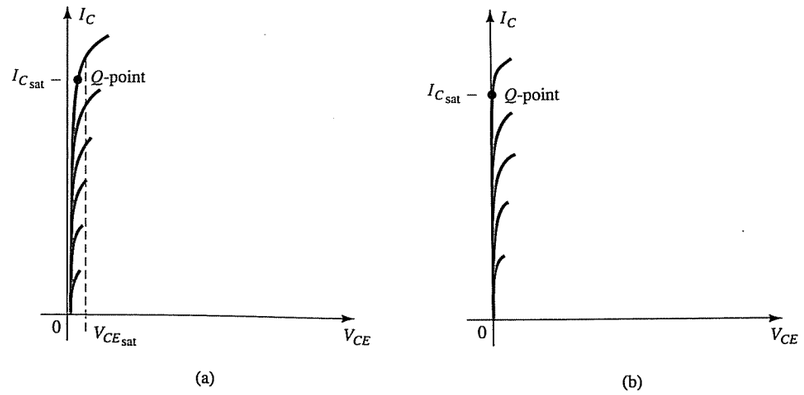


FIG. 4.8
Saturation regions: (a) actual; (b) approximate.

If we approximate the curves of Fig. 4.8a by those appearing in Fig. 4.8b, a quick, direct method for determining the saturation level becomes apparent. In Fig. 4.8b, the current is relatively high and the voltage V_{CE} is assumed to be 0 V. Applying Ohm's law, we can determine the resistance between collector and emitter terminals as follows:

$$R_{CE} = \frac{V_{CE}}{I_C} = \frac{0\text{ V}}{I_{C_{sat}}} = 0\ \Omega$$

Applying the results to the network schematic results in the configuration of Fig. 4.9.

For the future, therefore, if there were an immediate need to know the approximate maximum collector current (saturation level) for a particular design, simply insert a short-circuit equivalent between collector and emitter of the transistor and calculate the resulting collector current. In short, set $V_{CE} = 0$ V. For the fixed-bias configuration of Fig. 4.10, the short circuit has been applied, causing the voltage across R_C to be the applied voltage V_{CC}. The resulting saturation current for the fixed-bias configuration is

$$\boxed{I_{C_{sat}} = \frac{V_{CC}}{R_C}} \qquad \textbf{(4.11)}$$

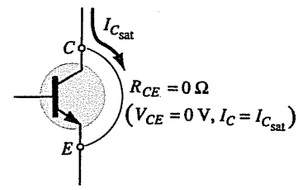


FIG. 4.9
Determining $I_{C_{sat}}$.

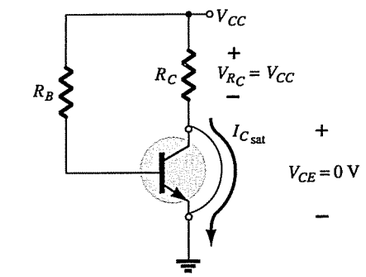


FIG. 4.10
Determining $I_{C_{sat}}$ for the fixed-bias configuration.

Once $I_{C_{sat}}$ is known, we have some idea of the maximum possible collector current for the chosen design and the level to stay below if we expect linear amplification.

EXAMPLE 4.2 Determine the saturation level for the network of Fig. 4.7.

Solution:

$$I_{C_{sat}} = \frac{V_{CC}}{R_C} = \frac{12\text{ V}}{2.2\text{ k}\Omega} = \mathbf{5.45\text{ mA}}$$

The design of Example 4.1 resulted in $I_{C_Q} = 2.35$ mA, which is far from the saturation level and about one-half the maximum value for the design.

Load-Line Analysis

The analysis thus far has been performed using a level of β corresponding to the resulting Q-point. We will now investigate how the network parameters define the possible range of Q-points and how the actual Q-point is determined. The network of Fig. 4.11a establishes an output equation that relates the variables I_C and V_{CE} in the following manner:

$$\boxed{V_{CE} = V_{CC} - I_C R_C} \qquad \textbf{(4.12)}$$

The output characteristics of the transistor also relate the same two variables I_C and V_{CE} as shown in Fig. 4.11b.

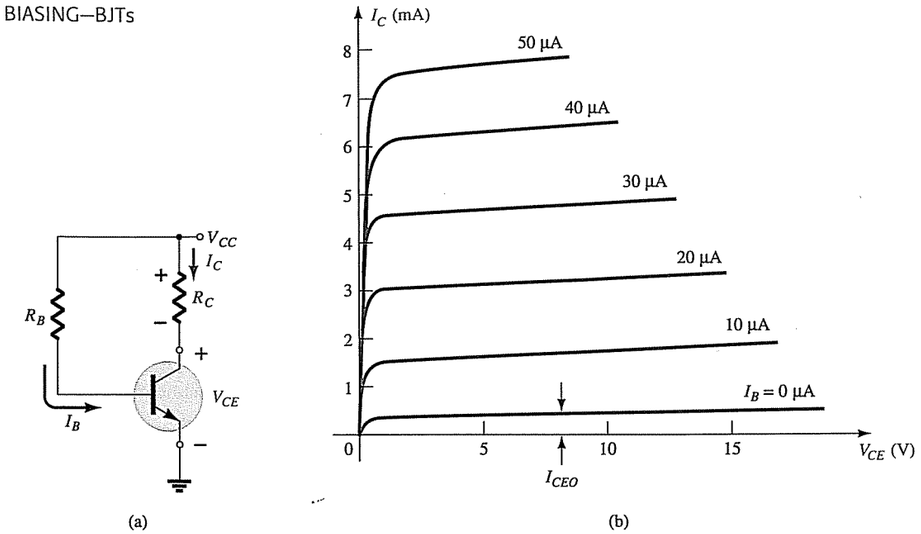


FIG. 4.11
Load-line analysis: (a) the network; (b) the device characteristics.

In essence, therefore, we have a network equation and a set of characteristics that employ the same variables. The common solution of the two occurs where the constraints established by each are satisfied simultaneously. In other words, this is similar to finding the solution of two simultaneous equations: one established by the network and the other by the device characteristics.

The device characteristics of I_C versus V_{CE} are provided in Fig. 4.11b. We must now superimpose the straight line defined by Eq. (4.12) on the characteristics. The most direct method of plotting Eq. (4.12) on the output characteristics is to use the fact that a straight line is defined by two points. If we *choose* I_C to be 0 mA, we are specifying the horizontal axis as the line on which one point is located. By substituting $I_C = 0$ mA into Eq. (4.12), we find that

$$V_{CE} = V_{CC} - (0)R_C$$

and

$$\boxed{V_{CE} = V_{CC}|_{I_C=0\,\text{mA}}} \tag{4.13}$$

defining one point for the straight line as shown in Fig. 4.12.

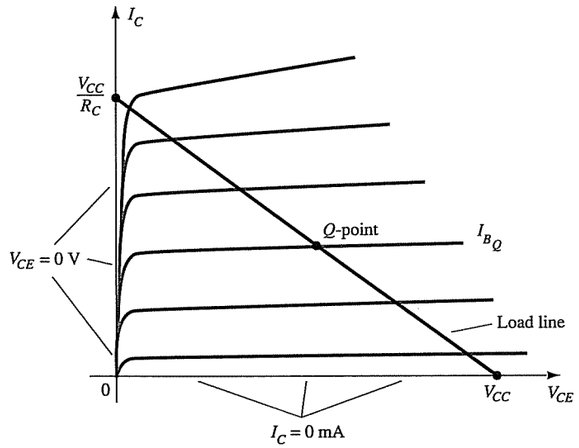


FIG. 4.12
Fixed-bias load line.

If we now *choose* V_{CE} to be 0 V, which establishes the vertical axis as the line on which the second point will be defined, we find that I_C is determined by the following equation:

$$0 = V_{CC} - I_C R_C$$

and

$$\boxed{I_C = \frac{V_{CC}}{R_C}\bigg|_{V_{CE}=0\,\text{V}}} \tag{4.14}$$

as appearing on Fig. 4.12.

By joining the two points defined by Eqs. (4.13) and (4.14), we can draw the straight line established by Eq. (4.12). The resulting line on the graph of Fig. 4.12 is called the *load line* since it is defined by the load resistor R_C. By solving for the resulting level of I_B, we can establish the actual Q-point as shown in Fig. 4.12.

If the level of I_B is changed by varying the value of R_B, the Q-point moves up or down the load line as shown in Fig. 4.13. If V_{CC} is held fixed and R_C changed, the load line will shift as shown in Fig. 4.14. If I_B is held fixed, the Q-point will move as shown in the same figure. If R_C is fixed and V_{CC} varied, the load line shifts as shown in Fig. 4.15.

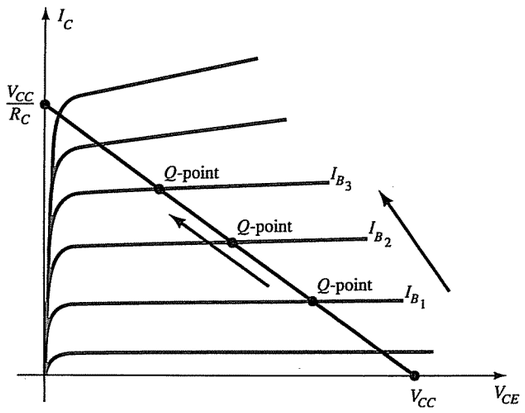


FIG. 4.13
Movement of the Q-point with increasing level of I_B.

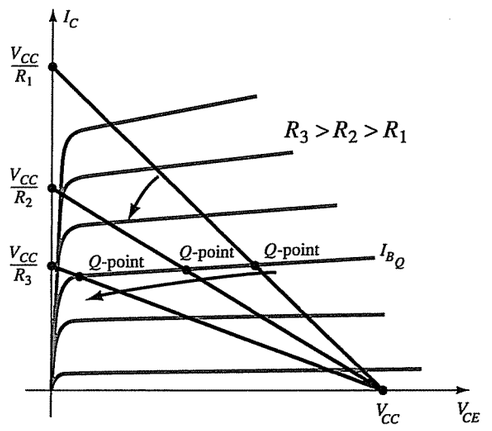


FIG. 4.14
Effect of an increasing level of R_C on the load line and the Q-point.

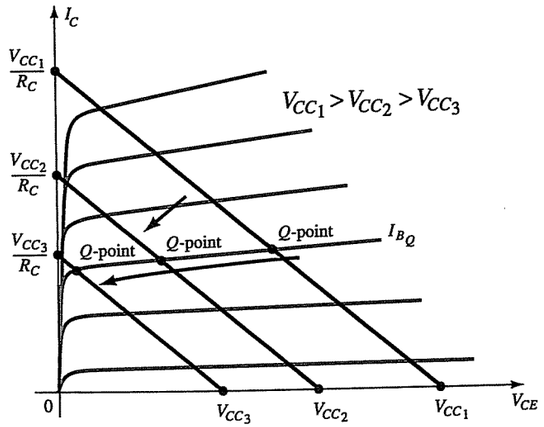


FIG. 4.15
Effect of lower values of V_{CC} on the load line and the Q-point.

EXAMPLE 4.3 Given the load line of Fig. 4.16 and the defined Q-point, determine the required values of V_{CC}, R_C, and R_B for a fixed-bias configuration.

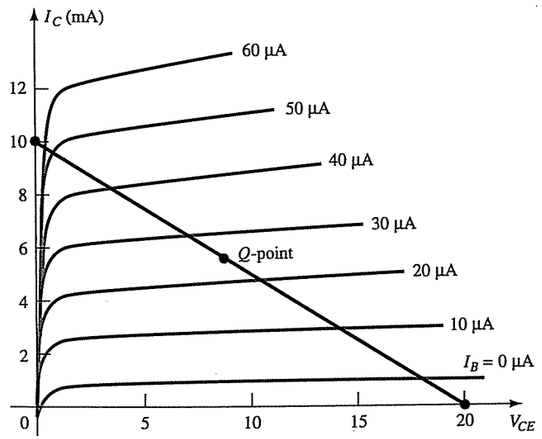


FIG. 4.16
Example 4.3.

Solution: From Fig. 4.16,

$$V_{CE} = V_{CC} = \mathbf{20\ V} \text{ at } I_C = 0\text{ mA}$$

$$I_C = \frac{V_{CC}}{R_C} \text{ at } V_{CE} = 0\text{ V}$$

and

$$R_C = \frac{V_{CC}}{I_C} = \frac{20\text{ V}}{10\text{ mA}} = \mathbf{2\ k\Omega}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

and

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{20\text{ V} - 0.7\text{ V}}{25\ \mu\text{A}} = \mathbf{772\ k\Omega}$$

The dc bias network of Fig. 4.17 contains an emitter resistor to improve the stability level over that of the fixed-bias configuration. The improved stability will be demonstrated through a numerical example later in the section. The analysis will be performed by first examining the base–emitter loop and then using the results to investigate the collector–emitter loop.

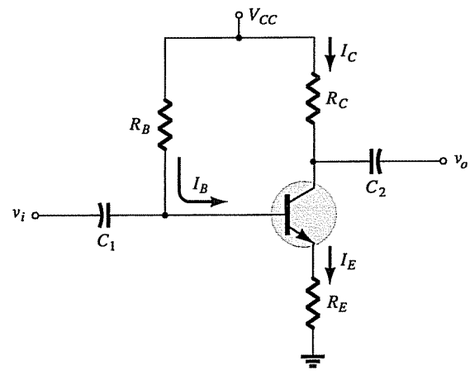


FIG. 4.17
BJT bias circuit with emitter resistor.

Base–Emitter Loop

The base–emitter loop of the network of Fig. 4.17 can be redrawn as shown in Fig. 4.18. Writing Kirchhoff's voltage law around the indicated loop in the clockwise direction results in the following equation:

$$+V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0 \qquad \textbf{(4.15)}$$

Recall from Chapter 3 that

$$I_E = (\beta + 1)I_B \qquad \textbf{(4.16)}$$

Substituting for I_E in Eq. (4.15) results in

$$V_{CC} - I_B R_B - V_{BE} - (\beta + I)I_B R_E = 0$$

Grouping terms then provides the following:

$$-I_B(R_B + (\beta + 1)R_E) + V_{CC} - V_{BE} = 0$$

Multiplying through by (-1), we have

$$I_B(R_B + (\beta + 1)R_E) - V_{CC} + V_{BE} = 0$$

with

$$I_B(R_B + (\beta + 1)R_E) = V_{CC} - V_{BE}$$

and solving for I_B gives

$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}} \qquad \textbf{(4.17)}$$

Note that the only difference between this equation for I_B and that obtained for the fixed-bias configuration is the term $(\beta + 1)R_E$.

There is an interesting result that can be derived from Eq. (4.17) if the equation is used to sketch a series network that would result in the same equation. Such is the case for the network of Fig. 4.19. Solving for the current I_B results in the same equation as obtained above. Note that aside from the base-to-emitter voltage V_{BE}, the resistor R_E is *reflected* back to the input base circuit by a factor $(\beta + 1)$. In other words, the emitter resistor, which is part of the collector–emitter loop, "appears as" $(\beta + 1)R_E$ in the base–emitter loop. Since β is typically 50 or more, the emitter resistor appears to be a great deal larger in the base circuit. In general, therefore, for the configuration of Fig. 4.20,

$$\boxed{R_i = (\beta + 1)R_E} \qquad \textbf{(4.18)}$$

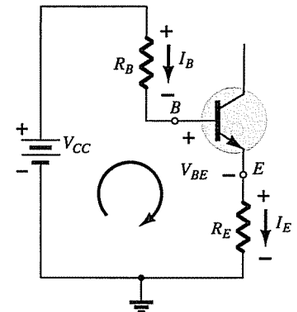


FIG. 4.18
Base–emitter loop.

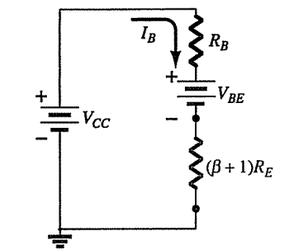


FIG. 4.19
Network derived from Eq. (4.17).

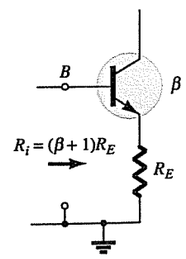


FIG. 4.20
Reflected impedance level of R_E.

Equation (4.18) will prove useful in the analysis to follow. In fact, it provides a fairly easy way to remember Eq. (4.17). Using Ohm's law, we know that the current through a system is the voltage divided by the resistance of the circuit. For the base–emitter circuit the net voltage is $V_{CC} - V_{BE}$. The resistance levels are R_B plus R_E reflected by $(\beta + 1)$. The result is Eq. (4.17).

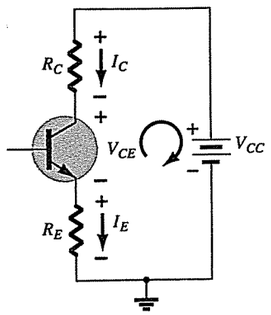


FIG. 4.21
Collector–emitter loop.

Collector–Emitter Loop

The collector–emitter loop is redrawn in Fig. 4.21. Writing Kirchhoff's voltage law for the indicated loop in the clockwise direction results in

$$+I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

Substituting $I_E \cong I_C$ and grouping terms gives

$$V_{CE} - V_{CC} + I_C(R_C + R_E) = 0$$

and

$$\boxed{V_{CE} = V_{CC} - I_C(R_C + R_E)} \qquad \textbf{(4.19)}$$

The single-subscript voltage V_E is the voltage from emitter to ground and is determined by

$$\boxed{V_E = I_E R_E} \qquad \textbf{(4.20)}$$

whereas the voltage from collector to ground can be determined from

$$V_{CE} = V_C - V_E$$

and

$$\boxed{V_C = V_{CE} + V_E} \qquad \textbf{(4.21)}$$

or

$$\boxed{V_C = V_{CC} - I_C R_C} \qquad \textbf{(4.22)}$$

The voltage at the base with respect to ground can be determined from

$$\boxed{V_B = V_{CC} - I_B R_B} \qquad \textbf{(4.23)}$$

or

$$\boxed{V_B = V_{BE} + V_E} \qquad \textbf{(4.24)}$$

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EXAMPLE 4.4 For the emitter bias network of Fig. 4.22, determine:

a. I_B.
b. I_C.
c. V_{CE}.
d. V_C.
e. V_E.
f. V_B.
g. V_{BC}.

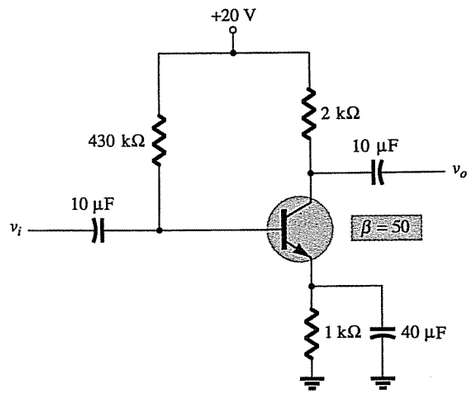


FIG. 4.22
Emitter-stabilized bias circuit for Example 4.4.

Solution:

a. Eq. (4.17): $$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{20\text{ V} - 0.7\text{ V}}{430\text{ k}\Omega + (51)(1\text{ k}\Omega)}$$
$$= \frac{19.3\text{ V}}{481\text{ k}\Omega} = \mathbf{40.1\ \mu A}$$

b. $I_C = \beta I_B$
$= (50)(40.1\ \mu\text{A})$
$\cong \mathbf{2.01\text{ mA}}$

c. Eq. (4.19): $V_{CE} = V_{CC} - I_C(R_C + R_E)$
$= 20\text{ V} - (2.01\text{ mA})(2\text{ k}\Omega + 1\text{ k}\Omega) = 20\text{ V} - 6.03\text{ V}$
$= \mathbf{13.97\text{ V}}$

d. $V_C = V_{CC} - I_C R_C$
$= 20\text{ V} - (2.01\text{ mA})(2\text{ k}\Omega) = 20\text{ V} - 4.02\text{ V}$
$= \mathbf{15.98\text{ V}}$

e. $V_E = V_C - V_{CE}$
$= 15.98\text{ V} - 13.97\text{ V}$
$= \mathbf{2.01\text{ V}}$

or $V_E = I_E R_E \cong I_C R_E$
$= (2.01\text{ mA})(1\text{ k}\Omega)$
$= \mathbf{2.01\text{ V}}$

f. $V_B = V_{BE} + V_E$
$= 0.7\text{ V} + 2.01\text{ V}$
$= \mathbf{2.71\text{ V}}$

g. $V_{BC} = V_B - V_C$
$= 2.71\text{ V} - 15.98\text{ V}$
$= \mathbf{-13.27\text{ V}}$ (reverse-biased as required)

Improved Bias Stability

The addition of the emitter resistor to the dc bias of the BJT provides improved stability, that is, the dc bias currents and voltages remain closer to where they were set by the circuit when outside conditions, such as temperature and transistor beta, change. Although a mathematical analysis is provided in Section 4.12, some comparison of the improvement can be obtained as demonstrated by Example 4.5.

EXAMPLE 4.5 Prepare a table and compare the bias voltage and currents of the circuits of Fig. 4.7 and Fig. 4.22 for the given value of $\beta = 50$ and for a new value of $\beta = 100$. Compare the changes in I_C and V_{CE} for the same increase in β.

Solution: Using the results calculated in Example 4.1 and then repeating for a value of $\beta = 100$ yields the following:

β	I_B (μA)	I_C (mA)	V_{CE} (V)
50	47.08	2.35	6.83
100	47.08	4.71	1.64

The BJT collector current is seen to change by 100% due to the 100% change in the value of β. The value of I_B is the same, and V_{CE} decreased by 76%.

Using the results calculated in Example 4.4 and then repeating for a value of $\beta = 100$, we have the following:

β	I_B (μA)	I_C (mA)	V_{CE} (V)
50	40.1	2.01	13.97
100	36.3	3.63	9.11

Now the BJT collector current increases by about 81% due to the 100% increase in β. Notice that I_B decreased, helping maintain the value of I_C—or at least reducing the overall change in I_C due to the change in β. The change in V_{CE} has dropped to about 35%. The network of Fig. 4.22 is therefore more stable than that of Fig. 4.7 for the same change in β.

Saturation Level

The collector saturation level or maximum collector current for an emitter-bias design can be determined using the same approach applied to the fixed-bias configuration: Apply a short circuit between the collector–emitter terminals as shown in Fig. 4.23 and calculate the resulting collector current. For Fig. 4.23

$$I_{C_{sat}} = \frac{V_{CC}}{R_C + R_E} \tag{4.25}$$

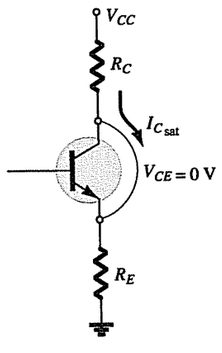


FIG. 4.23
Determining $I_{C_{sat}}$ for the emitter-stabilized bias circuit.

The addition of the emitter resistor reduces the collector saturation level below that obtained with a fixed-bias configuration using the same collector resistor.

EXAMPLE 4.6 Determine the saturation current for the network of Example 4.4.

Solution:

$$I_{C_{sat}} = \frac{V_{CC}}{R_C + R_E} = \frac{20\text{ V}}{2\text{ k}\Omega + 1\text{ k}\Omega} = \frac{20\text{ V}}{3\text{ k}\Omega} = \mathbf{6.67\text{ mA}}$$

which is about three times the level of I_{C_Q} for Example 4.4.

Load-Line Analysis

The load-line analysis of the emitter-bias network is only slightly different from that encountered for the fixed-bias configuration. The level of I_B as determined by Eq. (4.17) defines the level of I_B on the characteristics of Fig. 4.24 (denoted I_{B_Q}).

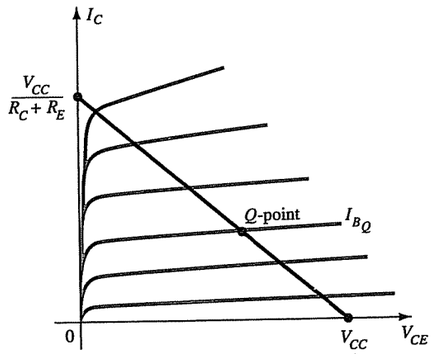


FIG. 4.24
Load line for the emitter-bias configuration.

The collector–emitter loop equation that defines the load line is

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

Choosing $I_C = 0$ mA gives

$$\boxed{V_{CE} = V_{CC}|_{I_C = 0\text{ mA}}} \tag{4.26}$$

as obtained for the fixed-bias configuration. Choosing $V_{CE} = 0$ V gives

$$\boxed{I_C = \frac{V_{CC}}{R_C + R_E}\bigg|_{V_{CE} = 0\text{ V}}} \tag{4.27}$$

as shown in Fig. 4.24. Different levels of I_{B_Q} will, of course, move the Q-point up or down the load line.

4.5 VOLTAGE-DIVIDER BIAS

In the previous bias configurations the bias current I_{C_Q} and voltage V_{CE_Q} were a function of the current gain β of the transistor. However, since β is temperature sensitive, especially for silicon transistors, and the actual value of beta is usually not well defined, it would be desirable to develop a bias circuit that is less dependent on, or in fact is independent of, the transistor beta. The voltage-divider bias configuration of Fig. 4.25 is such a network. If analyzed on an exact basis, the sensitivity to changes in beta is quite small. If the circuit parameters are properly chosen, the resulting levels of I_{C_Q} and V_{CE_Q} can be almost totally independent of beta. Recall from previous discussions that a Q-point is defined by a fixed level of I_{C_Q} and V_{CE_Q} as shown in Fig. 4.26. The level of I_{B_Q} will change with the change in beta, but the operating point on the characteristics defined by I_{C_Q} and V_{CE_Q} can remain fixed if the proper circuit parameters are employed.

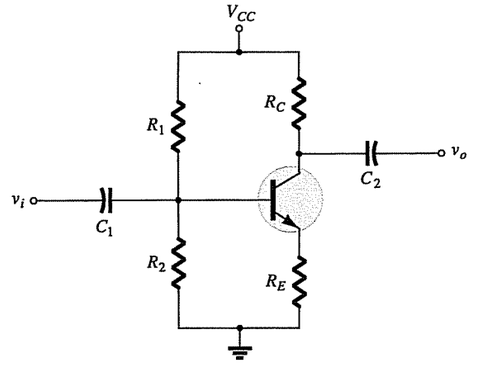


FIG. 4.25
Voltage-divider bias configuration.

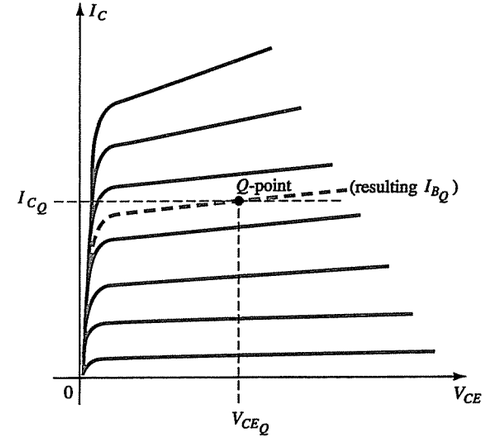


FIG. 4.26
Defining the Q-point for the voltage-divider bias configuration.

As noted above, there are two methods that can be applied to analyze the voltage-divider configuration. The reason for the choice of names for this configuration will become obvious in the analysis to follow. The first to be demonstrated is the *exact method*, which can be applied to *any* voltage-divider configuration. The second is referred to as the *approximate method* and can be applied only if specific conditions are satisfied. The approximate approach permits a more direct analysis with a savings in time and energy. It is also particularly helpful in the design mode to be described in a later section. All in all, the approximate approach can be applied to the majority of situations and therefore should be examined with the same interest as the exact method.

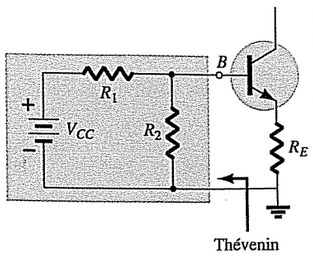


FIG. 4.27
Redrawing the input side of the network of Fig. 4.25.

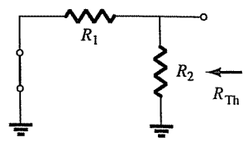


FIG. 4.28
Determining R_{Th}.

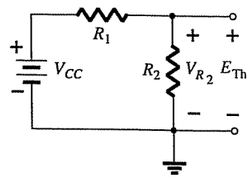


FIG. 4.29
Determining E_{Th}.

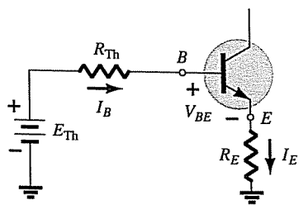


FIG. 4.30
Inserting the Thévenin equivalent circuit.

Exact Analysis

The input side of the network of Fig. 4.25 can be redrawn as shown in Fig. 4.27 for the dc analysis. The Thévenin equivalent network for the network to the left of the base terminal can then be found in the following manner:

R_{Th} The voltage source is replaced by a short-circuit equivalent as shown in Fig. 4.28:

$$R_{Th} = R_1 \| R_2 \tag{4.28}$$

E_{Th} The voltage source V_{CC} is returned to the network and the open-circuit Thévenin voltage of Fig. 4.29 determined as follows:

Applying the voltage-divider rule gives

$$E_{Th} = V_{R_2} = \frac{R_2 V_{CC}}{R_1 + R_2} \tag{4.29}$$

The Thévenin network is then redrawn as shown in Fig. 4.30, and I_{BQ} can be determined by first applying Kirchhoff's voltage law in the clockwise direction for the loop indicated:

$$E_{Th} - I_B R_{Th} - V_{BE} - I_E R_E = 0$$

Substituting $I_E = (\beta + 1)I_B$ and solving for I_B yields

$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E} \tag{4.30}$$

Although Eq. (4.30) initially appears to be different from those developed earlier, note that the numerator is again a difference of two voltage levels and the denominator is the base resistance plus the emitter resistor reflected by $(\beta + 1)$—certainly very similar to Eq. (4.17).

Once I_B is known, the remaining quantities of the network can be found in the same manner as developed for the emitter-bias configuration. That is,

$$V_{CE} = V_{CC} - I_C(R_C + R_E) \tag{4.31}$$

which is exactly the same as Eq. (4.19). The remaining equations for V_E, V_C, and V_B are also the same as obtained for the emitter-bias configuration.

EXAMPLE 4.7 Determine the dc bias voltage V_{CE} and the current I_C for the voltage-divider configuration of Fig. 4.31.

Solution:

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Eq. (4.28): $$R_{Th} = R_1 \| R_2 = \frac{(39\,\text{k}\Omega)(3.9\,\text{k}\Omega)}{39\,\text{k}\Omega + 3.9\,\text{k}\Omega} = 3.55\,\text{k}\Omega$$

Eq. (4.29): $$E_{Th} = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{(3.9\,\text{k}\Omega)(22\,\text{V})}{39\,\text{k}\Omega + 3.9\,\text{k}\Omega} = 2\,\text{V}$$

Eq. (4.30): $$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E} = \frac{2\,\text{V} - 0.7\,\text{V}}{3.55\,\text{k}\Omega + (141)(1.5\,\text{k}\Omega)} = \frac{1.3\,\text{V}}{3.55\,\text{k}\Omega + 211.5\,\text{k}\Omega}$$
$$= 6.05\,\mu\text{A}$$
$$I_C = \beta I_B = (140)(6.05\,\mu\text{A}) = \mathbf{0.85\,mA}$$

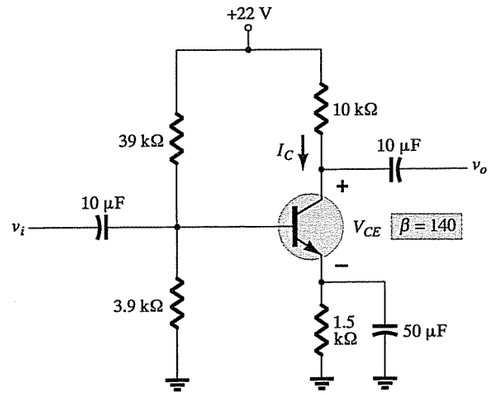


FIG. 4.31
Beta-stabilized circuit for Example 4.7.

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Eq. (4.31): $$V_{CE} = V_{CC} - I_C(R_C + R_E) = 22\,\text{V} - (0.85\,\text{mA})(10\,\text{k}\Omega + 1.5\,\text{k}\Omega) = 22\,\text{V} - 9.78\,\text{V} = \mathbf{12.22\,V}$$

Approximate Analysis

The input section of the voltage-divider configuration can be represented by the network of Fig. 4.32. The resistance R_i is the equivalent resistance between base and ground for the transistor with an emitter resistor R_E. Recall from Section 4.4 [Eq. (4.18)] that the reflected resistance between base and emitter is defined by $R_i = (\beta + 1)R_E$. If R_i is much larger than the resistance R_2, the current I_B will be much smaller than I_2 (current always seeks the path of least resistance) and I_2 will be approximately equal to I_1. If we accept the approximation that I_B is essentially 0 A compared to I_1 or I_2, then $I_1 = I_2$, and R_1 and R_2 can be considered series elements. The voltage across R_2, which is actually the base voltage, can be determined using the voltage-divider rule (hence the name for the configuration). That is,

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2} \tag{4.32}$$

Since $R_i = (\beta + 1)R_E \cong \beta R_E$ the condition that will define whether the approximate approach can be applied is

$$\beta R_E \geq 10 R_2 \tag{4.33}$$

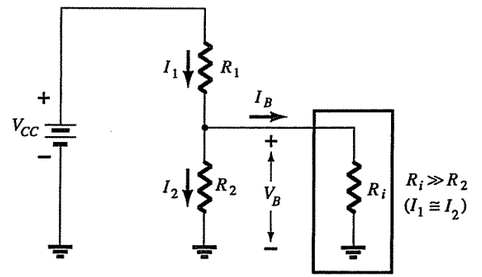


FIG. 4.32
Partial-bias circuit for calculating the approximate base voltage V_B.

In other words, if β times the value of R_E is at least 10 times the value of R_2, the approximate approach can be applied with a high degree of accuracy.

Once V_B is determined, the level of V_E can be calculated from

$$V_E = V_B - V_{BE} \tag{4.34}$$

and the emitter current can be determined from

$$I_E = \frac{V_E}{R_E} \tag{4.35}$$

and

$$I_{C_Q} \cong I_E \tag{4.36}$$

The collector-to-emitter voltage is determined by

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

but since $I_E \cong I_C$,

$$V_{CE_Q} = V_{CC} - I_C(R_C + R_E) \tag{4.37}$$

Note in the sequence of calculations from Eq. (4.33) through Eq. (4.37) that β does not appear and I_B was not calculated. The Q-point (as determined by I_{C_Q} and V_{CE_Q}) is therefore independent of the value of β.

EXAMPLE 4.8 Repeat the analysis of Fig. 4.31 using the approximate technique, and compare solutions for I_{C_Q} and V_{CE_Q}.

Solution: Testing:

$$\begin{aligned} \beta R_E &\geq 10R_2 \\ (140)(1.5\,\text{k}\Omega) &\geq 10(3.9\,\text{k}\Omega) \\ 210\,\text{k}\Omega &\geq 39\,\text{k}\Omega \ (\textit{satisfied}) \end{aligned}$$

$$\begin{aligned} \text{Eq. (4.32):} \quad V_B &= \frac{R_2 V_{CC}}{R_1 + R_2} \\ &= \frac{(3.9\,\text{k}\Omega)(22\,\text{V})}{39\,\text{k}\Omega + 3.9\,\text{k}\Omega} \\ &= 2\,\text{V} \end{aligned}$$

Note that the level of V_B is the same as E_{Th} determined in Example 4.7. Essentially, therefore, the primary difference between the exact and approximate techniques is the effect of R_{Th} in the exact analysis that separates E_{Th} and V_B.

$$\begin{aligned} \text{Eq. (4.34):} \quad V_E &= V_B - V_{BE} \\ &= 2\,\text{V} - 0.7\,\text{V} \\ &= 1.3\,\text{V} \end{aligned}$$

$$I_{CQ} \cong I_E = \frac{V_E}{R_E} = \frac{1.3\,\text{V}}{1.5\,\text{k}\Omega} = \mathbf{0.867\,mA}$$

compared to 0.85 mA with the exact analysis. Finally,

$$\begin{aligned} V_{CE_Q} &= V_{CC} - I_C(R_C + R_E) \\ &= 22\,\text{V} - (0.867\,\text{mA})(10\,\text{kV} + 1.5\,\text{k}\Omega) \\ &= 22\,\text{V} - 9.97\,\text{V} \\ &= \mathbf{12.03\,V} \end{aligned}$$

versus 12.22 V obtained in Example 4.7.

The results for I_{C_Q} and V_{CE_Q} are certainly close, and considering the actual variation in parameter values, one can certainly be considered as accurate as the other. The larger the level of R_i compared to R_2, the closer is the approximate to the exact solution. Example 4.10 will compare solutions at a level well below the condition established by Eq. (4.33).

EXAMPLE 4.9 Repeat the exact analysis of Example 4.7 if β is reduced to 70, and compare solutions for I_{C_Q} and V_{CE_Q}.

Solution: This example is not a comparison of exact versus approximate methods, but a testing of how much the Q-point will move if the level of β is cut in half. R_{Th} and E_{Th} are the same:

$$\begin{aligned} R_{\text{Th}} &= 3.55\,\text{k}\Omega, \qquad E_{\text{Th}} = 2\,\text{V} \\ I_B &= \frac{E_{\text{Th}} - V_{BE}}{R_{\text{Th}} + (\beta + 1)R_E} \\ &= \frac{2\,\text{V} - 0.7\,\text{V}}{3.55\,\text{k}\Omega + (71)(1.5\,\text{k}\Omega)} = \frac{1.3\,\text{V}}{3.55\,\text{k}\Omega + 106.5\,\text{k}\Omega} \\ &= 11.81\,\mu\text{A} \\ I_{C_Q} &= \beta I_B \\ &= (70)(11.81\,\mu\text{A}) \\ &= 0.83\,\text{mA} \\ V_{CE_Q} &= V_{CC} - I_C(R_C + R_E) \\ &= 22\,\text{V} - (0.83\,\text{mA})(10\,\text{k}\Omega + 1.5\,\text{k}\Omega) \\ &= \mathbf{12.46\,V} \end{aligned}$$

Tabulating the results, we have:

β	I_{C_Q} (mA)	V_{CE_Q} (V)
140	0.85	12.22
70	0.83	12.46

The results clearly show the relative insensitivity of the circuit to the change in β. Even though β is drastically cut in half, from 140 to 70, the levels of I_{C_Q} and V_{CE_Q} are essentially the same.



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EXAMPLE 4.10 Determine the levels of I_{C_Q} and V_{CE_Q} for the voltage-divider configuration of Fig. 4.33 using the exact and approximate techniques and compare solutions. In this case, the conditions of Eq. (4.33) *will not be satisfied* and the results will reveal the difference in solution if the criterion of Eq. (4.33) is ignored.

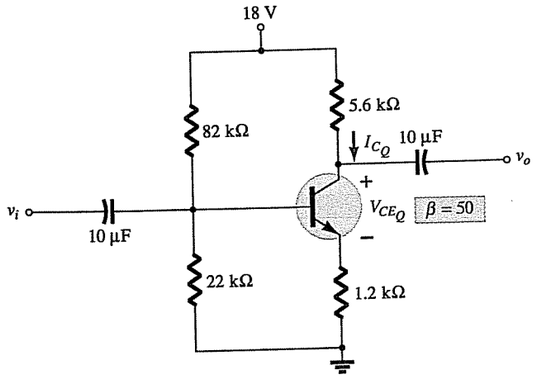
Solution: Exact Analysis:

$$\begin{aligned} \text{Eq. (4.33):} \quad \beta R_E &\geq 10R_2 \\ (50)(1.2\,\text{k}\Omega) &\geq 10(22\,\text{k}\Omega) \\ 60\,\text{k}\Omega &\ngeq 220\,\text{k}\Omega \ (\textit{not satisfied}) \end{aligned}$$

$$R_{\text{Th}} = R_1 \| R_2 = 82\,\text{k}\Omega \| 22\,\text{k}\Omega = 17.35\,\text{k}\Omega$$

$$E_{\text{Th}} = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{22\,\text{k}\Omega(18\,\text{V})}{82\,\text{k}\Omega + 22\,\text{k}\Omega} = 3.81\,\text{V}$$

$$I_B = \frac{E_{\text{Th}} - V_{BE}}{R_{\text{Th}} + (\beta + 1)R_E} = \frac{3.81\,\text{V} - 0.7\,\text{V}}{17.35\,\text{k}\Omega + (51)(1.2\,\text{k}\Omega)} = \frac{3.11\text{V}}{78.55\text{k}\Omega} = 39.6\mu\text{A}$$



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FIG. 4.33
Voltage-divider configuration for Example 4.10.

$$I_{C_Q} = \beta I_B = (50)(39.6\,\mu\text{A}) = \mathbf{1.98\ mA}$$
$$V_{CE_Q} = V_{CC} - I_C(R_C + R_E)$$
$$= 18\text{ V} - (1.98\text{ mA})(5.6\,\text{k}\Omega + 1.2\,\text{k}\Omega)$$
$$= \mathbf{4.54\ V}$$

Approximate Analysis:

$$V_B = E_{\text{Th}} = 3.81\text{ V}$$
$$V_E = V_B - V_{BE} = 3.81\text{ V} - 0.7\text{ V} = 3.11\text{ V}$$
$$I_{C_Q} \cong I_E = \frac{V_E}{R_E} = \frac{3.11\text{ V}}{1.2\,\text{k}\Omega} = \mathbf{2.59\ mA}$$
$$V_{CE_Q} = V_{CC} - I_C(R_C + R_E)$$
$$= 18\text{ V} - (2.59\text{ mA})(5.6\,\text{k}\Omega + 1.2\,\text{k}\Omega)$$
$$= \mathbf{3.88\ V}$$

Tabulating the results, we have:

	I_{C_Q} (mA)	V_{CE_Q} (V)
Exact	1.98	4.54
Approximate	2.59	3.88

The results reveal the difference between exact and approximate solutions. I_{C_Q} is about 30% greater with the approximate solution, whereas V_{CE_Q} is about 10% less. The results are notably different in magnitude, but even though βR_E is only about three times larger than R_2, the results are still relatively close to each other. For the future, however, our analysis will be dictated by Eq. (4.33) to ensure a close similarity between exact and approximate solutions.

Transistor Saturation

The output collector–emitter circuit for the voltage-divider configuration has the same appearance as the emitter-biased circuit analyzed in Section 4.4. The resulting equation for the saturation current (when V_{CE} is set to 0 V on the schematic) is therefore the same as obtained for the emitter-biased configuration. That is,

$$I_{C_{\text{sat}}} = I_{C_{\text{max}}} = \frac{V_{CC}}{R_C + R_E} \tag{4.38}$$

Load-Line Analysis

The similarities with the output circuit of the emitter-biased configuration result in the same intersections for the load line of the voltage-divider configuration. The load line will therefore have the same appearance as that of Fig. 4.24, with

$$I_C = \left.\frac{V_{CC}}{R_C + R_E}\right|_{V_{CE}=0\text{ V}} \tag{4.39}$$

and

$$V_{CE} = V_{CC}|_{I_C=0\text{ mA}} \tag{4.40}$$

The level of I_B is of course determined by a different equation for the voltage-divider bias and the emitter-bias configurations.

Mathcad

The power and usefulness of Mathcad can now be demonstrated for the network of Example 4.7. When using Mathcad, there is no need to worry about whether the exact or the approximate method should be applied to the voltage-divider bias network—Mathcad will always provide the most accurate results possible for the given data.

As shown in Fig. 4.34, all the parameters (variables) of the network are first entered, with the unit of measure. Although the listing will appear as shown in Fig. 4.34, in storage (internal

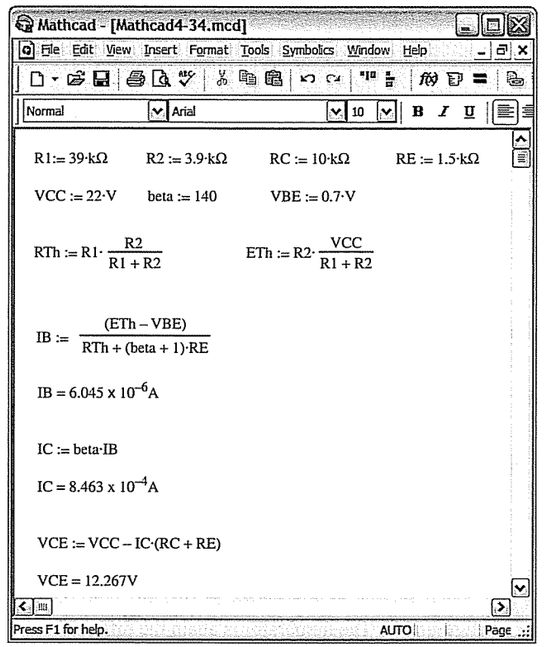


FIG. 4.34
Verifying the results of Example 4.7 using Mathcad 11.

hard disk or floppy disk) the parameters can easily be changed at any time with an immediate change in results. All the equations are then introduced in an order that permits using the results of one calculation to calculate the next quantity of interest. That is, the equations must be entered from left to right and down the display. In this example, R_{Th} and E_{Th} are first determined because they will be used to find **IB** on the next line.

Using Mathcad, the results obtained are an exact match for **IB** and **IC** and only slightly different for **VCE** because the level of **IC** carried a higher order of accuracy in the Mathcad solution. The advantage of having this sequence of calculations in storage is that it can be called up for any voltage-divider network, and the desired results can be obtained quickly and accurately simply by changing the magnitude of specific variables.

4.6 DC BIAS WITH VOLTAGE FEEDBACK

An improved level of stability can also be obtained by introducing a feedback path from collector to base as shown in Fig. 4.35. Although the Q-point is not totally independent of beta (even under approximate conditions), the sensitivity to changes in beta or temperature variations is normally less than encountered for the fixed-bias or emitter-biased configurations. The analysis will again be performed by first analyzing the base–emitter loop, with the results then applied to the collector–emitter loop.

Base–Emitter Loop

Figure 4.36 shows the base–emitter loop for the voltage feedback configuration. Writing Kirchhoff's voltage law around the indicated loop in the clockwise direction will result in

$$V_{CC} - I'_C R_C - I_B R_B - V_{BE} - I_E R_E = 0$$

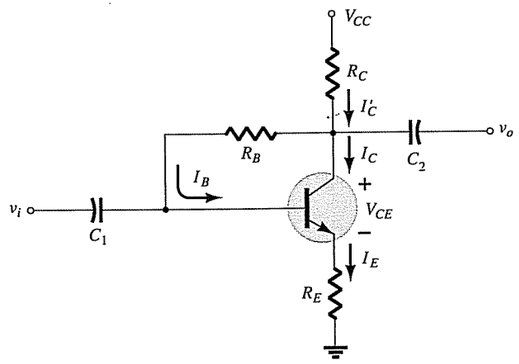


FIG. 4.35
DC bias circuit with voltage feedback.

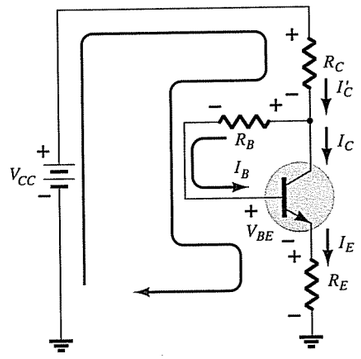


FIG. 4.36
Base–emitter loop for the network of Fig. 4.35.

It is important to note that the current through R_C is not I_C, but I'_C (where $I'_C = I_C + I_B$). However, the level of I_C and I'_C far exceeds the usual level of I_B, and the approximation $I'_C \cong I_C$ is normally employed. Substituting $I'_C \cong I_C = \beta I_B$ and $I_E \cong I_C$ results in

$$V_{CC} - \beta I_B R_C - I_B R_B - V_{BE} - \beta I_B R_E = 0$$

Gathering terms, we have

$$V_{CC} - V_{BE} - \beta I_B (R_C + R_E) - I_B R_B = 0$$

and solving for I_B yields

$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)}} \qquad (4.41)$$

The result is quite interesting in that the format is very similar to equations for I_B obtained for earlier configurations. The numerator is again the difference of available voltage levels, whereas the denominator is the base resistance plus the collector and emitter resistors reflected by beta. In general, therefore, the feedback path results in a reflection of the resistance R_C back to the input circuit, much like the reflection of R_E.

In general, the equation for I_B has the following format:

$$I_B = \frac{V'}{R_B + \beta R'}$$

with the absence of R' for the fixed-bias configuration, $R' = R_E$ for the emitter-bias setup (with $\beta + 1 \cong \beta$), and $R' = R_C + R_E$ for the collector-feedback arrangement. The voltage V' is the difference between two voltage levels.

Since $I_C = \beta I_B$,

$$I_{C_Q} = \frac{\beta V'}{R_B + \beta R'}$$

In general, the larger $\beta R'$ is compared to R_B, the lower is the sensitivity of I_{C_Q} to variations in beta. Obviously, if $\beta R' \gg R_B$ and $R_B + \beta R' \cong \beta R'$, then

$$I_{C_Q} = \frac{\beta V'}{R_B + \beta R'} \cong \frac{\beta V'}{\beta R'} = \frac{V'}{R'}$$

and I_{C_Q} is independent of the value of beta. Since R' is typically larger for the voltage-feedback configuration than for the emitter-bias configuration, the sensitivity to variations in beta is less. Of course, R' is 0 Ω for the fixed-bias configuration and is therefore quite sensitive to variations in beta.

Collector–Emitter Loop

The collector–emitter loop for the network of Fig. 4.35 is provided in Fig. 4.37. Applying Kirchhoff's voltage law around the indicated loop in the clockwise direction results in

$$I_E R_E + V_{CE} + I'_C R_C - V_{CC} = 0$$

Since $I'_C \cong I_C$ and $I_E \cong I_C$, we have

$$I_C(R_C + R_E) + V_{CE} - V_{CC} = 0$$

and

$$\boxed{V_{CE} = V_{CC} - I_C(R_C + R_E)} \qquad (4.42)$$

which is exactly as obtained for the emitter-bias and voltage-divider bias configurations.

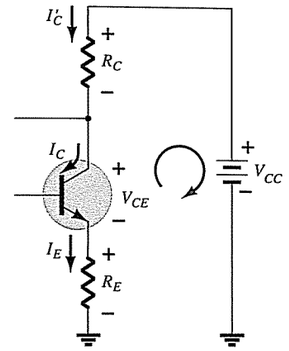


FIG. 4.37
Collector–emitter loop for the network of Fig. 4.35.

EXAMPLE 4.11 Determine the quiescent levels of I_{C_Q} and V_{CE_Q} for the network of Fig. 4.38.

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FIG. 4.38
Network for Example 4.11.

Solution:

$$\text{Eq. (4.41):} \quad I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)}$$

$$= \frac{10\,\text{V} - 0.7\,\text{V}}{250\,\text{k}\Omega + (90)(4.7\,\text{k}\Omega + 1.2\,\text{k}\Omega)}$$

$$= \frac{9.3\,\text{V}}{250\,\text{k}\Omega + 531\,\text{k}\Omega} = \frac{9.3\,\text{V}}{781\,\text{k}\Omega}$$

$$= 11.91\,\mu\text{A}$$

$$I_{C_Q} = \beta I_B = (90)(11.91\,\mu\text{A})$$

$$= \mathbf{1.07\,mA}$$

$$V_{CE_Q} = V_{CC} - I_C(R_C + R_E)$$

$$= 10\,\text{V} - (1.07\,\text{mA})(4.7\,\text{k}\Omega + 1.2\,\text{k}\Omega)$$

$$= 10\,\text{V} - 6.31\,\text{V}$$

$$= \mathbf{3.69\,V}$$

EXAMPLE 4.12 Repeat Example 4.11 using a beta of 135 (50% greater than in Example 4.11).

Solution: It is important to note in the solution for I_B in Example 4.11 that the second term in the denominator of the equation is larger than the first. Recall in a recent discussion that the larger this second term is compared to the first, the less is the sensitivity to changes in beta. In this example the level of beta is increased by 50%, which will increase the magnitude of this second term even more compared to the first. It is more important to note in these examples, however, that once the second term is relatively large compared to the first, the sensitivity to changes in beta is significantly less.

Solving for I_B gives

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)}$$
$$= \frac{10\text{ V} - 0.7\text{ V}}{250\,\text{k}\Omega + (135)(4.7\,\text{k}\Omega + 1.2\,\text{k}\Omega)}$$
$$= \frac{9.3\text{ V}}{250\,\text{k}\Omega + 796.5\,\text{k}\Omega} = \frac{9.3\text{ V}}{1046.5\,\text{k}\Omega}$$
$$= 8.89\,\mu\text{A}$$

and
$$I_{C_Q} = \beta I_B$$
$$= (135)(8.89\,\mu\text{A})$$
$$= \mathbf{1.2\text{ mA}}$$

and
$$V_{CE_Q} = V_{CC} - I_C(R_C + R_E)$$
$$= 10\text{ V} - (1.2\text{ mA})(4.7\,\text{k}\Omega + 1.2\,\text{k}\Omega)$$
$$= 10\text{ V} - 7.08\text{ V}$$
$$= \mathbf{2.92\text{ V}}$$

Even though the level of β increased 50%, the level of I_{C_Q} only increased 12.1%, whereas the level of V_{CE_Q} decreased about 20.9%. If the network were a fixed-bias design, a 50% increase in β would have resulted in a 50% increase in I_{C_Q} and a dramatic change in the location of the Q-point.



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EXAMPLE 4.13 Determine the dc level of I_B and V_C for the network of Fig. 4.39.

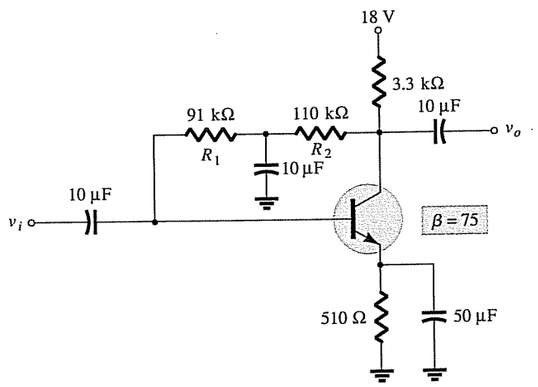


FIG. 4.39
Network for Example 4.13.

Solution: In this case, the base resistance for the dc analysis is composed of two resistors with a capacitor connected from their junction to ground. For the dc mode, the capacitor assumes the open-circuit equivalence, and $R_B = R_1 + R_2$.

Solving for I_B gives

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)}$$
$$= \frac{18\text{ V} - 0.7\text{ V}}{(91\,\text{k}\Omega + 110\,\text{k}\Omega) + (75)(3.3\,\text{k}\Omega + 0.51\,\text{k}\Omega)}$$
$$= \frac{17.3\text{ V}}{201\,\text{k}\Omega + 285.75\,\text{k}\Omega} = \frac{17.3\text{ V}}{486.75\,\text{k}\Omega}$$
$$= \mathbf{35.5\,\mu A}$$
$$I_C = \beta I_B$$
$$= (75)(35.5\,\mu\text{A})$$
$$= 2.66\text{ mA}$$
$$V_C = V_{CC} - I_C' R_C \cong V_{CC} - I_C R_C$$
$$= 18\text{ V} - (2.66\text{ mA})(3.3\,\text{k}\Omega)$$
$$= 18\text{ V} - 8.78\text{ V}$$
$$= \mathbf{9.22\text{ V}}$$

Saturation Conditions

Using the approximation $I_C' = I_C$, we find that the equation for the saturation current is the same as obtained for the voltage-divider and emitter-bias configurations. That is,

$$I_{C_{sat}} = I_{C_{max}} = \frac{V_{CC}}{R_C + R_E} \tag{4.43}$$

Load-Line Analysis

Continuing with the approximation $I_C' = I_C$ results in the same load line defined for the voltage-divider and emitter-biased configurations. The level of I_{B_Q} is defined by the chosen bias configuration.

4.7 MISCELLANEOUS BIAS CONFIGURATIONS

There are a number of BJT bias configurations that do not match the basic mold of those analyzed in the previous sections. In fact, there are variations in design that would require many more pages than is possible in a book of this type. However, the primary purpose here is to emphasize those characteristics of the device that permit a dc analysis of the configuration and to establish a general procedure toward the desired solution. For each configuration discussed thus far, the first step has been the derivation of an expression for the base current. Once the base current is known, the collector current and voltage levels of the output circuit can be determined quite directly. This is not to imply that all solutions will take this path, but it does suggest a possible route to follow if a new configuration is encountered.

The first example is simply one where the emitter resistor has been dropped from the voltage-feedback configuration of Fig. 4.35. The analysis is quite similar, but does require dropping R_E from the applied equation.

EXAMPLE 4.14 For the network of Fig. 4.40:

a. Determine I_{C_Q} and V_{CE_Q}.
b. Find V_B, V_C, V_E, and V_{BC}.

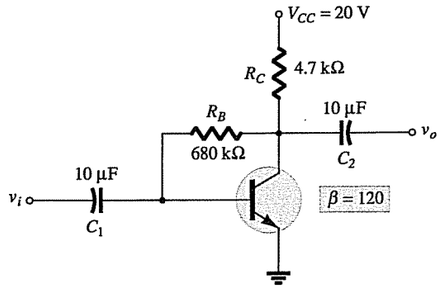


FIG. 4.40
Collector feedback with $R_E = 0\ \Omega$.

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Solution:

a. The absence of R_E reduces the reflection of resistive levels to simply that of R_C, and the equation for I_B reduces to

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta R_C}$$
$$= \frac{20\text{ V} - 0.7\text{ V}}{680\text{ k}\Omega + (120)(4.7\text{ k}\Omega)} = \frac{19.3\text{ V}}{1.244\text{ M}\Omega}$$
$$= 15.51\ \mu\text{A}$$
$$I_{C_Q} = \beta I_B = (120)(15.51\ \mu\text{A})$$
$$= \mathbf{1.86\text{ mA}}$$
$$V_{CE_Q} = V_{CC} - I_C R_C$$
$$= 20\text{ V} - (1.86\text{ mA})(4.7\text{ k}\Omega)$$
$$= \mathbf{11.26\text{ V}}$$

b.
$$V_B = V_{BE} = \mathbf{0.7\text{ V}}$$
$$V_C = V_{CE} = \mathbf{11.26\text{ V}}$$
$$V_E = \mathbf{0\text{ V}}$$
$$V_{BC} = V_B - V_C = 0.7\text{ V} - 11.26\text{ V}$$
$$= \mathbf{-10.56\text{ V}}$$

In the next example, the applied voltage is connected to the emitter leg and R_C is connected directly to ground. Initially, it appears somewhat unorthodox and quite different from those encountered thus far, but one application of Kirchhoff's voltage law to the base circuit will result in the desired base current.

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EXAMPLE 4.15 Determine V_C and V_B for the network of Fig. 4.41.

Solution: Applying Kirchhoff's voltage law in the clockwise direction for the base–emitter loop results in

$$-I_B R_B - V_{BE} + V_{EE} = 0$$

and
$$I_B = \frac{V_{EE} - V_{BE}}{R_B}$$

Substitution yields

$$I_B = \frac{9\text{ V} - 0.7\text{ V}}{100\text{ k}\Omega}$$
$$= \frac{8.3\text{ V}}{100\text{ k}\Omega}$$
$$= 83\ \mu\text{A}$$

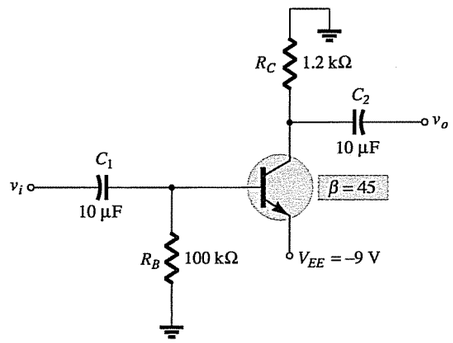


FIG. 4.41
Example 4.15.

$$I_C = \beta I_B$$
$$= (45)(83\ \mu\text{A})$$
$$= 3.735\text{ mA}$$
$$V_C = -I_C R_C$$
$$= -(3.735\text{ mA})(1.2\text{ k}\Omega)$$
$$= \mathbf{-4.48\text{ V}}$$
$$V_B = -I_B R_B$$
$$= -(83\ \mu\text{A})(100\text{ k}\Omega)$$
$$= \mathbf{-8.3\text{ V}}$$

The next example employs a network referred to as an *emitter–follower* configuration. When the same network is analyzed on an ac basis, we will find that the output and input signals are in phase (one following the other) and the output voltage is slightly less than the applied signal. For the dc analysis the collector is grounded and the applied voltage is in the emitter leg.

EXAMPLE 4.16 Determine V_{CE_Q} and I_E for the network of Fig. 4.42.

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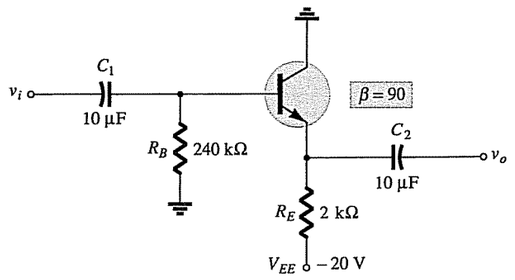


FIG. 4.42
Common-collector (emitter-follower) configuration.

Solution: Applying Kirchhoff's voltage law to the input circuit results in

$$-I_B R_B - V_{BE} - I_E R_E + V_{EE} = 0$$

but
$$I_E = (\beta + 1) I_B$$

and
$$V_{EE} - V_{BE} - (\beta + 1) I_B R_E - I_B R_B = 0$$

with
$$I_B = \frac{V_{EE} - V_{BE}}{R_B + (\beta + 1) R_E}$$

Substituting values yields

$$I_B = \frac{20\text{ V} - 0.7\text{ V}}{240\,\text{k}\Omega + (91)(2\,\text{k}\Omega)} = \frac{19.3\text{ V}}{240\,\text{k}\Omega + 182\,\text{k}\Omega} = \frac{19.3\text{ V}}{422\,\text{k}\Omega}$$
$$= 45.73\,\mu\text{A}$$
$$I_C = \beta I_B = (90)(45.73\,\mu\text{A}) = 4.12\,\text{mA}$$

Applying Kirchhoff's voltage law to the output circuit, we have

$$-V_{EE} + I_E R_E + V_{CE} = 0$$

but $$I_E = (\beta + 1)I_B$$

and $$V_{CE_Q} = V_{EE} - (\beta + 1)I_B R_E = 20\text{ V} - (91)(45.73\,\mu\text{A})(2\,\text{k}\Omega) = \mathbf{11.68\text{ V}}$$
$$I_E = \mathbf{4.16\text{ mA}}$$

All of the examples thus far have employed a common-emitter or common-collector configuration. In the next example we investigate the common-base configuration. In this situation the input circuit will be employed to determine I_E rather than I_B. The collector current is then available to perform an analysis of the output circuit.



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EXAMPLE 4.17 Determine the voltage V_{CB} and the current I_B for the common-base configuration of Fig. 4.43.

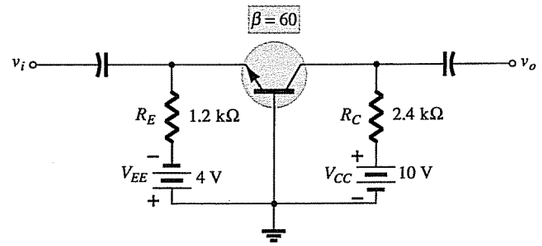


FIG. 4.43
Common-base configuration.

Solution: Applying Kirchhoff's voltage law to the input circuit yields

$$-V_{EE} + I_E R_E + V_{BE} = 0$$

and $$I_E = \frac{V_{EE} - V_{BE}}{R_E}$$

Substituting values, we obtain

$$I_E = \frac{4\text{ V} - 0.7\text{ V}}{1.2\,\text{k}\Omega} = 2.75\,\text{mA}$$

Applying Kirchhoff's voltage law to the output circuit gives

$$-V_{CB} + I_C R_C - V_{CC} = 0$$

and $$V_{CB} = V_{CC} - I_C R_C \text{ with } I_C \cong I_E = 10\text{ V} - (2.75\,\text{mA})(2.4\,\text{k}\Omega) = \mathbf{3.4\text{ V}}$$

$$I_B = \frac{I_C}{\beta} = \frac{2.75\,\text{mA}}{60} = \mathbf{45.8\,\mu\text{A}}$$

Example 4.18 employs a split supply and will require the application of Thévenin's theorem to determine the desired unknowns.

EXAMPLE 4.18 Determine V_C and V_B for the network of Fig. 4.44.

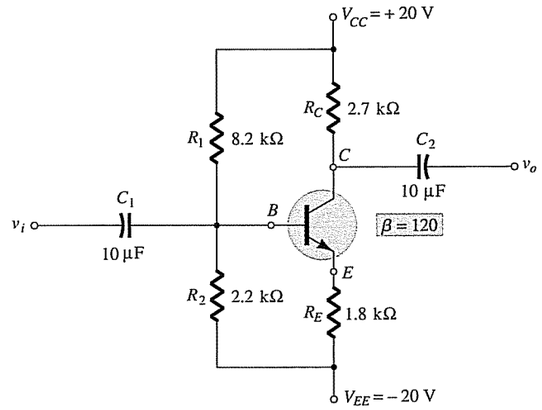


FIG. 4.44
Example 4.18.

Solution: The Thévenin resistance and voltage are determined for the network to the left of the base terminal as shown in Figs. 4.45 and 4.46.

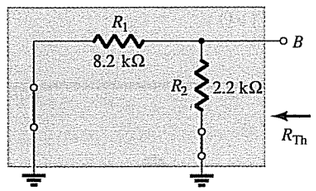


FIG. 4.45
Determining R_{Th}.

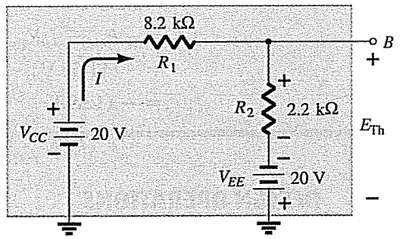


FIG. 4.46
Determining E_{Th}.

R_{Th}

$$R_{Th} = 8.2\,\text{k}\Omega \| 2.2\,\text{k}\Omega = 1.73\,\text{k}\Omega$$

E_{Th}

$$I = \frac{V_{CC} + V_{EE}}{R_1 + R_2} = \frac{20\text{ V} + 20\text{ V}}{8.2\,\text{k}\Omega + 2.2\,\text{k}\Omega} = \frac{40\text{ V}}{10.4\,\text{k}\Omega} = 3.85\,\text{mA}$$
$$E_{Th} = IR_2 - V_{EE} = (3.85\,\text{mA})(2.2\,\text{k}\Omega) - 20\text{ V} = -11.53\text{ V}$$

The network can then be redrawn as shown in Fig. 4.47, where the application of Kirchhoff's voltage law results in

$$-E_{\text{Th}} - I_B R_{\text{Th}} - V_{BE} - I_E R_E + V_{EE} = 0$$

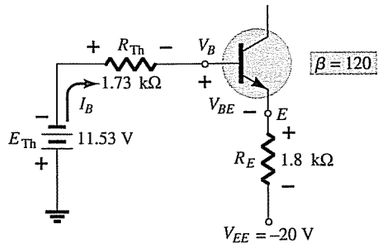


FIG. 4.47
Substituting the Thévenin equivalent circuit.

Substituting $I_E = (\beta + 1)I_B$ gives

$$V_{EE} - E_{\text{Th}} - V_{BE} - (\beta + 1)I_B R_E - I_B R_{\text{Th}} = 0$$

and

$$I_B = \frac{V_{EE} - E_{\text{Th}} - V_{BE}}{R_{\text{Th}} + (\beta + 1)R_E}$$
$$= \frac{20\,\text{V} - 11.53\,\text{V} - 0.7\,\text{V}}{1.73\,\text{k}\Omega + (121)(1.8\,\text{k}\Omega)}$$
$$= \frac{7.77\,\text{V}}{219.53\,\text{k}\Omega}$$
$$= 35.39\,\mu\text{A}$$
$$I_C = \beta I_B$$
$$= (120)(35.39\,\mu\text{A})$$
$$= 4.25\,\text{mA}$$
$$V_C = V_{CC} - I_C R_C$$
$$= 20\,\text{V} - (4.25\,\text{mA})(2.7\,\text{k}\Omega)$$
$$= \mathbf{8.53\,V}$$
$$V_B = -E_{\text{Th}} - I_B R_{\text{Th}}$$
$$= -(11.53\,\text{V}) - (35.39\,\mu\text{A})(1.73\,\text{k}\Omega)$$
$$= \mathbf{-11.59\,V}$$

4.8 DESIGN OPERATIONS

Discussions thus far have focused on the analysis of existing networks. All the elements are in place, and it is simply a matter of solving for the current and voltage levels of the configuration. The design process is one where a current and/or voltage may be specified and the elements required to establish the designated levels must be determined. This synthesis process requires a clear understanding of the characteristics of the device, the basic equations for the network, and a firm understanding of the basic laws of circuit analysis, such as Ohm's law, Kirchhoff's voltage law, and so on. In most situations the thinking process is challenged to a higher degree in the design process than in the analysis sequence. The path toward a solution is less defined and in fact may require a number of basic assumptions that do not have to be made when simply analyzing a network.

The design sequence is obviously sensitive to the components that are already specified and the elements to be determined. If the transistor and supplies are specified, the design process will simply determine the required resistors for a particular design. Once the theoretical values of the resistors are determined, the nearest standard commercial values are normally chosen and any variations due to not using the exact resistance values are accepted as part of the design. This is certainly a valid approximation considering the tolerances normally associated with resistive elements and the transistor parameters.

If resistive values are to be determined, one of the most powerful equations is simply Ohm's law in the following form:

$$R_{\text{unknown}} = \frac{V_R}{I_R} \tag{4.44}$$

In a particular design the voltage across a resistor can often be determined from specified levels. If additional specifications define the current level, Eq. (4.44) can then be used to calculate the required resistance level. The first few examples will demonstrate how particular elements can be determined from specified levels. A complete design procedure will then be introduced for two popular configurations.

EXAMPLE 4.19 Given the device characteristics of Fig. 4.48a, determine V_{CC}, R_B, and R_C for the fixed-bias configuration of Fig. 4.48b.

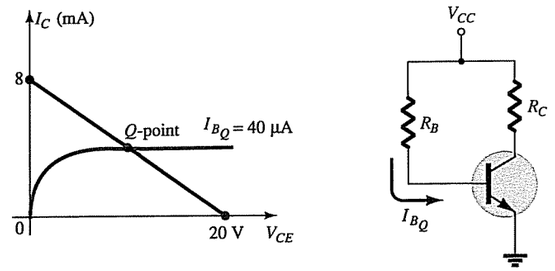


FIG. 4.48
Example 4.19.

Solution: From the load line

$$V_{CC} = \mathbf{20\,V}$$
$$I_C = \left.\frac{V_{CC}}{R_C}\right|_{V_{CE}=0\,\text{V}}$$

and

$$R_C = \frac{V_{CC}}{I_C} = \frac{20\,\text{V}}{8\,\text{mA}} = \mathbf{2.5\,k\Omega}$$
$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

with

$$R_B = \frac{V_{CC} - V_{BE}}{I_B}$$
$$= \frac{20\,\text{V} - 0.7\,\text{V}}{40\,\mu\text{A}} = \frac{19.3\,\text{V}}{40\,\mu\text{A}}$$
$$= \mathbf{482.5\,k\Omega}$$

Standard resistor values are

$$R_C = 2.4\,\text{k}\Omega$$
$$R_B = 470\,\text{k}\Omega$$

Using standard resistor values gives

$$I_B = 41.1\,\mu\text{A}$$

which is well within 5% of the value specified.

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EXAMPLE 4.20 Given that $I_{C_Q} = 2\,\text{mA}$ and $V_{CE_Q} = 10\,\text{V}$, determine R_1 and R_C for the network of Fig. 4.49.

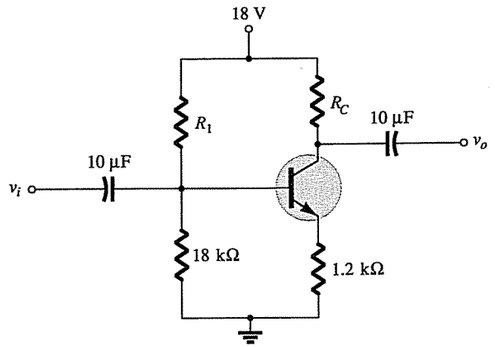


FIG. 4.49
Example 4.20.

Solution:

$$V_E = I_E R_E \cong I_C R_E$$
$$= (2\,\text{mA})(1.2\,\text{k}\Omega) = 2.4\,\text{V}$$
$$V_B = V_{BE} + V_E = 0.7\,\text{V} + 2.4\,\text{V} = 3.1\,\text{V}$$
$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2} = 3.1\,\text{V}$$

and
$$\frac{(18\,\text{k}\Omega)(18\,\text{V})}{R_1 + 18\,\text{k}\Omega} = 3.1\,\text{V}$$
$$324\,\text{k}\Omega = 3.1R_1 + 55.8\,\text{k}\Omega$$
$$3.1R_1 = 268.2\,\text{k}\Omega$$
$$R_1 = \frac{268.2\,\text{k}\Omega}{3.1} = \mathbf{86.52\,k\Omega}$$

Eq. (4.44):
$$R_C = \frac{V_{R_C}}{I_C} = \frac{V_{CC} - V_C}{I_C}$$

with
$$V_C = V_{CE} + V_E = 10\,\text{V} + 2.4\,\text{V} = 12.4\,\text{V}$$

and
$$R_C = \frac{18\,\text{V} - 12.4\,\text{V}}{2\,\text{mA}}$$
$$= \mathbf{2.8\,k\Omega}$$

The nearest standard commercial values to R_1 are 82 Ω and 91 kΩ. However, using the series combination of standard values of 82 kΩ and 4.7 kΩ = 86.7 kΩ would result in a value very close to the design level.

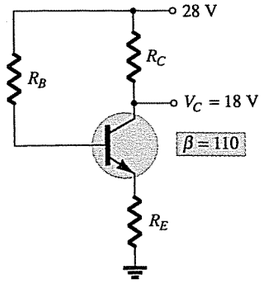


FIG. 4.50
Example 4.21.

EXAMPLE 4.21 The emitter-bias configuration of Fig. 4.50 has the following specifications: $I_{C_Q} = \frac{1}{2}I_{C_{sat}}$, $I_{C_{sat}} = 8\,\text{mA}$, $V_C = 18\,\text{V}$, and $\beta = 110$. Determine R_C, R_E, and R_B.

Solution:

$$I_{C_Q} = \tfrac{1}{2}I_{C_{sat}} = 4\,\text{mA}$$
$$R_C = \frac{V_{R_C}}{I_{C_Q}} = \frac{V_{CC} - V_C}{I_{C_Q}}$$
$$= \frac{28\,\text{V} - 18\,\text{V}}{4\,\text{mA}} = \mathbf{2.5\,k\Omega}$$

$$I_{C_{sat}} = \frac{V_{CC}}{R_C + R_E}$$

and
$$R_C + R_E = \frac{V_{CC}}{I_{C_{sat}}} = \frac{28\,\text{V}}{8\,\text{mA}} = 3.5\,\text{k}\Omega$$
$$R_E = 3.5\,\text{k}\Omega - R_C$$
$$= 3.5\,\text{k}\Omega - 2.5\,\text{k}\Omega$$
$$= \mathbf{1\,k\Omega}$$
$$I_{B_Q} = \frac{I_{C_Q}}{\beta} = \frac{4\,\text{mA}}{110} = 36.36\,\mu\text{A}$$
$$I_{B_Q} = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$$

and
$$R_B + (\beta + 1)R_E = \frac{V_{CC} - V_{BE}}{I_{B_Q}}$$

with
$$R_B = \frac{V_{CC} - V_{BE}}{I_{B_Q}} - (\beta + 1)R_E$$
$$= \frac{28\,\text{V} - 0.7\,\text{V}}{36.36\,\mu\text{A}} - (111)(1\,\text{k}\Omega)$$
$$= \frac{27.3\,\text{V}}{36.36\,\mu\text{A}} - 111\,\text{k}\Omega$$
$$= \mathbf{639.8\,k\Omega}$$

For standard values,

$$R_C = 2.4\,\text{k}\Omega$$
$$R_E = 1\,\text{k}\Omega$$
$$R_B = 620\,\text{k}\Omega$$

The discussion to follow will introduce one technique for designing an entire circuit to operate at a specified bias point. Often the manufacturer's specification (spec) sheets provide information on a suggested operating point (or operating region) for a particular transistor. In addition, other system components connected to the given amplifier stage may also define the current swing, voltage swing, value of common supply voltage, and so on, for the design.

In actual practice, many other factors may have to be considered that may affect the selection of the desired operating point. For the moment we concentrate on determining the component values to obtain a specified operating point. The discussion will be limited to the emitter-bias and voltage-divider bias configurations, although the same procedure can be applied to a variety of other transistor circuits.

Design of a Bias Circuit with an Emitter Feedback Resistor

Consider first the design of the dc bias components of an amplifier circuit having emitter-resistor bias stabilization as shown in Fig. 4.51. The supply voltage and operating point were selected from the manufacturer's information on the transistor used in the amplifier.

The selection of collector and emitter resistors cannot proceed directly from the information just specified. The equation that relates the voltages around the collector–emitter loop has two unknown quantities present—the resistors R_C and R_E. At this point some engineering judgment must be made, such as the level of the emitter voltage compared to the applied supply voltage. Recall that the need for including a resistor from emitter to ground was to provide a means of dc bias stabilization so that the change of collector current due to leakage currents in the transistor and the transistor beta would not cause a large shift in the operating point. The emitter resistor cannot be

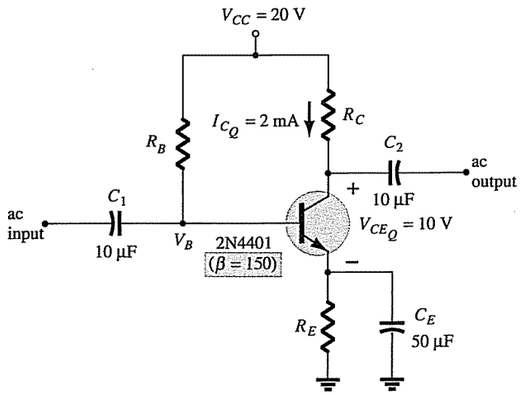


FIG. 4.51
Emitter-stabilized bias circuit for design consideration.

unreasonably large because the voltage across it limits the range of swing of the voltage from collector to emitter (to be noted when the ac response is discussed). The examples examined in this chapter reveal that the voltage from emitter to ground is typically around one-fourth to one-tenth of the supply voltage. Selecting the conservative case of one-tenth will permit calculating the emitter resistor R_E and the resistor R_C in a manner similar to the examples just completed. In the next example we perform a complete design of the network of Fig. 4.51 using the criteria just introduced for the emitter voltage.

EXAMPLE 4.22 Determine the resistor values for the network of Fig. 4.51 for the indicated operating point and supply voltage.

Solution:

$$V_E = \tfrac{1}{10}V_{CC} = \tfrac{1}{10}(20\text{ V}) = 2\text{ V}$$

$$R_E = \frac{V_E}{I_E} \cong \frac{V_E}{I_C} = \frac{2\text{ V}}{2\text{ mA}} = \mathbf{1\,k\Omega}$$

$$R_C = \frac{V_{R_C}}{I_C} = \frac{V_{CC} - V_{CE} - V_E}{I_C} = \frac{20\text{ V} - 10\text{ V} - 2\text{ V}}{2\text{ mA}} = \frac{8\text{ V}}{2\text{ mA}}$$
$$= \mathbf{4\,k\Omega}$$

$$I_B = \frac{I_C}{\beta} = \frac{2\text{ mA}}{150} = 13.33\,\mu\text{A}$$

$$R_B = \frac{V_{R_B}}{I_B} = \frac{V_{CC} - V_{BE} - V_E}{I_B} = \frac{20\text{ V} - 0.7\text{ V} - 2\text{ V}}{13.33\,\mu\text{A}}$$
$$\cong \mathbf{1.3\,M\Omega}$$

Design of a Current-Gain-Stabilized (Beta-Independent) Circuit

The circuit of Fig. 4.52 provides stabilization both for leakage and current gain (beta) changes. The four resistor values shown must be obtained for the specified operating point. Engineering judgment in selecting a value of emitter voltage V_E, as in the previous design consideration, leads to a direct, straightforward solution for all the resistor values. The design steps are all demonstrated in the next example.

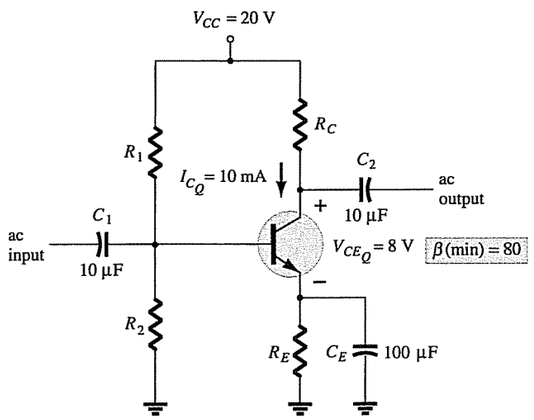


FIG. 4.52
Current-gain-stabilized circuit for design considerations.

EXAMPLE 4.23 Determine the levels of R_C, R_E, R_1, and R_2 for the network of Fig. 4.52 for the operating point indicated.

Solution:

$$V_E = \tfrac{1}{10}V_{CC} = \tfrac{1}{10}(20\text{ V}) = 2\text{ V}$$

$$R_E = \frac{V_E}{I_E} \cong \frac{V_E}{I_C} = \frac{2\text{ V}}{10\text{ mA}} = \mathbf{200\,\Omega}$$

$$R_C = \frac{V_{R_C}}{I_C} = \frac{V_{CC} - V_{CE} - V_E}{I_C} = \frac{20\text{ V} - 8\text{ V} - 2\text{ V}}{10\text{ mA}} = \frac{10\text{ V}}{10\text{ mA}}$$
$$= \mathbf{1\,k\Omega}$$

$$V_B = V_{BE} + V_E = 0.7\text{ V} + 2\text{ V} = 2.7\text{ V}$$

The equations for the calculation of the base resistors R_1 and R_2 will require a little thought. Using the value of base voltage calculated above and the value of the supply voltage will provide one equation—but there are two unknowns, R_1 and R_2. An additional equation can be obtained from an understanding of the operation of these two resistors in providing the necessary base voltage. For the circuit to operate efficiently, it is assumed that the current through R_1 and R_2 should be approximately equal to and much larger than the base current (at least 10:1). This fact and the voltage-divider equation for the base voltage provide the two relationships necessary to determine the base resistors. That is,

$$R_2 \leq \tfrac{1}{10}\beta R_E$$

and

$$V_B = \frac{R_2}{R_1 + R_2}\,V_{CC}$$

Substitution yields

$$R_2 \leq \tfrac{1}{10}(80)(0.2\,\text{k}\Omega)$$
$$= \mathbf{1.6\,k\Omega}$$

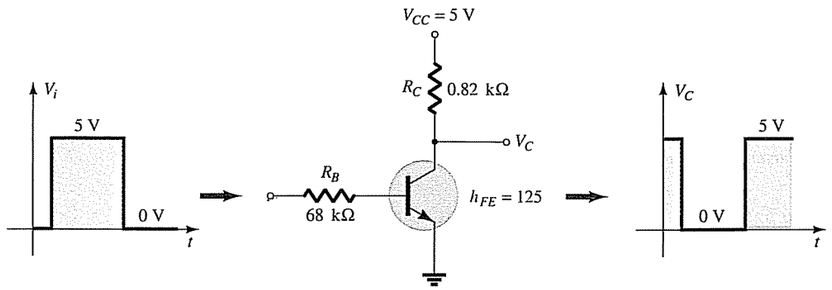
$$V_B = 2.7\text{ V} = \frac{(1.6\,\text{k}\Omega)(20\text{ V})}{R_1 + 1.6\,\text{k}\Omega}$$

and

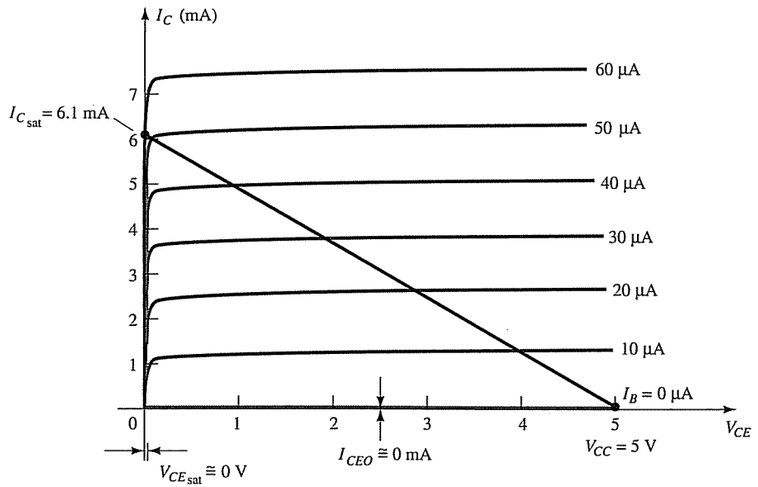
$$2.7R_1 + 4.32\,\text{k}\Omega = 32\,\text{k}\Omega$$
$$2.7R_1 = 27.68\,\text{k}\Omega$$
$$R_1 = \mathbf{10.25\,k\Omega} \quad (\text{use } 10\,\text{k}\Omega)$$

4.9 TRANSISTOR SWITCHING NETWORKS

The application of transistors is not limited solely to the amplification of signals. Through proper design transistors can be used as switches for computer and control applications. The network of Fig. 4.53a can be employed as an *inverter* in computer logic circuitry. Note that the output voltage V_C is opposite to that applied to the base or input terminal. In addition, note the absence of a dc supply connected to the base circuit. The only dc source is connected to the collector or output side, and for computer applications is typically equal to the magnitude of the "high" side of the applied signal—in this case 5 V.



(a)



(b)

FIG. 4.53
Transistor inverter.

Proper design for the inversion process requires that the operating point switch from cutoff to saturation along the load line depicted in Fig. 4.53b. For our purposes we will assume that $I_C = I_{CEO} = 0$ mA when $I_B = 0\ \mu$A (an excellent approximation in light of improving construction techniques), as shown in Fig. 4.53b. In addition, we will assume that $V_{CE} = V_{CE_{sat}} = 0$ V rather than the typical 0.1- to 0.3-V level.

When $V_i = 5$ V, the transistor will be "on" and the design must ensure that the network is heavily saturated by a level of I_B greater than that associated with the I_B curve appearing near the saturation level. In Fig. 4.53b, this requires that $I_B > 50\ \mu$A. The saturation level

for the collector current for the circuit of Fig. 4.53a is defined by

$$\boxed{I_{C_{sat}} = \frac{V_{CC}}{R_C}} \tag{4.45}$$

The level of I_B in the active region just before saturation results can be approximated by the following equation:

$$I_{B_{max}} \cong \frac{I_{C_{sat}}}{\beta_{dc}}$$

For the saturation level we must therefore ensure that the following condition is satisfied:

$$\boxed{I_B > \frac{I_{C_{sat}}}{\beta_{dc}}} \tag{4.46}$$

For the network of Fig. 4.53b, when $V_i = 5$ V, the resulting level of I_B is

$$I_B = \frac{V_i - 0.7\text{ V}}{R_B} = \frac{5\text{ V} - 0.7\text{ V}}{68\text{ k}\Omega} = 63\ \mu\text{A}$$

and

$$I_{C_{sat}} = \frac{V_{CC}}{R_C} = \frac{5\text{ V}}{0.82\text{ k}\Omega} \cong 6.1\text{ mA}$$

Testing Eq. (4.46) gives

$$I_B = 63\ \mu\text{A} > \frac{I_{C_{sat}}}{\beta_{dc}} = \frac{6.1\text{ mA}}{125} = 48.8\ \mu\text{A}$$

which is satisfied. Certainly, any level of I_B greater than 60 μA will pass through a Q-point on the load line that is very close to the vertical axis.

For $V_i = 0$ V, $I_B = 0\ \mu$A, and since we are assuming that $I_C = I_{CEO} = 0$ mA, the voltage drop across R_C as determined by $V_{R_C} = I_C R_C = 0$ V, resulting in $V_C = +5$ V for the response indicated in Fig. 4.53a.

In addition to its contribution to computer logic, the transistor can also be employed as a switch using the same extremities of the load line. At saturation, the current I_C is quite high and the voltage V_{CE} very low. The result is a resistance level between the two terminals determined by

$$R_{sat} = \frac{V_{CE_{sat}}}{I_{C_{sat}}}$$

and is depicted in Fig. 4.54.

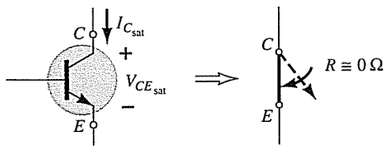


FIG. 4.54
Saturation conditions and the resulting terminal resistance.

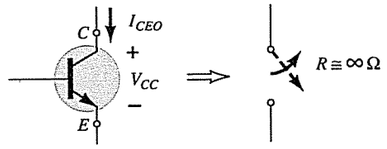


FIG. 4.55
Cutoff conditions and the resulting terminal resistance.

Using a typical average value of $V_{CE_{sat}}$ such as 0.15 V gives

$$R_{sat} = \frac{V_{CE_{sat}}}{I_{C_{sat}}} = \frac{0.15\text{ V}}{6.1\text{ mA}} = 24.6\ \Omega$$

which is a relatively low value and can be considered as approximately 0 Ω when placed in series with resistors in the kilohm range.

For $V_i = 0$ V, as shown in Fig. 4.55, the cutoff condition results in a resistance level of the following magnitude:

$$R_{cutoff} = \frac{V_{CC}}{I_{CEO}} = \frac{5\text{ V}}{0\text{ mA}} = \infty\ \Omega$$

resulting in the open-circuit equivalence. For a typical value of $I_{CEO} = 10\,\mu A$, the magnitude of the cutoff resistance is

$$R_{cutoff} = \frac{V_{CC}}{I_{CEO}} = \frac{5\text{ V}}{10\,\mu\text{A}} = \mathbf{500\,k\Omega}$$

which certainly approaches an open-circuit equivalence for many situations.



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EXAMPLE 4.24 Determine R_B and R_C for the transistor inverter of Fig. 4.56 if $I_{C_{sat}} = 10$ mA.

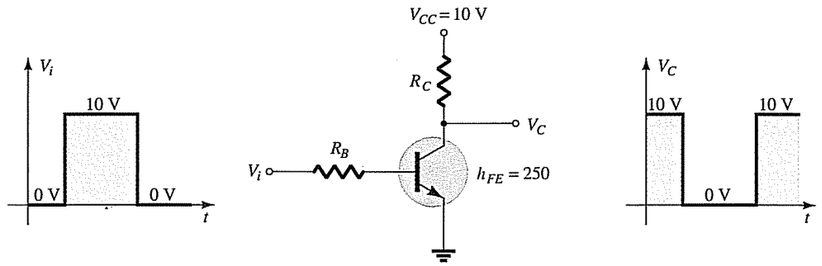


FIG. 4.56
Inverter for Example 4.24.

Solution: At saturation,

$$I_{C_{sat}} = \frac{V_{CC}}{R_C}$$

and

$$10\text{ mA} = \frac{10\text{ V}}{R_C}$$

so that

$$R_C = \frac{10\text{ V}}{10\text{ mA}} = 1\text{ k}\Omega$$

At saturation,

$$I_B \cong \frac{I_{C_{sat}}}{\beta_{dc}} = \frac{10\text{ mA}}{250} = 40\,\mu\text{A}$$

Choosing $I_B = 60\,\mu A$ to ensure saturation and using

$$I_B = \frac{V_i - 0.7\text{ V}}{R_B}$$

we obtain

$$R_B = \frac{V_i - 0.7\text{ V}}{I_B} = \frac{10\text{ V} - 0.7\text{ V}}{60\,\mu\text{A}} = 155\text{ k}\Omega$$

Choose $R_B = 150\,\text{k}\Omega$, which is a standard value. Then

$$I_B = \frac{V_i - 0.7\text{ V}}{R_B} = \frac{10\text{ V} - 0.7\text{ V}}{150\text{ k}\Omega} = 62\,\mu\text{A}$$

and

$$I_B = 62\,\mu\text{A} > \frac{I_{C_{sat}}}{\beta_{dc}} = 40\,\mu\text{A}$$

Therefore, use $R_B = \mathbf{150\,k\Omega}$ and $R_C = \mathbf{1\,k\Omega}$.

There are transistors that are referred to as *switching transistors* due to the speed with which they can switch from one voltage level to the other. In Fig. 3.23c the periods of time defined as t_s, t_d, t_r, and t_f are provided versus collector current. Their impact on the speed of response of the collector output is defined by the collector current response of Fig. 4.57.

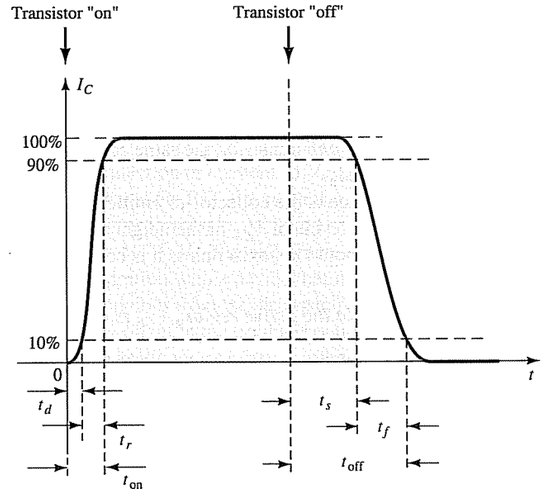


FIG. 4.57
Defining the time intervals of a pulse waveform.

The total time required for the transistor to switch from the "off" to the "on" state is designated as t_{on} and is defined by

$$\boxed{t_{on} = t_r + t_d} \qquad \textbf{(4.47)}$$

with t_d the delay time between the changing state of the input and the beginning of a response at the output. The time element t_r is the rise time from 10% to 90% of the final value.

The total time required for a transistor to switch from the "on" to the "off" state is referred to as t_{off} and is defined by

$$\boxed{t_{off} = t_s + t_f} \qquad \textbf{(4.48)}$$

where t_s is the storage time and t_f the fall time from 90% to 10% of the initial value.

For the general-purpose transistor of Fig. 3.23c at $I_C = 10$ mA, we find that

$$t_s = 120\text{ ns}$$
$$t_d = 25\text{ ns}$$
$$t_r = 13\text{ ns}$$

and $t_f = 12\text{ ns}$

so that $t_{on} = t_r + t_d = 13\text{ ns} + 25\text{ ns} = \mathbf{38\text{ ns}}$

and $t_{off} = t_s + t_f = 120\text{ ns} + 12\text{ ns} = \mathbf{132\text{ ns}}$

Comparing the values above with the following parameters of a BSV52L switching transistor reveals one of the reasons for choosing a switching transistor when the need arises:

$$t_{on} = \mathbf{12\text{ ns}} \quad \text{and} \quad t_{off} = \mathbf{18\text{ ns}}$$

4.10 TROUBLESHOOTING TECHNIQUES

The art of troubleshooting is such a broad topic that a full range of possibilities and techniques cannot be covered in a few sections of a book. However, the practitioner should be aware of a few basic maneuvers and measurements that can isolate the problem area and possibly identify a solution.

Quite obviously, the first step in being able to troubleshoot a network is to fully understand the behavior of the network and to have some idea of the expected voltage and current levels. For the transistor in the active region, the most important measurable dc level is the base-to-emitter voltage.

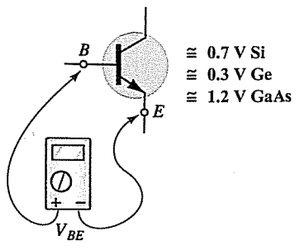


FIG. 4.58
Checking the dc level of V_{BE}.

For an "on" transistor, the voltage V_{BE} should be in the neighborhood of 0.7 V.

The proper connections for measuring V_{BE} appear in Fig. 4.58. Note that the positive (red) lead is connected to the base terminal for an *npn* transistor and the negative (black) lead to the emitter terminal. Any reading totally different from the expected level of about 0.7 V, such as 0, 4, or 12 V or a negative value, would be suspect and the device or network connections should be checked. For a *pnp* transistor, the same connections can be used, but a negative reading should be expected.

A voltage level of equal importance is the collector-to-emitter voltage. Recall from the general characteristics of a BJT that levels of V_{CE} in the neighborhood of 0.3 V suggest a saturated device—a condition that should not exist unless it is being employed in a switching mode. However:

For the typical transistor amplifier in the active region, V_{CE} is usually about 25% to 75% of V_{CC}.

For $V_{CC} = 20$ V, a reading of V_{CE} of 1 V to 2 V or from 18 V to 20 V as measured in Fig. 4.59 is certainly an uncommon result, and unless the device was knowingly designed for this response, the design and operation should be investigated. If $V_{CE} = 20$ V (with $V_{CC} = 20$ V) at least two possibilities exist—either the device (BJT) is damaged and has the characteristics of an open circuit between collector and emitter terminals or a connection in the collector–emitter or base–emitter circuit loop is open as shown in Fig. 4.60, establishing I_C at 0 mA and $V_{R_C} = 0$ V. In Fig. 4.60, the black lead of the voltmeter is connected to the

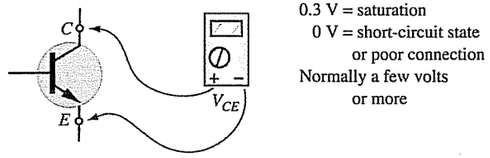


FIG. 4.59
Checking the dc level of V_{CE}.

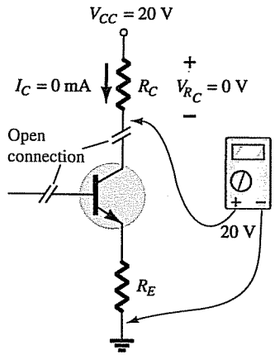


FIG. 4.60
Effect of a poor connection or damaged device.

common ground of the supply and the red lead to the bottom terminal of the resistor. The absence of a collector current and a resulting drop across R_C will result in a reading of 20 V. If the meter is connected to the collector terminal of the BJT, the reading will be 0 V since V_{CC} is blocked from the active device by the open circuit. One of the most common errors in the laboratory is the use of the wrong resistance value for a given design. Imagine the impact of using a 680-Ω resistor for R_B rather than the design value of 680 kΩ. For $V_{CC} = 20$ V and a fixed-bias configuration, the resulting base current would be

$$I_B = \frac{20\text{ V} - 0.7\text{ V}}{680\ \Omega} = 28.4\text{ mA}$$

rather than the desired 28.4 μA—a significant difference!

A base current of 28.4 mA would certainly place the design in a saturation region and possibly damage the device. Since actual resistor values are often different from the nominal color-code value (recall the common tolerance levels for resistive elements), it is time well spent to measure a resistor before inserting it in the network. The result is actual values closer to theoretical levels and some insurance that the correct resistance value is being employed.

There are times when frustration will develop. You check the device on a curve tracer or other BJT testing instrumentation and it looks good. All resistor levels seem correct, the connections appear solid, and the proper supply voltage has been applied—what next? Now the troubleshooter must strive to attain a higher level of sophistication. Could it be that the internal connection between the wire and the end connection of a lead is faulty? How often has simply touching a lead at the proper point created a "make or break" situation between connections? Perhaps the supply was turned on and set at the proper voltage but the current-limiting knob was left in the zero position, preventing the proper level of current as demanded by the network design. Obviously, the more sophisticated the system, the broader is the range of possibilities. In any case, one of the most effective methods of checking the operation of a network is to check various voltage levels with respect to ground by hooking up the black (negative) lead of a voltmeter to ground and "touching" the important terminals with the red (positive) lead. In Fig. 4.61, if the red lead is connected directly to V_{CC}, it should read V_{CC} volts since the network has one common ground for the supply and network parameters. At V_C the reading should be less, as determined by the drop across R_C, and V_E should be less than V_C by the collector–emitter voltage V_{CE}. The failure of any of these points to register what would appear to be a reasonable level may be sufficient in itself to define the faulty connection or element. If V_{R_C} and V_{R_E} are reasonable values but V_{CE} is 0 V, the possibility exists that the BJT is damaged and displays a short-circuit equivalence between collector and emitter terminals. As noted earlier, if V_{CE} registers a level of about 0.3 V as defined by $V_{CE} = V_C - V_E$ (the difference of the two levels as measured above), the network may be in saturation with a device that may or may not be defective.

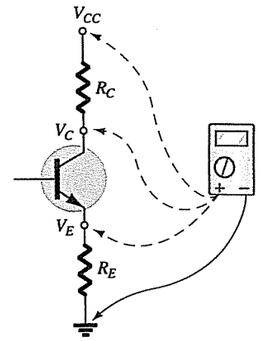


FIG. 4.61
Checking voltage levels with respect to ground.

It should be somewhat obvious from the discussion above that the voltmeter section of the VOM or DMM is quite important in the troubleshooting process. Current levels are usually calculated from the voltage levels across resistors rather than "breaking" the network to insert the milliammeter section of a multimeter. On large schematics, specific voltage levels are provided with respect to ground for easy checking and identification of possible problem areas. Of course, for the networks covered in this chapter, one must simply be aware of typical levels within the system as defined by the applied potential and general operation of the network.

All in all, the troubleshooting process is a true test of your clear understanding of the proper behavior of a network and the ability to isolate problem areas using a few basic measurements with the appropriate instruments. Experience is the key, and that will come only with continued exposure to practical circuits.

EXAMPLE 4.25 Based on the readings provided in Fig. 4.62, determine whether the network is operating properly and, if not, the probable cause.

Solution: The 20 V at the collector immediately reveals that $I_C = 0$ mA, due to an open circuit or a nonoperating transistor. The level of $V_{R_B} = 19.85$ V also reveals that the transistor is "off" since the difference of $V_{CC} - V_{R_B} = 0.15$ V is less than that required to turn "on" the transistor and provide some voltage for V_E. In fact, if we assume a short-circuit condition from base to emitter, we obtain the following current through R_B:

$$I_{R_B} = \frac{V_{CC}}{R_B + R_E} = \frac{20\text{ V}}{252\text{ k}\Omega} = 79.4\ \mu\text{A}$$

which matches that obtained from

$$I_{R_B} = \frac{V_{R_B}}{R_B} = \frac{19.85\text{ V}}{250\text{ k}\Omega} = 79.4\ \mu\text{A}$$

If the network were operating properly, the base current should be

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{20\text{ V} - 0.7\text{ V}}{250\text{ k}\Omega + (101)(2\text{ k}\Omega)} = \frac{19.3\text{ V}}{452\text{ k}\Omega} = 42.7\ \mu\text{A}$$

The result, therefore, is that the transistor is in a damaged state, with a short-circuit condition between base and emitter.

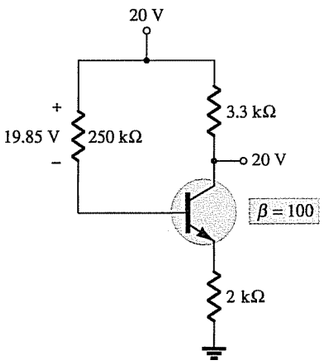


FIG. 4.62
Network for Example 4.25.

EXAMPLE 4.26 Based on the readings appearing in Fig. 4.63, determine whether the transistor is "on" and the network is operating properly.

Solution: Based on the resistor values of R_1 and R_2 and the magnitude of V_{CC}, the voltage $V_B = 4$ V seems appropriate (and in fact it is). The 3.3 V at the emitter results in a 0.7-V drop across the base-to-emitter junction of the transistor, suggesting an "on" transistor. However, the 20 V at the collector reveals that $I_C = 0$ mA, although the connection to the supply must be "solid" or the 20 V would not appear at the collector of the device. Two possibilities exist—there can be a poor connection between R_C and the collector terminal of the transistor or the transistor has an open base-to-collector junction. First, check the continuity at the collector junction using an ohm-meter, and if it is okay, check the transistor using one of the methods described in Chapter 3.

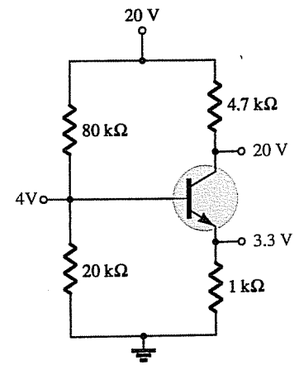


FIG. 4.63
Network for Example 4.26.

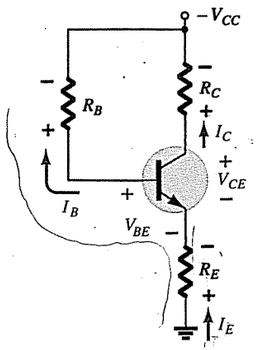


FIG. 4.64
pnp transistor in an emitter-stabilized configuration.

4.11 *pnp* TRANSISTORS

The analysis thus far has been limited totally to *npn* transistors to ensure that the initial analysis of the basic configurations was as clear as possible and uncomplicated by switching between types of transistors. Fortunately, the analysis of *pnp* transistors follows the same pattern established for *npn* transistors. The level of I_B is first determined, followed by the application of the appropriate transistor relationships to determine the list of unknown quantities. In fact, the only difference between the resulting equations for a network in which an *npn* transistor has been replaced by a *pnp* transistor is the sign associated with particular quantities.

As noted in Fig. 4.64, the double-subscript notation continues as normally defined. The current directions, however, have been reversed to reflect the actual conduction directions. Using the defined polarities of Fig. 4.64, both V_{BE} and V_{CE} will be negative quantities.

Applying Kirchhoff's voltage law to the base–emitter loop results in the following equation for the network of Fig. 4.64:

$$-I_E R_E + V_{BE} - I_B R_B + V_{CC} = 0$$

Substituting $I_E = (\beta + 1)I_B$ and solving for I_B yields

$$I_B = \frac{V_{CC} + V_{BE}}{R_B + (\beta + 1)R_E} \tag{4.49}$$

The resulting equation is the same as Eq. (4.17) except for the sign for V_{BE}. However, in this case $V_{BE} = -0.7$ V and the substitution of values results in the same sign for each term of Eq. (4.49) as Eq. (4.17). Keep in mind that the direction of I_B is now defined opposite of that for a *pnp* transistor as shown in Fig. 4.64.

For V_{CE} Kirchhoff's voltage law is applied to the collector–emitter loop, resulting in the following equation:

$$-I_E R_E + V_{CE} - I_C R_C + V_{CC} = 0$$

Substituting $I_E \cong I_C$ gives

$$V_{CE} = -V_{CC} + I_C(R_C + R_E) \tag{4.50}$$

The resulting equation has the same format as Eq. (4.19), but the sign in front of each term on the right of the equal sign has changed. Since V_{CC} will be larger than the magnitude of the succeeding term, the voltage V_{CE} will have a negative sign, as noted in an earlier paragraph.

EXAMPLE 4.27 Determine V_{CE} for the voltage-divider bias configuration of Fig. 4.65.

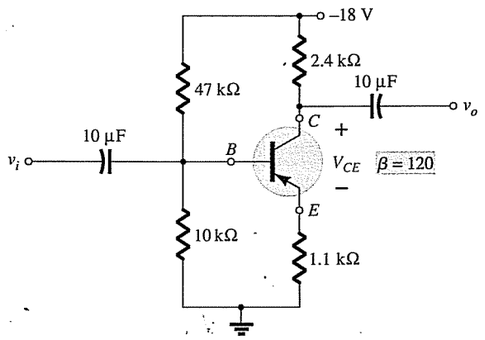


FIG. 4.65
pnp transistor in a voltage-divider bias configuration.

Solution: Testing the condition

$$\beta R_E \geq 10R_2$$

results in

$$(120)(1.1\,\text{k}\Omega) \geq 10(10\,\text{k}\Omega)$$
$$132\,\text{k}\Omega \geq 100\,\text{k}\Omega \quad (\textit{satisfied})$$

Solving for V_B, we have

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{(10\,\text{k}\Omega)(-18\,\text{V})}{47\,\text{k}\Omega + 10\,\text{k}\Omega} = -3.16\,\text{V}$$

Note the similarity in format of the equation with the resulting negative voltage for V_B.

Applying Kirchhoff's voltage law around the base–emitter loop yields

$$+V_B - V_{BE} - V_E = 0$$

and

$$V_E = V_B - V_{BE}$$

Substituting values, we obtain

$$V_E = -3.16\,\text{V} - (-0.7\,\text{V})$$
$$= -3.16\,\text{V} + 0.7\,\text{V}$$
$$= -2.46\,\text{V}$$

Note in the equation above that the standard single- and double-subscript notation is employed. For an *npn* transistor the equation $V_E = V_B - V_{BE}$ would be exactly the same. The only difference surfaces when the values are substituted.

The current is

$$I_E = \frac{V_E}{R_E} = \frac{2.46\,\text{V}}{1.1\,\text{k}\Omega} = 2.24\,\text{mA}$$

For the collector–emitter loop,

$$-I_E R_E + V_{CE} - I_C R_C + V_{CC} = 0$$

Substituting $I_E \cong I_C$ and gathering terms, we have

$$V_{CE} = -V_{CC} + I_C(R_C + R_E)$$

Substituting values gives

$$V_{CE} = -18\,\text{V} + (2.24\,\text{mA})(2.4\,\text{k}\Omega + 1.1\,\text{k}\Omega)$$
$$= -18\,\text{V} + 7.84\,\text{V}$$
$$= \mathbf{-10.16\,V}$$

4.12 BIAS STABILIZATION

The stability of a system is a measure of the sensitivity of a network to variations in its parameters. In any amplifier employing a transistor the collector current I_C is sensitive to each of the following parameters:

β: increases with increase in temperature

$|V_{BE}|$: decreases about 2.5 mV per degree Celsius (°C) increase in temperature

I_{CO} (reverse saturation current): doubles in value for every 10°C increase in temperature

Any or all of these factors can cause the bias point to drift from the designed point of operation. Table 4.1 reveals how the levels of I_{CO} and V_{BE} change with increase in temperature for a particular transistor. At room temperature (about 25°C) $I_{CO} = 0.1$ nA, whereas at 100°C (boiling point of water) I_{CO} is about 200 times larger, at 20 nA. For the same

TABLE 4.1
Variation of Silicon Transistor Parameters with Temperature

T (°C)	I_{CO} (nA)	β	V_{BE} (V)
−65	0.2×10^{-3}	20	0.85
25	0.1	50	0.65
100	20	80	0.48
175	3.3×10^{3}	120	0.3

temperature variation, β increases from 50 to 80 and V_{BE} drops from 0.65 to 0.48 V. Recall that I_B is quite sensitive to the level of V_{BE}, especially for levels beyond the threshold value.

The effect of changes in leakage current (I_{CO}) and current gain (β) on the dc bias point is demonstrated by the common-emitter collector characteristics of Fig. 4.66a and b. Figure 4.66 shows how the transistor collector characteristics change from a temperature of 25°C to a temperature of 100°C. Note that the significant increase in leakage current not only causes the curves to rise, but also causes an increase in beta, as revealed by the larger spacing between curves.

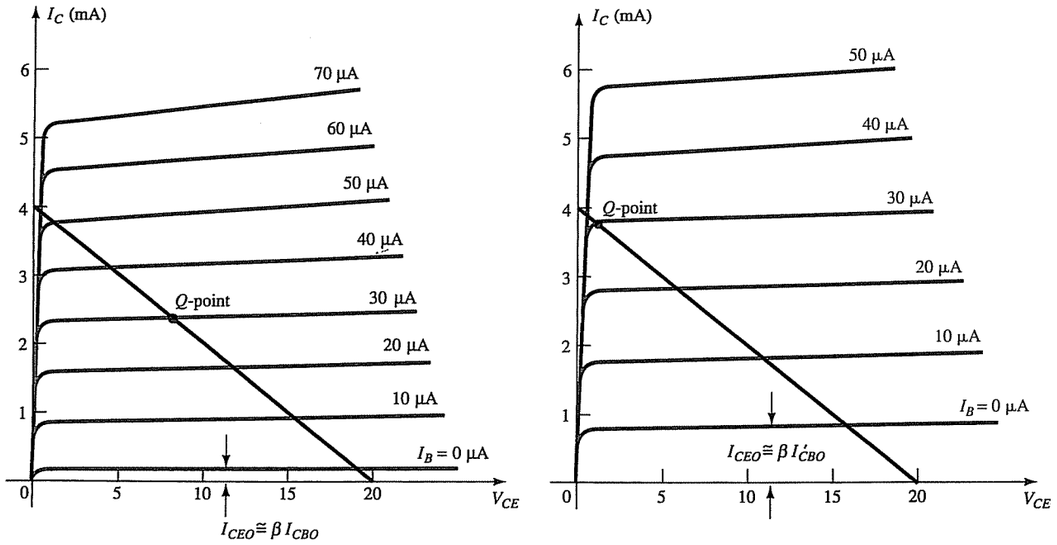


FIG. 4.66
Shift in dc bias point (Q-point) due to change in temperature: (a) 25°C; (b) 100°C.

An operating point may be specified by drawing the circuit dc load line on the graph of the collector characteristic and noting the intersection of the load line and the dc base current set by the input circuit. An arbitrary point is marked in Fig. 4.66a at $I_B = 30\ \mu A$. Since the fixed-bias circuit provides a base current whose value depends approximately on the supply voltage and base resistor, neither of which is affected by temperature or the change in leakage current or beta, the same base current magnitude will exist at high temperatures as indicated on the graph of Fig. 4.66b. As the figure shows, this will result in the dc bias point's shifting to a higher collector current and a lower collector–emitter voltage operating point. In the extreme, the transistor could be driven into saturation. In any case, the new operating point may not be at all satisfactory, and considerable distortion may result because of the bias-point shift. A better bias circuit is one that will stabilize or maintain the dc bias initially set, so that the amplifier can be used in a changing-temperature environment.

Stability Factors $S(I_{CO})$, $S(V_{BE})$, and $S(\beta)$

A stability factor S is defined for each of the parameters affecting bias stability as follows:

$$S(I_{CO}) = \frac{\Delta I_C}{\Delta I_{CO}} \tag{4.51}$$

$$S(V_{BE}) = \frac{\Delta I_C}{\Delta V_{BE}} \tag{4.52}$$

$$S(\beta) = \frac{\Delta I_C}{\Delta \beta} \tag{4.53}$$

In each case, the delta symbol (Δ) signifies change in that quantity. The numerator of each equation is the change in collector current as established by the change in the quantity in the denominator. For a particular configuration, if a change in I_{CO} fails to produce a significant change in I_C, the stability factor defined by $S(I_{CO}) = \Delta I_C/\Delta I_{CO}$ will be quite small. In other words:

Networks that are quite stable and relatively insensitive to temperature variations have low stability factors.

In some ways it would seem more appropriate to consider the quantities defined by Eqs. (4.51) through (4.53) to be sensitivity factors because:

The higher the stability factor, the more sensitive is the network to variations in that parameter.

The study of stability factors requires the knowledge of differential calculus. Our purpose here, however, is to review the results of the mathematical analysis and to form an overall assessment of the stability factors for a few of the most popular bias configurations. A great deal of literature is available on this subject, and if time permits, you are encouraged to read more on the subject.

$S(I_{CO})$: Emitter-Bias Configuration

For the emitter-bias configuration of Section 4.4, an analysis of the network results in

$$S(I_{CO}) = (\beta + 1)\frac{1 + R_B/R_E}{(\beta + 1) + R_B/R_E} \tag{4.54}$$

For $R_B/R_E \gg (\beta + 1)$, Eq. (4.54) reduces to the following:

$$S(I_{CO}) = \beta + 1 \tag{4.55}$$

as shown on the graph of $S(I_{CO})$ versus R_B/R_E in Fig. 4.67.

For $R_B/R_E \ll 1$, Eq. (4.54) will approach the following level (as shown in Fig. 4.67):

$$S(I_{CO}) = (\beta + 1)\frac{1}{(\beta + 1)} = \rightarrow 1 \tag{4.56}$$

revealing that the stability factor will approach its lowest level as R_E becomes sufficiently large. Keep in mind, however, that good bias control normally requires that R_B be greater

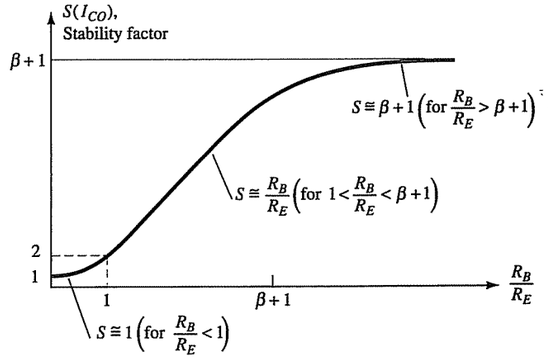


FIG. 4.67
Variation of stability factor $S(I_{CO})$ with the resistor ratio R_B/R_E for the emitter-bias configuration.

than R_E. The result therefore is a situation where the best stability levels are associated with poor design criteria. Obviously, a trade-off must occur that will satisfy both the stability and bias specifications. It is interesting to note in Fig. 4.67 that the lowest value of $S(I_{CO})$ is 1, revealing that I_C will always increase at a rate equal to or greater than I_{CO}.

For the range where R_B/R_E ranges between 1 and $(\beta + 1)$, the stability factor will be determined by

$$S(I_{CO}) \cong \frac{R_B}{R_E} \tag{4.57}$$

as shown in Fig. 4.67. The results reveal that the emitter-bias configuration is quite stable when the ratio R_B/R_E is as small as possible and the least stable when the same ratio approaches $(\beta + 1)$.

EXAMPLE 4.28 Calculate the stability factor and the change in I_C from 25°C to 100°C for the transistor defined by Table 4.1 for the following emitter-bias arrangements:

a. $R_B/R_E = 250$ $(R_B = 250R_E)$.
b. $R_B/R_E = 10$ $(R_B = 10R_E)$.
c. $R_B/R_E = 0.01$ $(R_E = 100R_B)$.

Solution:

a. $$S(I_{CO}) = (\beta + 1)\frac{1 + R_B/R_E}{(\beta + 1) + R_B/R_E}$$
$$= 51\left(\frac{1 + 250}{51 + 250}\right) = 51\left(\frac{251}{301}\right)$$
$$\cong \mathbf{42.53}$$

which begins to approach the level defined by $\beta + 1 = 51$.
The change in I_C is given by

$$\Delta I_C = [S(I_{CO})](\Delta I_{CO}) = (42.53)(19.9\,\text{nA})$$
$$\cong \mathbf{0.85\ \mu A}$$

b. $$S(I_{CO}) = (\beta + 1)\frac{1 + R_B/R_E}{1 + \beta + R_B/R_E}$$
$$= 51\left(\frac{1 + 10}{51 + 10}\right) = 51\left(\frac{11}{61}\right)$$
$$\cong \mathbf{9.2}$$
$$\Delta I_C = [S(I_{CO})](\Delta I_{CO}) = (9.2)(19.9\,\text{nA})$$
$$\cong \mathbf{0.18\ \mu A}$$

c. $$S(I_{CO}) = (\beta + 1)\frac{1 + R_B/R_E}{1 + \beta + R_B/R_E}$$
$$= 51\left(\frac{1 + 0.01}{51 + 0.01}\right) = 51\left(\frac{1.01}{51.01}\right)$$
$$\cong \mathbf{1.01}$$

which is certainly very close to the level of 1 forecast if $R_B/R_E \ll 1$.
We have

$$\Delta I_C = [S(I_{CO})](\Delta I_{CO}) = 1.01(19.9\,\text{nA})$$
$$= \mathbf{20.1\ nA}$$

Example 4.28 reveals how lower and lower levels of I_{CO} for the modern-day BJT transistor have improved the stability level of the basic bias configurations. Even though the change in I_C is considerably different in a circuit having ideal stability $(S = 1)$ from one having a stability factor of 42.53, the change in I_C is not that significant. For example, the amount of change in I_C from a dc bias current set at, say, 2 mA, would be from 2 mA to 2.085 mA in the worst case, which is obviously small enough to be ignored for most applications. Some power transistors exhibit larger leakage currents, but for most amplifier circuits the lower levels of I_{CO} have had a very positive impact on the stability question.

Fixed-Bias Configuration

For the fixed-bias configuration, if we multiply the top and bottom of Eq. (4.54) by R_E and then plug in $R_E = 0\ \Omega$, the following equation results:

$$S(I_{CO}) = \beta + 1 \tag{4.58}$$

Note that the resulting equation matches the maximum value for the emitter-bias configuration. The result is a configuration with a poor stability factor and a high sensitivity to variations in I_{CO}.

Voltage-Divider Bias Configuration

Recall from Section 4.5 the development of the Thévenin equivalent network appearing in Fig. 4.68, for the voltage-divider bias configuration. For the network of Fig. 4.68, the equation for $S(I_{CO})$ is the following:

$$S(I_{CO}) = (\beta + 1)\frac{1 + R_{Th}/R_E}{(\beta + 1) + R_{Th}/R_E} \tag{4.59}$$

Note the similarities with Eq. (4.54), where it was determined that $S(I_{CO})$ had its lowest level and the network had its greatest stability when $R_E > R_B$. For Eq. (4.59), the corresponding condition is $R_E > R_{Th}$, or R_{Th}/R_E should be as small as possible. For the voltage-divider bias configuration, R_{Th} can be much less than the corresponding R_{Th} of the emitter-bias configuration and still have an effective design.

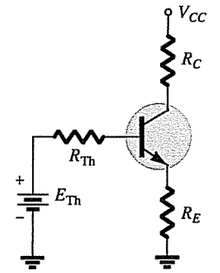


FIG. 4.68
Equivalent circuit for the voltage-divider configuration.

Feedback-Bias Configuration ($R_E = 0\ \Omega$)

In this case,

$$S(I_{CO}) = (\beta + 1)\frac{1 + R_B/R_C}{(\beta + 1) + R_B/R_C} \tag{4.60}$$

Since the equation is similar in format to that obtained for the emitter-bias and voltage-divider bias configurations, the same conclusions regarding the ratio R_B/R_C can be applied here also.

Physical Impact

Equations of the type developed above often fail to provide a physical sense for why the networks perform as they do. We are now aware of the relative levels of stability and how the choice of parameters can affect the sensitivity of the network, but without the equations it may be difficult for us to explain in words why one network is more stable than another. The next few paragraphs attempt to fill this void through the use of some of the very basic relationships associated with each configuration.

For the fixed-bias configuration of Fig. 4.69a, the equation for the base current is

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

with the collector current determined by

$$I_C = \beta I_B + (\beta + 1)I_{CO} \tag{4.61}$$

If I_C as defined by Eq. (4.61) should increase due to an increase in I_{CO}, there is nothing in the equation for I_B that would attempt to offset this undesirable increase in current level

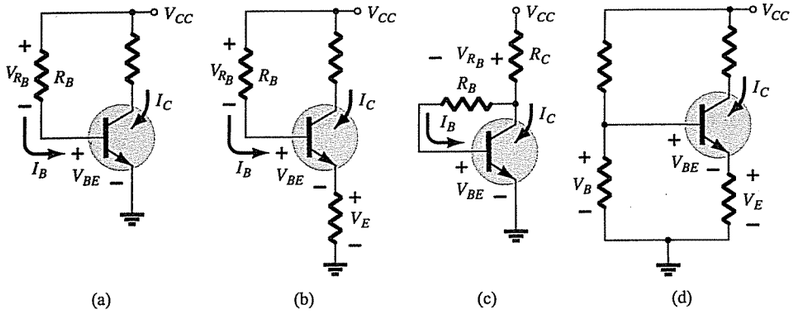


FIG. 4.69
Review of biasing managements and the stability factor $S(I_{CO})$.

(assuming V_{BE} remains constant). In other words, the level of I_C would continue to rise with temperature, with I_B maintaining a fairly constant value—a very unstable situation.

For the emitter-bias configuration of Fig. 4.69b, however, an increase in I_C due to an increase in I_{CO} will cause the voltage $V_E = I_E R_E \cong I_C R_E$ to increase. The result is a drop in the level of I_B as determined by the following equation:

$$I_B \downarrow = \frac{V_{CC} - V_{BE} - V_E \uparrow}{R_B} \tag{4.62}$$

A drop in I_B will have the effect of reducing the level of I_C through transistor action and thereby offset the tendency of I_C to increase due to an increase in temperature. In total, therefore, the configuration is such that there is a reaction to an increase in I_C that will tend to oppose the change in bias conditions.

The feedback configuration of Fig. 4.69c operates in much the same way as the emitter-bias configuration when it comes to levels of stability. If I_C should increase due to an increase in temperature, the level of V_{R_C} will increase in the equation

$$I_B \downarrow = \frac{V_{CC} - V_{BE} - V_{R_C} \uparrow}{R_B} \tag{4.63}$$

and the level of I_B will decrease. The result is a stabilizing effect as described for the emitter-bias configuration. One must be aware that the action described above does not happen in a step-by-step sequence. Rather, it is a simultaneous action to maintain the established bias conditions. In other words, the very instant I_C begins to rise, the network will sense the change and the balancing effect described above will take place.

The most stable of the configurations is the voltage-divider bias network of Fig. 4.69d. If the condition $\beta R_E \gg 10R_2$ is satisfied, the voltage V_B will remain fairly constant for changing levels of I_C. The base-to-emitter voltage of the configuration is determined by $V_{BE} = V_B - V_E$. If I_C should increase, V_E will increase as described above, and for a constant V_B the voltage V_{BE} will drop. A drop in V_{BE} will establish a lower level of I_B, which will try to offset the increased level of I_C.

$S(V_{BE})$

The stability factor is defined by

$$S(V_{BE}) = \frac{\Delta I_C}{\Delta V_{BE}}$$

and results in the following equation for the emitter-bias configuration:

$$\boxed{S(V_{BE}) = \frac{-\beta}{R_B + (\beta + 1)R_E}} \tag{4.64}$$

Substituting $R_E = 0\ \Omega$ as occurs for the fixed-bias configuration results in

$$\boxed{S(V_{BE}) = -\frac{\beta}{R_B}} \tag{4.65}$$

Equation (4.64) can be written in the following form:

$$S(V_{BE}) = \frac{-\beta/R_E}{R_B/R_E + (\beta + 1)} \tag{4.66}$$

Substituting the condition $(\beta + 1) \gg R_B/R_E$ results in the following equation for $S(V_{BE})$:

$$\boxed{S(V_{BE}) \cong \frac{-\beta/R_E}{\beta + 1} \cong \frac{-\beta/R_E}{\beta} = -\frac{1}{R_E}} \tag{4.67}$$

which shows that the larger the resistance R_E, the lower is the stability factor and the more stable is the system.

EXAMPLE 4.29 Determine the stability factor $S(V_{BE})$ and the change in I_C from 25°C to 100°C for the transistor defined by Table 4.1 for the following bias arrangements.

a. Fixed-bias with $R_B = 240\ \text{k}\Omega$ and $\beta = 100$.
b. Emitter-bias with $R_B = 240\ \text{k}\Omega$, $R_E = 1\ \text{k}\Omega$, and $\beta = 100$.
c. Emitter-bias with $R_B = 47\ \text{k}\Omega$, $R_E = 4.7\ \text{k}\Omega$, and $\beta = 100$.

Solution:

a. Eq. (4.65):
$$S(V_{BE}) = -\frac{\beta}{R_B} = -\frac{100}{240\ \text{k}\Omega} = \mathbf{-0.417 \times 10^{-3}}$$

and
$$\Delta I_C = [S(V_{BE})](\Delta V_{BE}) = (-0.417 \times 10^{-3})(0.48\ \text{V} - 0.65\ \text{V}) = (-0.417 \times 10^{-3})(-0.17\ \text{V}) = \mathbf{70.9\ \mu A}$$

b. In this case, $(\beta + 1) = 101$ and $R_B/R_E = 240$. The condition $(\beta + 1) \gg R_B/R_E$ is not satisfied, negating the use of Eq. (4.67) and requiring the use of Eq. (4.64).

Eq. (4.64):
$$S(V_{BE}) = \frac{-\beta}{R_B + (\beta + 1)R_E} = \frac{-100}{240\ \text{k}\Omega + (101)1\ \text{k}\Omega} = -\frac{100}{341\ \text{k}\Omega} = \mathbf{-0.293 \times 10^{-3}}$$

which is about 30% less than the fixed-bias value due to the additional $(\beta + 1)R_E$ term in the denominator of the $S(V_{BE})$ equation. We have

$$\Delta I_C = [S(V_{BE})](\Delta V_{BE}) = (-0.293 \times 10^{-3})(-0.17\ \text{V}) \cong \mathbf{50\ \mu A}$$

c. In this case,

$$(\beta + 1) = 101 \gg \frac{R_B}{R_E} = \frac{47\ \text{k}\Omega}{4.7\ \text{k}\Omega} = 10\ (\textit{satisfied})$$

Eq. (4.67):
$$S(V_{BE}) = -\frac{1}{R_E} = -\frac{1}{4.7\ \text{k}\Omega} = \mathbf{-0.212 \times 10^{-3}}$$

and
$$\Delta I_C = [S(V_{BE})](\Delta V_{BE}) = (-0.212 \times 10^{-3})(-0.17\ \text{V}) = \mathbf{36.04\ \mu A}$$

In Example 4.29, the increase of 70.9 μA will have some impact on the level of I_{C_Q}. For a situation where $I_{C_Q} = 2$ mA, the resulting collector current increases to a 3.5% increase.

$$I_{C_Q} = 2\,\text{mA} + 70.9\,\mu\text{A}$$
$$= 2.0709\,\text{mA}$$

For the voltage-divider configuration, the level of R_B will be changed to R_{Th} in Eq. (4.64) (as defined by Fig. 4.68). In Example 4.29, the use of $R_B = 47\,\text{k}\Omega$ is a questionable design. However, R_{Th} for the voltage-divider configuration can be this level or lower and still maintain good design characteristics. The resulting equation for $S(V_{BE})$ for the feedback network will be similar to that of Eq. (4.64) with R_E replaced by R_C.

$S(\beta)$

The last stability factor to be investigated is that of $S(\beta)$. The mathematical development is more complex than that encountered for $S(I_{CO})$ and $S(V_{BE})$, as suggested by the following equation for the emitter-bias configuration:

$$S(\beta) = \frac{\Delta I_C}{\Delta \beta} = \frac{I_{C_1}(1 + R_B/R_E)}{\beta_1(1 + \beta_2 + R_B/R_E)} \tag{4.68}$$

The notation I_{C_1} and β_1 is used to define their values under one set of network conditions, whereas the notation β_2 is used to define the new value of beta as established by such causes as temperature change, variation in β for the same transistor, or a change in transistors.

EXAMPLE 4.30 Determine I_{C_Q} at a temperature of 100°C if $I_{C_Q} = 2$ mA at 25°C. Use the transistor described by Table 4.1, where $\beta_1 = 50$ and $\beta_2 = 80$, and a resistance ratio R_B/R_E of 20.

Solution:

Eq. (4.68):
$$S(\beta) = \frac{I_{C_1}(1 + R_B/R_E)}{\beta_1(1 + \beta_2 + R_B/R_E)}$$
$$= \frac{(2 \times 10^{-3})(1 + 20)}{(50)(1 + 80 + 20)} = \frac{42 \times 10^{-3}}{5050}$$
$$= \mathbf{8.32 \times 10^{-6}}$$

and
$$\Delta I_C = [S(\beta)][\Delta\beta]$$
$$= (8.32 \times 10^{-6})(30)$$
$$\cong \mathbf{0.25\ mA}$$

In conclusion, therefore, the collector current changed from 2 mA at room temperature to 2.25 mA at 100°C, representing a change of 12.5%.

The fixed-bias configuration is defined by $S(\beta) = I_{C_1}/\beta_1$, and R_B of Eq. (4.68) can be replaced by R_{Th} for the voltage-divider configuration.

For the collector feedback configuration with $R_E = 0\,\Omega$,

$$S(\beta) = \frac{I_{C_1}(R_B + R_C)}{\beta_1(R_B + R_C(1 + \beta_2))} \tag{4.69}$$

Summary

Now that the three stability factors of importance have been introduced, the total effect on the collector current can be determined using the following equation:

$$\Delta I_C = S(I_{CO})\Delta I_{CO} + S(V_{BE})\Delta V_{BE} + S(\beta)\Delta\beta \tag{4.70}$$

The equation may initially appear quite complex, but note that each component is simply a stability factor for the configuration multiplied by the resulting change in a parameter between the temperature limits of interest. In addition, the ΔI_C to be determined is simply the change in I_C from the level at room temperature.

For instance, if we examine the fixed-bias configuration, Eq. (4.70) becomes

$$\Delta I_C = (\beta + 1)\Delta I_{CO} - \frac{\beta}{R_B}\Delta V_{BE} + \frac{I_{C_1}}{\beta_1}\Delta\beta \tag{4.71}$$

after substituting the stability factors as derived in this section. Let us now use Table 4.1 to find the change in collector current for a temperature change from 25°C (room temperature) to 100°C (the boiling point of water). For this range the table reveals that

$$\Delta I_{CO} = 20\,\text{nA} - 0.1\,\text{nA} = 19.9\,\text{nA}$$
$$\Delta V_{BE} = 0.48\,\text{V} - 0.65\,\text{V} = -0.17\,\text{V} \quad \text{(note the sign)}$$

and
$$\Delta\beta = 80 - 50 = 30$$

Starting with a collector current of 2 mA with an R_B of 240 kΩ, we obtain the resulting change in I_C due to an increase in temperature of 75°C as follows:

$$\Delta I_C = (50 + 1)(19.9\,\text{nA}) - \frac{50}{240\,\text{k}\Omega}(-0.17\,\text{V}) + \frac{2\,\text{mA}}{50}(30)$$
$$= 1.01\,\mu\text{A} + 35.42\,\mu\text{A} + 1200\,\mu\text{A}$$
$$= 1.236\,\text{mA}$$

which is a significant change due primarily to the change in β. The collector current has increased from 2 mA to 3.236 mA, but this was expected in the sense that we recognize from the content of this section that the fixed-bias configuration is the least stable.

If the more stable voltage-divider configuration is employed with a ratio $R_{\text{Th}}/R_E = 2$ and $R_E = 4.7\,\text{k}\Omega$, then

$$S(I_{CO}) = 2.89, \quad S(V_{BE}) = -0.2 \times 10^{-3}, \quad S(\beta) = 1.445 \times 10^{-6}$$

and
$$\Delta I_C = (2.89)(19.9\,\text{nA}) - 0.2 \times 10^{-3}(-0.17\,\text{V}) + 1.445 \times 10^{-6}(30)$$
$$= 57.51\,\text{nA} + 34\,\mu\text{A} + 43.4\,\mu\text{A}$$
$$= 0.077\,\text{mA}$$

The resulting collector current is 2.077 mA, or essentially 2.1 mA, compared to the 2.0 mA at 25°C. The network is obviously a great deal more stable than the fixed-bias configuration, as mentioned in earlier discussions. In this case, $S(\beta)$ did not override the other two factors and the effects of $S(V_{BE})$ and $S(I_{CO})$ were equally important. In fact, at higher temperatures, the effects of $S(I_{CO})$ and $S(V_{BE})$ will be greater than $S(\beta)$ for the device of Table 4.1. For temperatures below 25°C, I_C will decrease with increasingly negative temperature levels.

The effect of $S(I_{CO})$ in the design process is becoming a lesser concern because of improved manufacturing techniques, which continue to lower the level of $I_{CO} = I_{CBO}$. It should also be mentioned that for a particular transistor the variation in levels of I_{CBO} and V_{BE} from one transistor to another in a lot is almost negligible compared to the variation in beta. In addition, the results of the analysis above support the fact that for a good stabilized design:

General Conclusion:

The ratio R_B/R_E or R_{Th}/R_E should be as small as possible with due consideration to all aspects of the design, including the ac response.

Although the analysis above may have been clouded by some of the complex equations for some of the sensitivities, the purpose here was to develop a higher level of awareness of the factors that go into a good design and to be more intimate with the transistor parameters and their impact on the network's performance. The analysis of the earlier sections was for idealized situations with nonvarying parameter values. We are now more aware of how the dc response of the design can vary with the parameter variations of a transistor.

4.13 PRACTICAL APPLICATIONS

As with the diodes in Chapter 2, it would be virtually impossible to provide even a surface treatment of the broad areas of application of BJTs. However, a few applications are chosen here to demonstrate how different facets of the characteristics of BJTs are used to perform various functions.

Relay Driver

This application is in some ways a continuation of the discussion introduced for diodes about how the effects of inductive kick can be minimized through proper design. In Fig. 4.70a, a transistor is used to establish the current necessary to energize the relay in the collector circuit. With no input at the base of the transistor, the base current, collector current, and coil current are essentially 0 A, and the relay sits in the unenergized state (normally open, NO). However, when a positive pulse is applied to the base, the transistor turns on, establishing sufficient current through the coil of the electromagnet to close the relay. Problems can now develop when the signal is removed from the base to turn off the transistor and deenergize the relay. Ideally, the current through the coil and the transistor will quickly drop to zero, the arm of the relay will be released, and the relay will simply remain dormant until the next "on" signal. However, we know from our basic circuit courses that the current through a coil cannot change instantaneously, and, in fact, the more quickly it changes, the greater the induced voltage across the coil as defined by $v_L = L(di_L/dt)$. In this case, the rapidly changing current through the coil will develop a large voltage across the coil with the polarity shown in Fig. 4.70a, which will appear directly across the output of the transistor. The chances are likely that its magnitude will exceed the maximum ratings of the transistor, and the semiconductor device will be permanently damaged. The voltage across the coil will not remain at its highest switching level but will oscillate as shown until its level drops to zero as the system settles down.

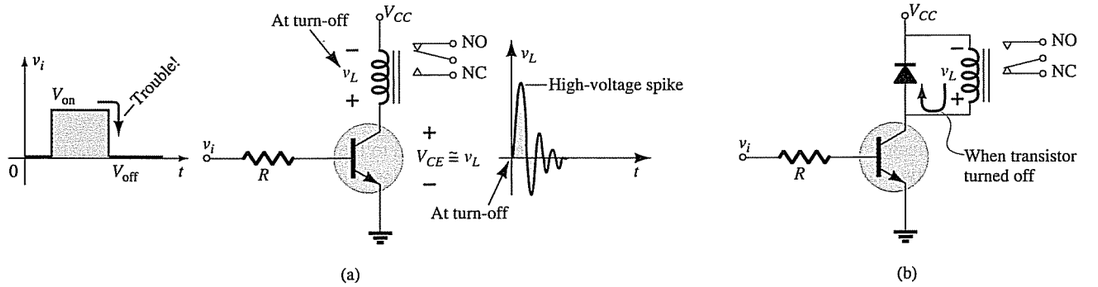


FIG. 4.70
Relay driver: (a) absence of protective device; (b) with a diode across the relay coil.

This destructive action can be subdued by placing a diode across the coil as shown in Fig. 4.70b. During the "on" state of the transistor, the diode is back-biased; it sits like an open circuit and doesn't affect a thing. However, when the transistor turns off, the voltage across the coil will reverse and will forward-bias the diode, placing the diode in its "on" state. The current through the inductor established during the "on" state of the transistor can then continue to flow through the diode, eliminating the severe change in current level. Because the inductive current is switched to the diode almost instantaneously after the "off" state is established, the diode must have a current rating to match the current through the inductor and the transistor when in the "on" state. Eventually, because of the resistive elements in the loop, including the resistance of the coil windings and the diode, the high-frequency (quickly oscillating) variation in voltage level across the coil will decay to zero, and the system will settle down.

Transistor Switch

In Fig. 4.71a, a transistor is used as a switch to control the "on" and "off" states of the light bulb in the collector branch of the network. When the switch is in the "on" position, we have a fixed-bias situation where the base-to-emitter voltage is at its 0.7-V level, and the base current is controlled by the resistor R_1 and the input impedance of the transistor. The current through the bulb will then be beta times the base current, and the bulb will light up. A problem can develop, however, if the bulb has not been on for a while. When a light bulb is first turned on, its resistance is quite low, even though the resistance will increase rapidly the longer the bulb is on. This can cause a momentary high level of collector current, which could damage the bulb and the transistor over time. In Fig. 4.71b, for instance, the load line for the same network with a cold and a hot resistance for the bulb is included. Note that even though the base current is set by the base circuit, the intersection with the load line results in a higher current for the cold light bulb. Any concern about the turn-on level can easily be corrected by inserting an additional small resistor in series with the light bulb, as shown in Fig. 4.71c, just to ensure a limit on the initial surge in current when the bulb is first turned on.

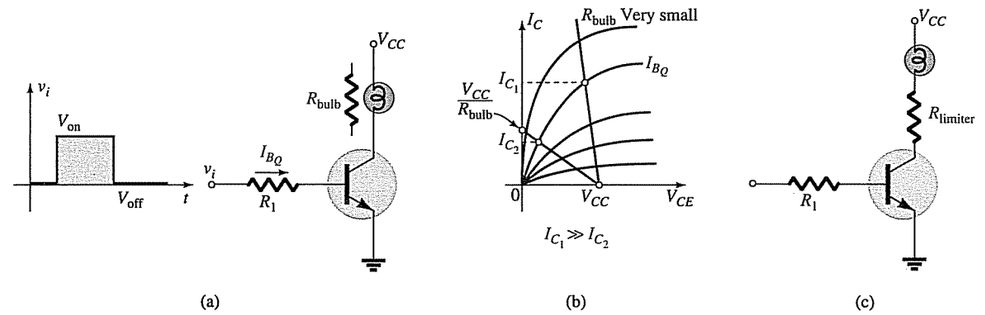


FIG. 4.71
Using the transistor as a switch to control the on–off states of a bulb: (a) network; (b) effect of low bulb resistance on collector current; (c) limiting resistor.

Constant-Current Source (CCS)

If we assume that the characteristics of a transistor appear as shown in Fig. 4.72a (constant beta throughout), an excellent current source can be created using the simple transistor configuration shown in Fig. 4.72b because no matter what the load resistance, the collector or load current will remain the same as shown in Fig. 4.72c. The base current is fixed; no matter where the load line is, the collector current remains the same. In other words, the collector current is independent of the load in the collector circuit—a perfect current source. However, because the actual characteristics are more like those in Fig. 4.71b, where beta will vary from point to point, and even though the base current may be fixed by the configuration, the beta will vary from point to point with the load intersection, and $I_C = I_L$ will vary—not characteristic of a good current source. Recall, however, that the voltage-divider

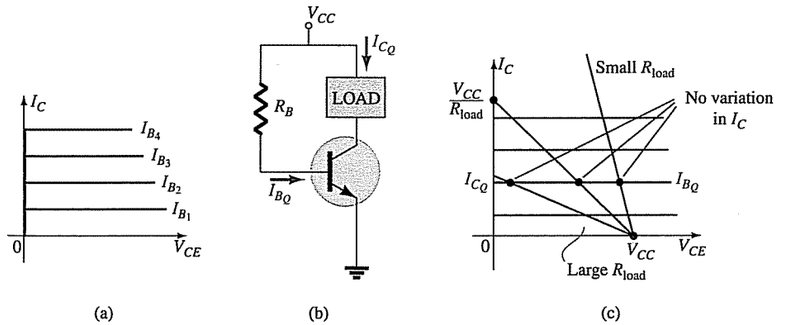


FIG. 4.72
Building a constant-current source assuming ideal BJT characteristics: (a) ideal characteristics; (b) network; (c) demonstrating why I_C remains constant.

configuration resulted in a low level of sensitivity to beta, so perhaps if that biasing arrangement is used, the current source equivalent is closer to reality. In fact, that is the case. If a biasing arrangement such as shown in Fig. 4.73 is employed, the sensitivity to changes in operating point due to varying loads is much less, and the collector current will remain fairly constant for changes in load resistance in the collector branch. In fact, the emitter voltage is determined by

$$V_E = V_B - 0.7\,\text{V}$$

with the collector or load current determined by

$$I_C \cong I_E = \frac{V_E}{R_E} = \frac{V_B - 0.7\,V}{R_E}$$

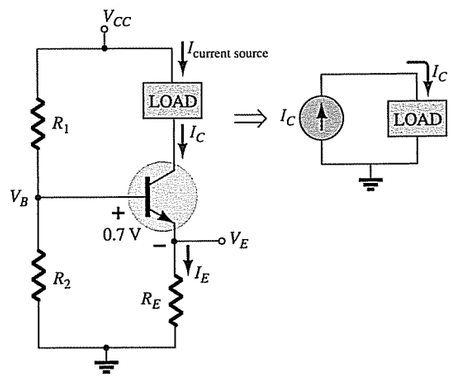


FIG. 4.73
Network establishing a fairly constant current source due to its reduced sensitivity to changes in beta.

Using Fig. 4.73, we can describe the improved stability by examining the case where I_C may be trying to rise for any number of reasons. The result is that $I_E = I_C$ will also rise and the voltage $V_{R_E} = I_E R_E$ will increase. However, if we assume V_B to be fixed (a good assumption since its level is determined by two fixed resistors and a voltage source), the base-to-emitter voltage $V_{BE} = V_B - V_{R_E}$ will drop. A drop in V_{BE} will cause I_B and therefore $I_C\,(= \beta I_B)$ to drop. The result is a situation where any tendency for I_C to increase will be met with a network reaction that will work against the change to stabilize the system.

Alarm System with a CCS

An alarm system with a constant-current source of the type just introduced appears in Fig. 4.74. Since $\beta R_E = (100)(1\,\text{k}\Omega) = 100\,\text{k}\Omega$ is much greater than R_1, we can use the approximate approach and find the voltage V_{R_1},

$$V_{R_1} = \frac{2\,\text{k}\Omega(16\,\text{V})}{2\,\text{k}\Omega + 4.7\,\text{k}\Omega} = 4.78\,\text{V}$$

and then the voltage across R_E,

$$V_{R_E} = V_{R_1} - 0.7\,\text{V} = 4.78\,\text{V} - 0.7\,\text{V} = 4.08\,\text{V}$$

and finally the emitter and collector current,

$$I_E = \frac{V_{R_E}}{R_E} = \frac{4.08\,\text{V}}{1\,\text{k}\Omega} = 4.08\,\text{mA} \cong 4\,\text{mA} = I_C$$

Since the collector current is the current through the circuit, the 4-mA current will remain fairly constant for slight variations in network loading. Note that the current passes through a series of sensor elements and finally into an op-amp designed to compare the 4-mA level with the set level of 2 mA. (Although the op-amp may be a new device to you, it will be discussed in detail in Chapter 10—you will not need to know the details of its behavior for this application.)

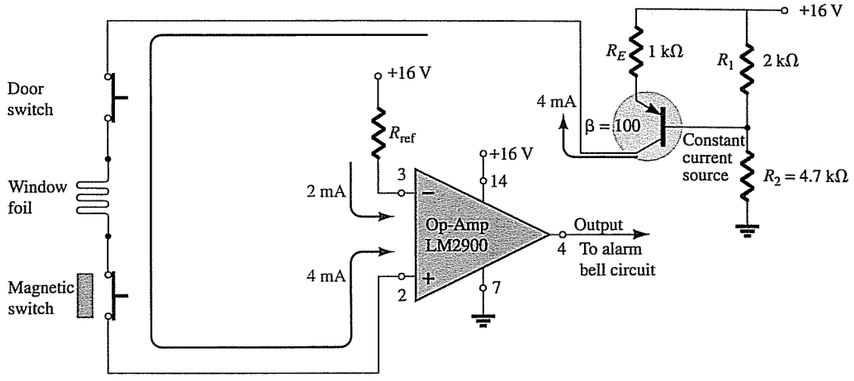


FIG. 4.74
An alarm system with a constant-current source and an op-amp comparator.

The LM2900 operational amplifier of Fig. 4.74 is one of four found in the dual-in-line integrated circuit package appearing in Fig. 4.75a. Pins 2, 3, 4, 7, and 14 were used for the design of Fig. 4.74. For the sake of interest only, note in Fig. 4.75b the number of elements required to establish the desired terminal characteristics for the op-amp—as mentioned earlier, the details of its internal operation are left for another time. The 2 mA at terminal 3 of the op-amp is a *reference* current established by the 16-V source and R_{ref} at the negative side of the op-amp input. The 2-mA current level is required as a level against which the 4-mA current of the network is to be compared. As long as the 4-mA current on the positive input to the op-amp remains constant, the op-amp will provide a "high" output voltage, exceeding 13.5 V, with a typical level of 14.2 V (according to the specification sheets for the op-amp). However,

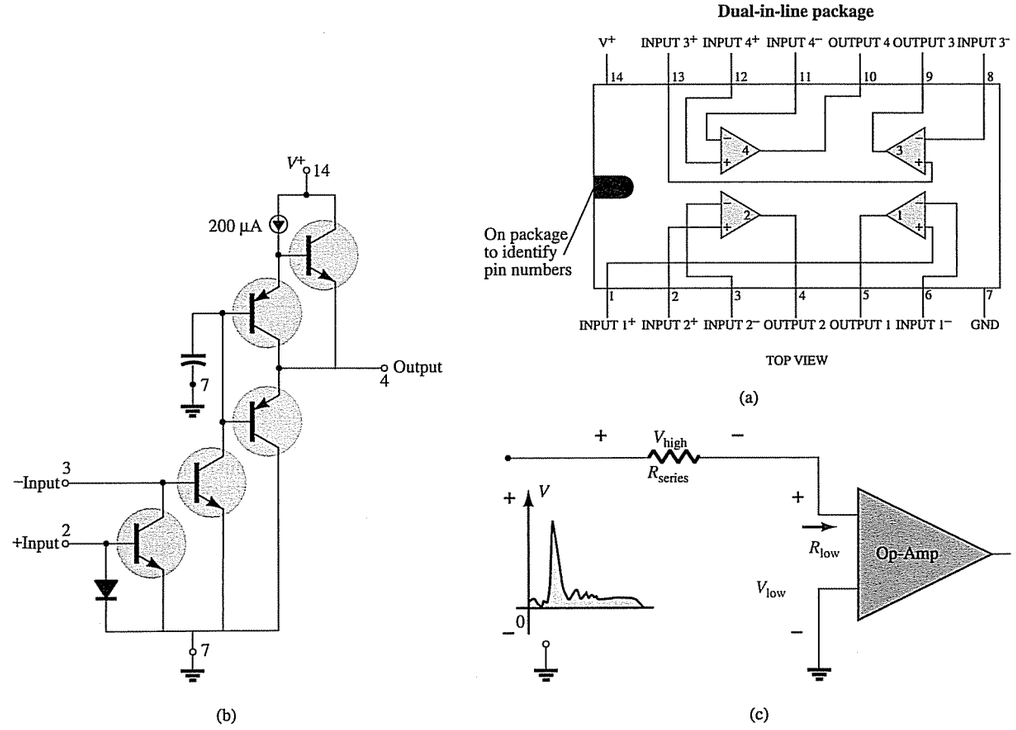


FIG. 4.75
LM2900 operational amplifier: (a) dual-in-line package (DIP); (b) components; (c) impact of low-input impedance.

if the sensor current drops from 4 mA to a level below 2 mA, the op-amp will respond with a "low" output voltage, typically about 0.1 V. The output of the op-amp will then signal the alarm circuit about the disturbance. Note from the above that it is not necessary for the sensor current to drop to all the way down to 0 mA to signal the alarm circuit. Only a variation around the reference level that appears unusual is required—a good alarm feature.

One very important characteristic of this particular op-amp is the low-input impedance as shown in Fig. 4.75c. This feature is important because one does not want alarm circuits reacting to every voltage spike or turbulence that comes down the line because of some external switching action or outside forces such as lightning. In Fig. 4.75c, for instance, if a high-voltage spike should appear at the input to the series configuration, most of the voltage will appear across the series resistor rather than the op-amp—thus preventing a false output and an activation of the alarm.

Logic Gates

By now it is probably a surprise to the reader that transistors in the dc mode are used for so many applications. For most students who have some prior awareness of transistors, the initial assumption is that a transistor is used only as an ac amplifier. In fact, most electronic components have a variety of applications in both the dc and the ac mode.

In this application, full use is made of the fact that the collector-to-emitter impedance of a transistor is quite low near or at saturation and large near or at cutoff. For instance, the load line defines *saturation* as the point where the current is quite high and the collector-to-emitter voltage quite low as shown in Fig. 4.76. The resulting resistance, defined by $R_{sat} = \frac{V_{CE_{sat}(low)}}{I_{C_{sat}(high)}}$, is quite low and is often approximated as a short circuit. At *cutoff*, the current is relatively low and the voltage near its maximum value as shown in Fig. 4.76, resulting in a very high impedance between the collector and emitter terminal, which is often approximated by an open circuit.

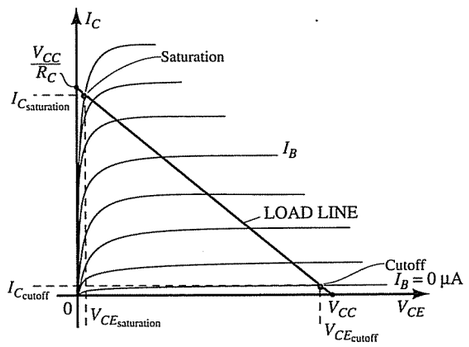
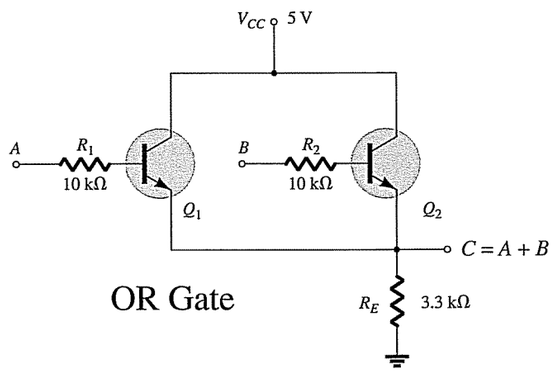


FIG. 4.76
Points of operation for a BJT logic gate.

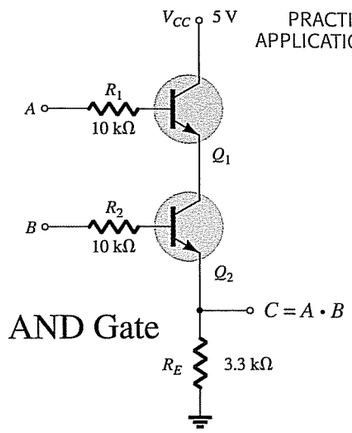
The above impedance levels established by "on" and "off" transistors make it relatively easy to understand the operation of the logic gates of Fig. 4.77. Because there are two inputs to each gate, there are four possible combinations of voltages at the input to the transistors. A 1, or "on," state is defined by a high voltage at the base terminal to turn the transistor on. A 0, or "off," state is defined by 0 V at the base, ensuring that transistor is off. If both *A* and *B* of the OR gate of Fig. 4.77a have a low or 0-V input, both transistors are off (cutoff), and the impedance between the collector and the emitter of each transistor can be approximated by an open circuit. Mentally replacing both transistors by open circuits between the collector and the emitter will remove any connection between the applied bias of 5 V and the output. The result is zero current through each transistor and through the 3.3-kΩ resistor. The output voltage is therefore 0 V, or "low"—a 0 state. On the other hand, if transistor Q_1 is on and Q_2 is off due to a positive voltage at the base of Q_1 and 0 V at the base of Q_2, then the short-circuit equivalent between the collector and



A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

1 = high
0 = low

(a)



A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

(b)

FIG. 4.77
BJT logic gates: (a) OR; (b) AND.

emitter for transistor Q_1 can be applied, and the voltage at the output is 5 V, or "high"—a 1 state. Finally, if both transistors are turned on by a positive voltage applied to the base of each, they will both ensure that the output voltage is 5 V, or "high"—a 1 state. The operation of the OR gate is properly defined: an output if either input terminal has applied turn-on voltage or if both are in the "on" state. A 0 state exists only if both do not have a 1 state at the input terminals.

The AND gate of Fig. 4.77b requires that the output be high only if both inputs have a turn-on voltage applied. If both are in the "on" state, a short-circuit equivalent can be used for the connection between the collector and the emitter of each transistor, providing a direct path from the applied 5-V source to the output—thereby establishing a high, or 1, state at the output terminal. If one or both transistors are off due to 0 V at the input terminal, an open circuit is placed in series with the path from the 5-V supply voltage to the output, and the output voltage is 0 V, or an "off" state.

Current Mirror

The current mirror is a dc network in which the current through the load is the mirror image of another current of the same network. If the controlling current of the network is changed, the current through the load will change also.

A common current mirror constructed of two back-to-back *npn* transistors is shown in Fig. 4.78. The load current is the collector current of Q_2, and the controlling current is the collector current of Q_1. Note, in particular, that the collector of Q_1 is connected directly to the base of the same transistor, establishing the same potential at each point. The result is that $V_{C_1} = V_{B_1} = V_{B_2} = 0.7$ V for the "on" transistor. The controlling element is resistor *R*. If you change its value, you change the controlling current as determined by $I_R = I_{C_1} = (10\text{ V} - 0.7\text{ V})/R$ (ignoring the drop-off in I_{C_1} due to I_B as shown in Fig. 4.78).

Once the resistance is set, the collector current of Q_2 will immediately change to the new level. The operation of the mirror network is totally dependent on the fact that Q_1 and

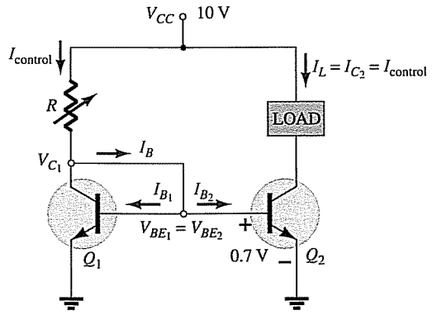


FIG. 4.78
Current mirror using back-to-back BJTs.

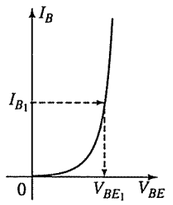


FIG. 4.79
Base characteristics for transistor Q_1 (and Q_2).

Q_2 are matched transistors, that is, transistors with very similar characteristics (ideally the same). In other words, a base current of 10 μA in either one will result in the same collector current for each; the base-to-emitter voltage of each in the "on" state will be the same; and so on.

The operation of the configuration is best defined by first setting the control current to the desired level, say I_{R_1}. This will define the level of I_{C_1} and of I_{B_1} from $I_{C_1}/\beta_1 = I_{R_1}/\beta_1$ and will establish the level of V_{BE_1} as shown in Fig. 4.79. Since they are matched transistors, $V_{BE_1} = V_{BE_2}$, and the resulting level of I_{B_2} will be same as I_{B_1}. The result is the same collector (load current) defined by $I_L = I_{C_2} = \beta_2 I_{B_2}$ since both betas are the same. In general, therefore, $I_L = I_{C_2} = I_{C_1} = I_R$ for matched transistors.

The network also has a measure of built-in control that will try to ensure that any variation in load current will be corrected by the configuration itself. For instance, if I_L should try to increase for whatever reason, the base current of Q_2 will also increase due to the relationship $I_{B_2} = I_{C_2}/\beta_2 = I_L/\beta_2$. Returning to Fig. 4.79, we find that an increase in I_{B_2} will cause voltage V_{BE_2} to increase also. Since the base of Q_2 is connected directly to the collector of Q_1, the voltage V_{CE_1} will increase also. This action causes the voltage across the control resistor R to decrease, causing I_R to drop. But if I_R drops, the base current I_B will drop, causing both I_{B_1} and I_{B_2} to drop also. A drop in I_{B_2} will cause the collector current and therefore the load current to drop also. The result, therefore, is a sensitivity to unwanted changes that the network will make every effort to correct.

The entire sequence of events just described can be presented on a single line as shown below. Note that at one end the load current is trying to increase, and at the end of the sequence the load current is forced to return to its original level.

$$I_L \uparrow I_{C_2} \uparrow I_{B_2} \uparrow V_{BE_2} \uparrow V_{CE_1} \downarrow, I_R \downarrow, I_B \downarrow, I_{B_2} \downarrow I_{C_2} \downarrow I_L \downarrow$$

Note

Voltage Level Indicator

The last application to be introduced in this section, the voltage level indicator, includes three of the elements introduced thus far: the transistor, the Zener diode, and the LED. The voltage level indicator is a relatively simple network using a green LED to indicate when the source voltage is close to its monitoring level of 9 V. In Fig. 4.80 the potentiometer is set to establish 5.4 V at the point indicated. The result is sufficient voltage to turn on both the 4.7-V Zener and the transistor and establish a collector current through the LED sufficient in magnitude to turn on the green LED.

Once the potentiometer is set, the LED will emit its green light as long as the supply voltage is near 9 V. However, if the terminal voltage of the 9-V battery should decrease, the voltage set up by the voltage-divider network may drop to 5 V from 5.4 V. At 5 V there is insufficient voltage to turn on both the Zener and the transistor, and the transistor will be in the "off" state. The LED will immediately turn off, revealing that the supply voltage has dropped below 9 V or that the power source has been disconnected.

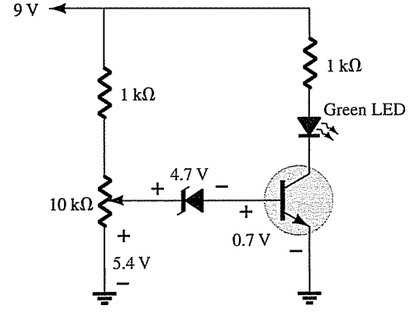


FIG. 4.80
Voltage level indicator.

4.14 SUMMARY

Important Conclusions and Concepts

1. No matter what type of configuration a transistor is used in, the basic relationships between the currents are **always the same**, and the base-to-emitter voltage is the **threshold value** if the transistor is in the "on" state.
2. The operating point defines where the transistor will operate on its characteristic curves under **dc conditions**. For linear (minimum distortion) amplification, the dc operating point should not be too close to the maximum power, voltage, or current rating and should avoid the regions of saturation and cutoff.
3. For most configurations the dc analysis begins with a determination of the **base current**.
4. For the dc analysis of a transistor network, all capacitors are replaced by an **open-circuit equivalent**.
5. The fixed-bias configuration is the simplest of transistor biasing arrangements, but it is also quite unstable due its **sensitivity to beta** at the operating point.
6. Determining the saturation (maximum) collector current for any configuration can usually be done quite easily if an **imaginary short circuit** is superimposed between the collector and emitter terminals of the transistor. The resulting current through the short is then the saturation current.
7. The equation for the load line of a transistor network can be found by applying **Kirchhoff's voltage law** to the output or collector network. The Q-point is then determined by finding the **intersection** between the base current and the load line drawn on the device characteristics.
8. The emitter-stabilized biasing arrangement is less sensitive to changes in beta—providing more stability for the network. Keep in mind, however, that any resistance in the emitter leg is "seen" at the base of the transistor as a much **larger resistor**, a fact that will reduce the base current of the configuration.
9. The voltage-divider bias configuration is probably the most common of all the configurations. Its popularity is due primarily to its **low sensitivity** to changes in beta from one transistor to another of the same lot (with the same transistor label). The exact analysis can be applied to any configuration, but the approximate one can be applied only if the reflected emitter resistance as seen at the base **is much larger** than the lower resistor of the voltage-divider bias arrangement connected to the base of the transistor.
10. When analyzing the dc bias with a voltage feedback configuration, be sure to remember that ***both*** the emitter resistor and the collector resistor are reflected back to the base circuit by beta. The least sensitivity to beta is obtained when the reflected resistance is much larger than the feedback resistor between the base and the collector.
11. For the common-base configuration the **emitter current is normally determined first** due to the presence of the base-to-emitter junction in the same loop. Then the fact that the emitter and the collector currents are essentially of the same magnitude is employed.

12. A clear understanding of the procedure employed to analyze a dc transistor network will usually permit a design of the same configuration with a minimum of difficulty and confusion. Simply start with those relationships that **minimize the number of unknowns** and then proceed to make some decisions about the unknown elements of the network.
13. In a switching configuration, a transistor quickly moves between **saturation and cutoff, or vice versa**. Essentially, the impedance between collector and emitter can be approximated as a short circuit for saturation and an open circuit for cutoff.
14. When checking the operation of a dc transistor network, first check that the base-to-emitter voltage is very close to **0.7 V** and that the collector-to-emitter voltage is between **25% and 75% of the applied voltage V_{CC}**.
15. The analysis of *pnp* configurations is exactly the same as that applied to *npn* transistors with the exception that current directions will **reverse** and voltages will have the **opposite** polarities.
16. Beta is very sensitive to **temperature**, and V_{BE} **decreases** about 2.5 mV (0.0025 V) for each 1° increase in temperature on a Celsius scale. The reverse saturation current typically **doubles** for every 10° increase in Celsius temperature.
17. Keep in mind that networks that are the **most stable** and least sensitive to temperature changes have the **smallest stability factors**.

Equations

$$V_{BE} = 0.7\text{ V}, \qquad I_E = (\beta + 1)I_B \cong I_C, \qquad I_C = \beta I_B$$

Fixed bias:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}, \qquad I_C = \beta I_B$$

Emitter stabilized:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}, \qquad R_i = (\beta + 1)R_E$$

Voltage-divider bias:

$$\textit{Exact:} \quad R_{\text{Th}} = R_1 \| R_2, \qquad E_{\text{Th}} = V_{R_2} = \frac{R_2 V_{CC}}{R_1 + R_2}, \qquad I_B = \frac{E_{\text{Th}} - V_{BE}}{R_{\text{Th}} + (\beta + 1)R_E}$$

$$\textit{Approximate:} \quad \textit{Test } \beta R_E \geq 10R_2$$

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2}, \qquad V_E = V_B - V_{BE}, \qquad I_E = \frac{V_E}{R_E} \cong I_C$$

DC bias with voltage feedback:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)}, \qquad I_C' \cong I_C \cong I_E$$

Common base:

$$I_E = \frac{V_{EE} - V_{BE}}{R_E}, \qquad I_C \cong I_E$$

Transistor switching networks:

$$I_{C_{\text{sat}}} = \frac{V_{CC}}{R_C}, \qquad I_B > \frac{I_{C_{\text{sat}}}}{\beta_{\text{dc}}}, \qquad R_{\text{sat}} = \frac{V_{CE_{\text{sat}}}}{I_{C_{\text{sat}}}}, \qquad t_{\text{on}} = t_r + t_d, \qquad t_{\text{off}} = t_s + t_f$$

Stability factors:

$$S(I_{CO}) = \frac{\Delta I_C}{\Delta I_{CO}}, \qquad S(V_{BE}) = \frac{\Delta I_C}{\Delta V_{BE}}, \qquad S(\beta) = \frac{\Delta I_C}{\Delta \beta}$$

$S(I_{CO})$:

$$\textit{Fixed bias:} \quad S(I_{CO}) = \beta + 1$$

$$\textit{Emitter bias:} \quad S(I_{CO}) = (\beta + 1)\frac{1 + R_B/R_E{}^*}{(\beta + 1) + R_B/R_E}$$

*Voltage-divider bias: Change R_B to R_{Th} in above equation.
*Feedback bias: Change R_E to R_C in above equation.

$S(V_{BE})$:

$$\textit{Fixed bias:} \quad S(V_{BE}) = -\frac{\beta}{R_B}$$

$$\textit{Emitter bias:} \quad S(V_{BE}) = \frac{-\beta^{\dagger}}{R_B + (\beta + 1)R_E}$$

†Voltage-divider bias: Change R_B to R_{Th} in above equation.
†Feedback bias: Change R_E to R_C in above equation.

$S(\beta)$:

$$\textit{Fixed bias:} \quad S(\beta) = \frac{I_{C_1}}{\beta_1}$$

$$\textit{Emitter bias:} \quad S(\beta) = \frac{I_{C_1}(1 + R_B/R_E)^{\ddagger}}{\beta_1(1 + \beta_2 + R_B/R_E)}$$

‡Voltage-divider bias: Change R_B to R_{Th} in above equation.
‡Feedback bias: Change R_E to R_C in above equation.

4.15 COMPUTER ANALYSIS

PSpice Windows

Voltage-Divider Configuration The results of Example 4.7 will now be verified using PSpice Windows. Using methods described in detail in the previous chapters, we can construct the network of Fig. 4.81. Recall from the previous chapter that the transistor is found under the **EVAL** library, the dc source under the **SOURCE** library, and the resistor under the **ANALOG** library. The capacitor has not been called up earlier but can also be found in the **ANALOG** library. For the transistor, the list of available transistors can be found in the **Place Part** dialog box by simply typing **transistor** in the space provided under **Part**.

The value of beta is changed to 140 to match Example 4.7 by first clicking on the transistor symbol on the screen. It will then appear boxed in red to reveal it is in an active status. Then proceed with **Edit-PSpice Model**, and the **PSpice Model Editor Lite** dialog box

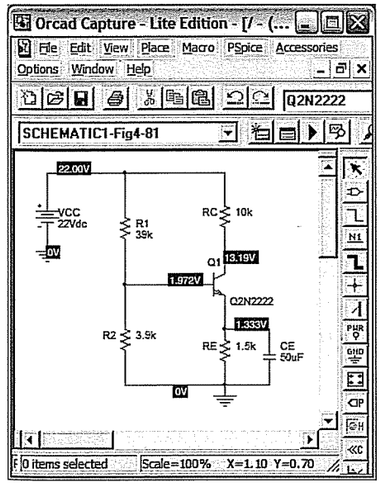


FIG. 4.81
Applying PSpice Windows to the voltage-divider configuration of Example 4.7.

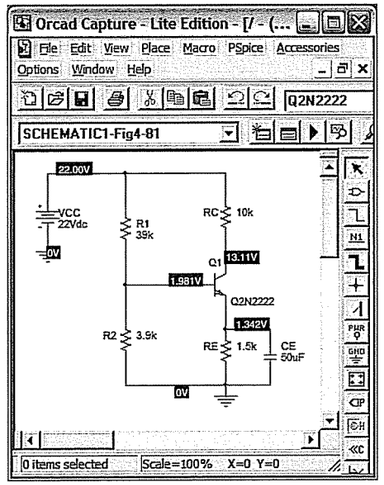


FIG. 4.82
Response obtained after changing β from 140 to 255.9 for the network of Fig. 4.81.

will appear in which **Bf** can be changed to **100**. As you try to leave the dialog box the **Model Editor/9.2** dialog box will appear asking if you want to save the changes in the network library. Once they are saved, the screen will automatically return with beta set at its new value.

The analysis can then proceed by selecting the **Create a new simulation profile** key (looks like a printout with an asterisk in the top left corner) to obtain the **New Simulation** dialog box. Insert Fig. 4.81 and select **Create**. The **Simulation Settings** dialog box will appear in which **Bias Point** is selected under the **Analysis Type** heading. An **OK**, and the system is ready for simulation.

Proceed by selecting the **Run PSpice** key (blue arrow) or the sequence **PSpice–Run**. The bias voltages will appear as shown in Fig. 4.81 if the **V** option selected. The collector-to-emitter voltage is 13.19 V − 1.333 V = 11.857 V versus 12.22 V of Example 4.7. The difference is primarily due to the fact that we are using an actual transistor whose parameters are very sensitive to the operating conditions. Also recall the difference in beta from the specification value and the value obtained from the plot of the previous chapter.

Since the voltage-divider network has a low sensitivity to changes in beta, let us return to the transistor specifications and replace beta by the default value of 255.9 and see how the results change. The result is the printout of Fig. 4.82, with voltage levels very close to those obtained in Fig. 4.81.

Note the distinct advantage of having the network set up in memory. Any parameter can now be changed and a new solution obtained almost instantaneously—a wonderful advantage in the design process.

Fixed-Bias Configuration Although the voltage-divider bias network is relatively insensitive to changes in the beta value, the fixed-bias configuration is very sensitive to beta variations. This can be demonstrated by setting up the fixed-bias configuration of Example 4.1 using a beta of 50 for the first run. The results of Fig. 4.83 demonstrate that the design is a fairly good one. The collector or collector-to-emitter voltage is appropriate for the applied source. The resulting base and collector currents are fairly common for a good design.

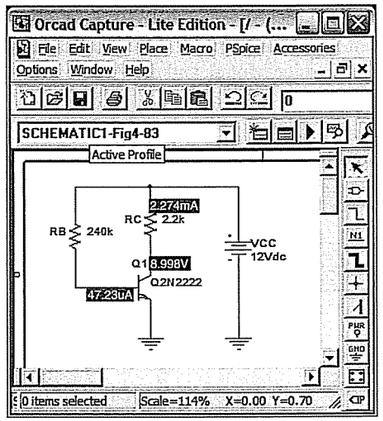


FIG. 4.83
Fixed-bias configuration with a β of 50.

However, if we now go back to the transistor specifications and change beta back to the default value of 255.9, we obtain the results of Fig. 4.84. The collector voltage is now only 0.113 V at a current of 5.4 mA—a terrible operating point. Any applied ac signal would be severely truncated due to the low collector voltage.

Clearly, therefore, from the above analysis, the voltage-divider configuration is the preferred design if there is any concern about beta variations.

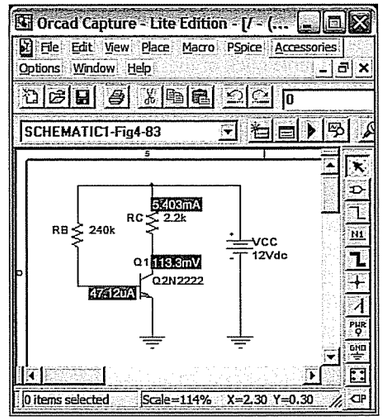


FIG. 4.84
Network of Fig. 4.83 with a β of 255.9.

Multisim

Multisim will now be applied to the fixed-bias network of Example 4.4 to provide an opportunity to review the transistor options internal to the software package and to compare results with the handwritten approximate solution.

All the components of Fig. 4.85 except the transistor can be entered using the procedure described in Chapter 2. Transistors are available through the **Transistor** key pad, which is the fourth option down on the first vertical toolbar. When it is selected, the **Select a Component** dialog box will appear, from which **BJT_NPN** is chosen. The result is a **Component**

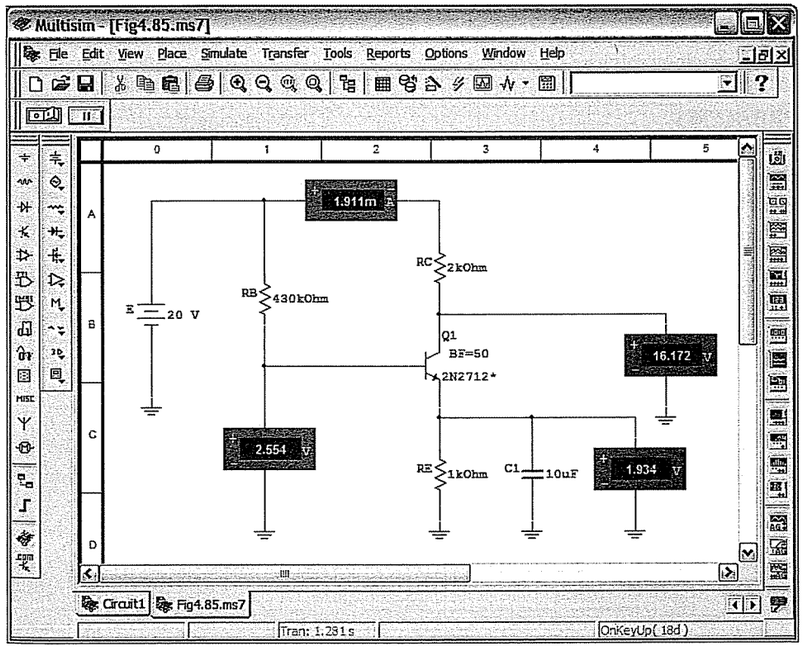


FIG. 4.85
Verifying the results of Example 4.4 using Multisim.

list, from which **2N2712** can be selected. An **OK**, and the transistor will appear on the screen with the labels **Q1** and **2N2712**. The label **Bf = 50** can be added by first selecting **Place** in the top toolbar followed by a double click of the **Text** option. The result is a blinking vertical line to mark the point where the text can be entered. When this is finished, a second double-click, and the label is set. To move the label to the position shown in Fig. 4.85, simply click on the label to place the four small squares around the device. Then click it once more and drag it to the desired position. Release the clicker, and it is in place. Another click, and the four small markers will disappear.

Even though the label may say **Bf = 50**, the transistor will still have the default parameters stored in memory. To change the parameters, the first step is to click on the device to place the four markers that mark its boundaries. Then select **Edit**, followed by **Properties**, to obtain the **BJT_NPN** dialog box. If it is not already present, select **Value** and then **Edit Model**. The result will be the **Edit Model** dialog box in which β and I_s can be set to 50 and 1 nA, respectively. Then choose **Change Part Model** to obtain the **BJT_NPN** dialog box again and select **OK**. The transistor symbol on the screen will now have an asterisk to indicate that the default parameters have been modified. One more click to remove the four markers, and the transistor is set with its new parameters.

The ammeter in the network is set by selecting the Indicator option (the 10th keypad down on the first vertical tool bar) to obtain the **Select a Component** dialog box. Under **Family**, **AMMETER** is selected, and under **Component**, **AMMETER H** is chosen. An **OK**, and it will appear on the screen with additional labels. The labels can be removed through the sequence **Edit-Properties-Display**. If all the checks are removed, an **OK** and one more click will result in the appearance for the ammeter appearing in Fig. 4.85. For the voltmeters the option **VOLTMETER V** is chosen.

Finally, the network must be simulated using one of the methods described in Chapter 2. For this example the switch was set to the **1** position and then back to the **0** position after the Indicator values stabilized. In particular, note that the base-to-emitter voltage is 2.554 V − 1.934 V = 0.62 V rather than the 0.7 V assumed in the handwritten analysis. The relatively low levels of current were partially responsible for the low level of this voltage. However, in general, both of the readings are a confirmation of the solutions of Example 4.4 using Multisim.

The relatively few comments required here to permit the analysis of transistor networks is a clear indication that the breadth of analysis using Multisim can be expanded dramatically without having to learn a whole new set of rules—a very welcome characteristic of most technology software packages.

PROBLEMS

*Note: Asterisks indicate more difficult problems.

4.3 Fixed-Bias Circuit

1. For the fixed-bias configuration of Fig. 4.86, determine:
   a. I_{B_Q}.
   b. I_{C_Q}.
   c. V_{CE_Q}.
   d. V_C.
   e. V_B.
   f. V_E.

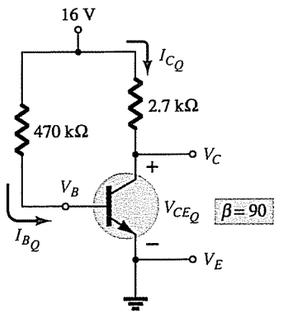


FIG. 4.86
Problems 1, 4, 11, 47, and 51 through 53.

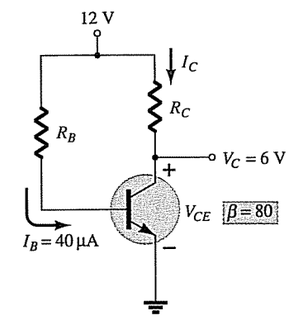


FIG. 4.87
Problem 2.

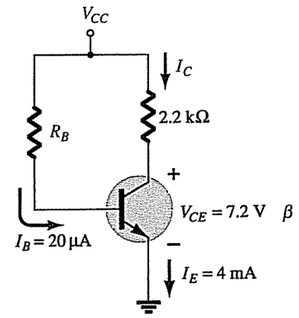


FIG. 4.88
Problem 3.

2. Given the information appearing in Fig. 4.87, determine:
   a. I_C.
   b. R_C.
   c. R_B.
   d. V_{CE}.
3. Given the information appearing in Fig. 4.88, determine:
   a. I_C.
   b. V_{CC}.
   c. β.
   d. R_B.
4. Find the saturation current ($I_{C_{sat}}$) for the fixed-bias configuration of Fig. 4.86.

*5. Given the BJT transistor characteristics of Fig. 4.89:
   a. Draw a load line on the characteristics determined by $E = 21$ V and $R_C = 3\,\text{k}\Omega$ for a fixed-bias configuration.
   b. Choose an operating point midway between cutoff and saturation. Determine the value of R_B to establish the resulting operating point.
   c. What are the resulting values of I_{C_Q} and V_{CE_Q}?
   d. What is the value of β at the operating point?

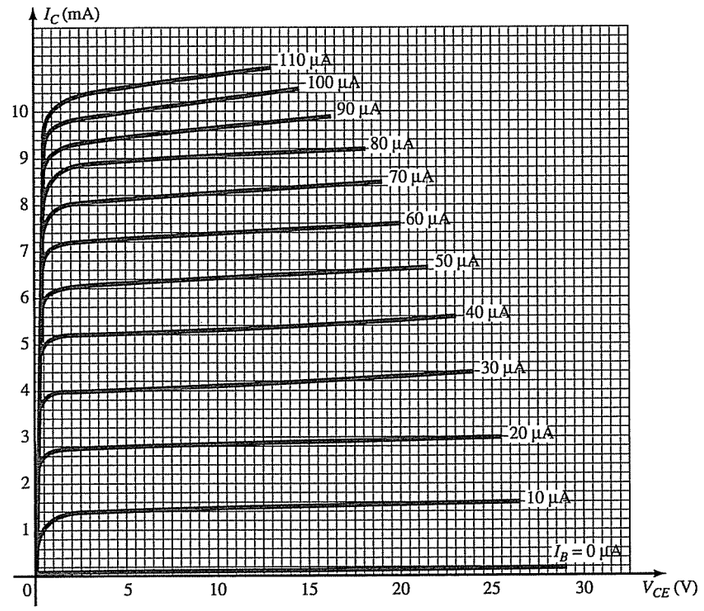


FIG. 4.89
Problems 5, 10, 19, 35, and 36.

e. What is the value of α defined by the operating point?
f. What is the saturation current ($I_{C_{sat}}$) for the design?
g. Sketch the resulting fixed-bias configuration.
h. What is the dc power dissipated by the device at the operating point?
i. What is the power supplied by V_{CC}?
j. Determine the power dissipated by the resistive elements by taking the difference between the results of parts (h) and (i).

4.4 Emitter Bias

6. For the emitter-stabilized bias circuit of Fig. 4.90, determine:
   a. I_{B_Q}.
   b. I_{C_Q}.
   c. V_{CE_Q}.
   d. V_C.
   e. V_B.
   f. V_E.
7. Given the information provided in Fig. 4.91, determine:
   a. R_C.
   b. R_E.
   c. R_B.
   d. V_{CE}.
   e. V_B.

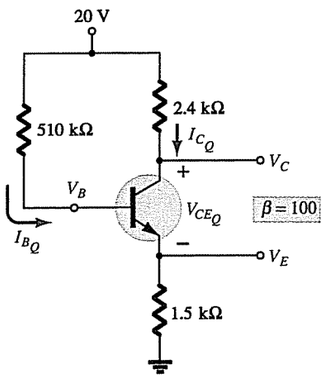


FIG. 4.90
Problems 6, 9, 11, 48, 51, and 54.

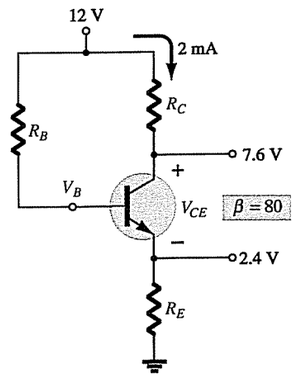


FIG. 4.91
Problem 7.

8. Given the information provided in Fig. 4.92, determine:
   a. β.
   b. V_{CC}.
   c. R_B.

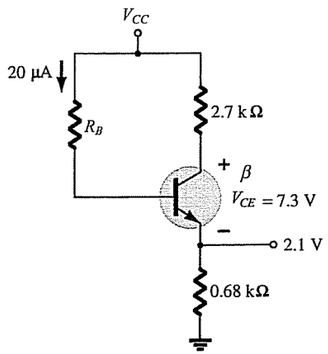


FIG. 4.92
Problem 8.

9. Determine the saturation current ($I_{C_{sat}}$) for the network of Fig. 4.90.

*10. Using the characteristics of Fig. 4.89, determine the following for an emitter-bias configuration if a Q-point is defined at $I_{C_Q} = 4\,\text{mA}$ and $V_{CE_Q} = 10\,\text{V}$.
   a. R_C if $V_{CC} = 24\,\text{V}$ and $R_E = 1.2\,\text{k}\Omega$.
   b. β at the operating point.
   c. R_B.
   d. Power dissipated by the transistor.
   e. Power dissipated by the resistor R_C.

*11. a. Determine I_C and V_{CE} for the network of Fig. 4.86.
   b. Change β to 135 and determine the new value of I_C and V_{CE} for the network of Fig. 4.86.
   c. Determine the magnitude of the percentage change in I_C and V_{CE} using the following equations:

$$\%\Delta I_C = \left|\frac{I_{C_{(\text{part b})}} - I_{C_{(\text{part a})}}}{I_{C_{(\text{part a})}}}\right| \times 100\%, \qquad \%\Delta V_{CE} = \left|\frac{V_{CE_{(\text{part b})}} - V_{CE_{(\text{part a})}}}{V_{CE_{(\text{part a})}}}\right| \times 100\%$$

   d. Determine I_C and V_{CE} for the network of Fig. 4.90.
   e. Change β to 150 and determine the new value of I_C and V_{CE} for the network of Fig. 4.90.
   f. Determine the magnitude of the percentage change in I_C and V_{CE} using the following equations:

$$\%\Delta I_C = \left|\frac{I_{C_{(\text{part c})}} - I_{C_{(\text{part d})}}}{I_{C_{(\text{part d})}}}\right| \times 100\%, \qquad \%\Delta V_{CE} = \left|\frac{V_{CE_{(\text{part c})}} - V_{CE_{(\text{part d})}}}{V_{CE_{(\text{part d})}}}\right| \times 100\%$$

   g. In each of the above, the magnitude of β was increased 50%. Compare the percentage change in I_C and V_{CE} for each configuration, and comment on which seems to be less sensitive to changes in β.

4.5 Voltage-Divider Bias

12. For the voltage-divider bias configuration of Fig. 4.93, determine:
   a. I_{B_Q}.
   b. I_{C_Q}.
   c. V_{CE_Q}.
   d. V_C.
   e. V_E.
   f. V_B.
13. Given the information provided in Fig. 4.94, determine:
   a. I_C.
   b. V_E.
   c. V_B.
   d. R_1.

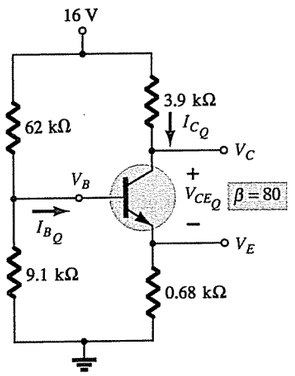


FIG. 4.93
Problems 12, 15, 18, 20, 24, 49, 51, 52, and 55.

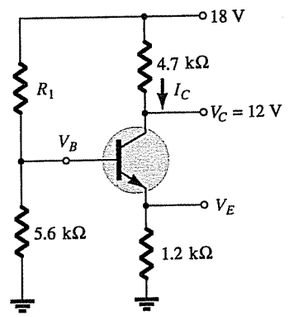


FIG. 4.94
Problem 13.

14. Given the information appearing in Fig. 4.95, determine:
    a. I_C.
    b. V_E.
    c. V_{CC}.
    d. V_{CE}.
    e. V_B.
    f. R_1.

15. Determine the saturation current ($I_{C_{sat}}$) for the network of Fig. 4.93.

*16. Determine the following for the voltage-divider configuration of Fig. 4.96 using the approximate approach if the condition established by Eq. (4.33) is satisfied.
    a. I_C.
    b. V_{CE}.
    c. I_B.
    d. V_E.
    e. V_B.

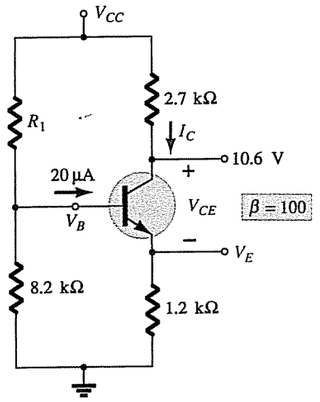


FIG. 4.95
Problem 14.

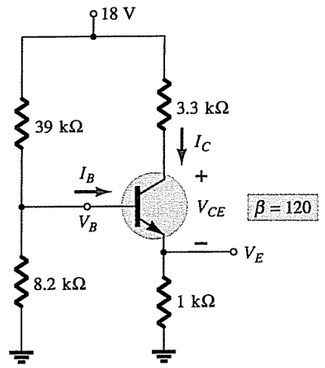


FIG. 4.96
Problems 16, 17, and 21.

*17. Repeat Problem 16 using the exact (Thévenin) approach and compare solutions. Based on the results, is the approximate approach a valid analysis technique if Eq. (4.33) is satisfied?

18. a. Determine I_{C_Q}, V_{CE_Q}, and I_{B_Q} for the network of Problem 12 (Fig. 4.93) using the approximate approach even though the condition established by Eq. (4.33) is not satisfied.
    b. Determine I_{C_Q}, V_{CE_Q}, and I_{B_Q} using the exact approach.
    c. Compare solutions and comment on whether the difference is sufficiently large to require standing by Eq. (4.33) when determining which approach to employ.

*19. a. Using the characteristics of Fig. 4.89, determine R_C and R_E for a voltage-divider network having a Q-point of $I_{C_Q} = 5$ mA and $V_{CE_Q} = 8$ V. Use $V_{CC} = 24$ V and $R_C = 3R_E$.
    b. Find V_E.
    c. Determine V_B.
    d. Find R_2 if $R_1 = 24\,\text{k}\Omega$ assuming that $\beta R_E > 10R_2$.
    e. Calculate β at the Q-point.
    f. Test Eq. (4.33), and note whether the assumption of part (d) is correct.

*20. a. Determine I_C and V_{CE} for the network of Fig. 4.93.
    b. Change β to 120 (50% increase), and determine the new values of I_C and V_{CE} for the network of Fig. 4.93.
    c. Determine the magnitude of the percentage change in I_C and V_{CE} using the following equations:

$$\%\Delta I_C = \left|\frac{I_{C(\text{part b})} - I_{C(\text{part a})}}{I_{C(\text{part a})}}\right| \times 100\%, \qquad \%\Delta V_{CE} = \left|\frac{V_{CE(\text{part b})} - V_{CE(\text{part a})}}{V_{CE(\text{part a})}}\right| \times 100\%$$

    d. Compare the solution to part (c) with the solutions obtained for parts (c) and (f) of Problem 11. If not performed, note the solutions provided in Appendix E.
    e. Based on the results of part (d), which configuration is least sensitive to variations in β?

*21. a. Repeat parts (a) through (e) of Problem 20 for the network of Fig. 4.96. Change β to 180 in part (b).
    b. What general conclusions can be made about networks in which the condition $\beta R_E > 10R_2$ is satisfied and the quantities I_C and V_{CE} are to be determined in response to a change in β?

4.6 DC Bias with Voltage Feedback

22. For the collector feedback configuration of Fig. 4.97, determine:
    a. I_B.
    b. I_C.
    c. V_C.

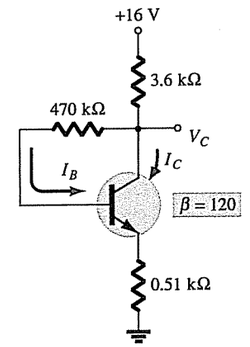


FIG. 4.97
Problems 22 and 56.

23. For the voltage feedback network of Fig. 4.98, determine:
    a. I_C.
    b. V_C.
    c. V_E.
    d. V_{CE}.

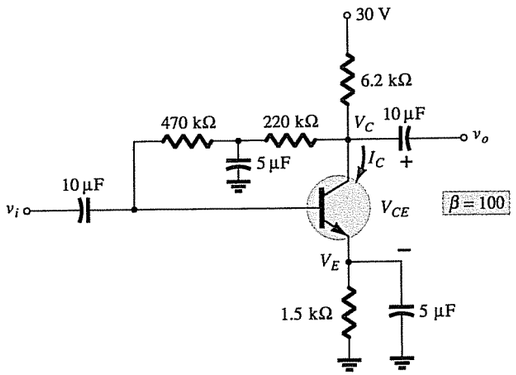


FIG. 4.98
Problem 23.

*24. a. Determine the levels of I_C and V_{CE} for the network of Fig. 4.99.
    b. Change β to 135 (50% increase), and calculate the new levels of I_C and V_{CE}.

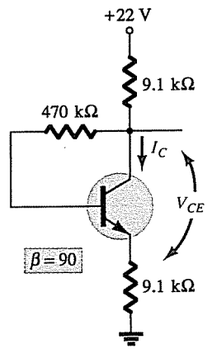


FIG. 4.99
Problem 24.

c. Determine the magnitude of the percentage change in I_C and V_{CE} using the following equations:

$$\%\Delta I_C = \left|\frac{I_{C(\text{part b})} - I_{C(\text{part a})}}{I_{C(\text{part a})}}\right| \times 100\%, \qquad \%\Delta V_{CE} = \left|\frac{V_{CE(\text{part b})} - V_{CE(\text{part a})}}{V_{CE(\text{part a})}}\right| \times 100\%$$

d. Compare the results of part (c) with those of Problems 11(c), 11(f), and 20(c). How does the collector-feedback network stack up against the other configurations in sensitivity to changes in β?

25. Determine the range of possible values for V_C for the network of Fig. 4.100 using the 1-MΩ potentiometer.

***26.** Given $V_B = 4$ V for the network of Fig. 4.101, determine:

a. V_E.
b. I_C.
c. V_C.
d. V_{CE}.
e. I_B.
f. β.

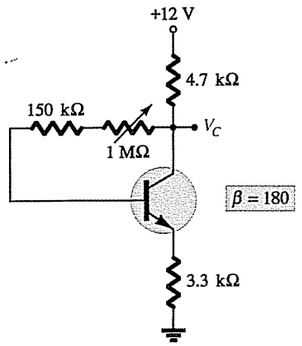


FIG. 4.100
Problem 25.

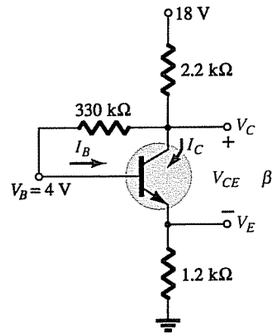


FIG. 4.101
Problem 26.

4.7 Miscellaneous Bias Configurations

27. Given $V_C = 8$ V for the network of Fig. 4.102, determine:

a. I_B.
b. I_C.
c. β.
d. V_{CE}.

***28.** For the network of Fig. 4.103, determine:

a. I_B.
b. I_C.
c. V_{CE}.
d. V_C.

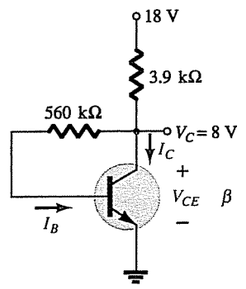


FIG. 4.102
Problem 27.

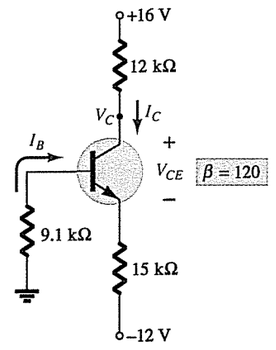


FIG. 4.103
Problem 28.

***29.** For the network of Fig. 4.104, determine:

a. I_B.
b. I_C.
c. V_E.
d. V_{CE}.

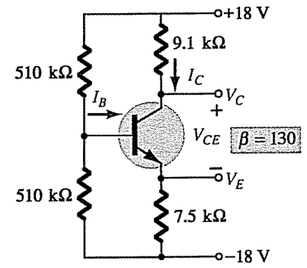


FIG. 4.104
Problem 29.

***30.** Determine the level of V_E and I_E for the network of Fig. 4.105.

***31.** For the network of Fig. 4.106, determine:

a. I_E.
b. V_C.
c. V_{CE}.

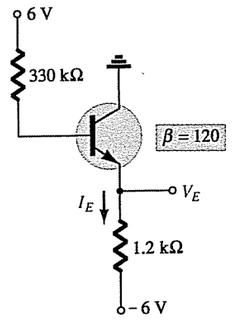


FIG. 4.105
Problem 30.

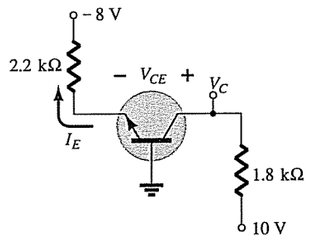


FIG. 4.106
Problem 31.

4.8 Design Operations

32. Determine R_C and R_B for a fixed-bias configuration if $V_{CC} = 12$ V, $\beta = 80$, and $I_{C_Q} = 2.5$ mA with $V_{CE_Q} = 6$ V. Use standard values.

33. Design an emitter-stabilized network at $I_{C_Q} = \frac{1}{2}I_{C_{sat}}$ and $V_{CE_Q} = \frac{1}{2}V_{CC}$. Use $V_{CC} = 20$ V, $I_{C_{sat}} = 10$ mA, $\beta = 120$, and $R_C = 4R_E$. Use standard values.

34. Design a voltage-divider bias network using a supply of 24 V, a transistor with a beta of 110, and an operating point of $I_{C_Q} = 4$ mA and $V_{CE_Q} = 8$ V. Choose $V_E = \frac{1}{8}V_{CC}$. Use standard values.

***35.** Using the characteristics of Fig. 4.89, design a voltage-divider configuration to have a saturation level of 10 mA and a Q-point one-half the distance between cutoff and saturation. The available supply is 28 V, and V_E is to be one-fifth of V_{CC}. The condition established by Eq. (4.33) should also be met to provide a high stability factor. Use standard values.

4.9 Transistor Switching Networks

***36.** Using the characteristics of Fig. 4.89, determine the appearance of the output waveform for the network of Fig. 4.107. Include the effects of $V_{CE_{sat}}$, and determine I_B, $I_{B_{max}}$, and $I_{C_{sat}}$ when $V_i = 10$ V. Determine the collector-to-emitter resistance at saturation and cutoff.

***37.** Design the transistor inverter of Fig. 4.108 to operate with a saturation current of 8 mA using a transistor with a beta of 100. Use a level of I_B equal to 120% of $I_{B_{max}}$ and standard resistor values.

38. a. Using the characteristics of Fig. 3.23c, determine t_{on} and t_{off} at a current of 2 mA. Note the use of log scales and the possible need to refer to Section 9.2.
b. Repeat part (a) at a current of 10 mA. How have t_{on} and t_{off} changed with increase in collector current?
c. For parts (a) and (b), sketch the pulse waveform of Fig. 4.57 and compare results.

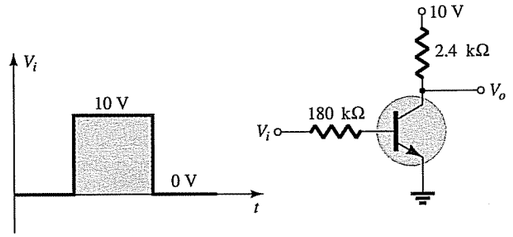


FIG. 4.107
Problem 36.

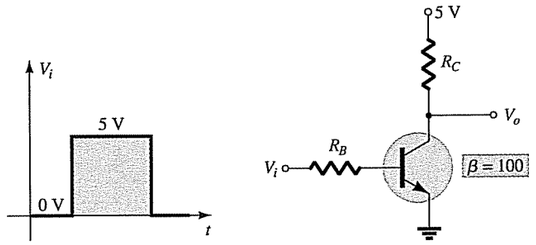


FIG. 4.108
Problem 37.

4.10 Troubleshooting Techniques

***39.** The measurements of Fig. 4.109 all reveal that the network is not functioning correctly. List as many reasons as you can for the measurements obtained.

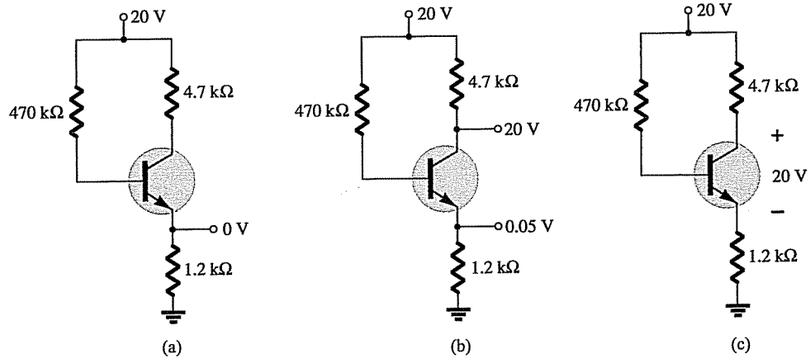


FIG. 4.109
Problem 39.

***40.** The measurements appearing in Fig. 4.110 reveal that the networks are not operating properly. Be specific in describing why the levels obtained reflect a problem with the expected network behavior. In other words, the levels obtained reflect a very specific problem in each case.

41. For the circuit of Fig. 4.111:
- **a.** Does V_C increase or decrease if R_B is increased?
- **b.** Does I_C increase or decrease if β is reduced?
- **c.** What happens to the saturation current if β is increased?
- **d.** Does the collector current increase or decrease if V_{CC} is reduced?
- **e.** What happens to V_{CE} if the transistor is replaced by one with smaller β?

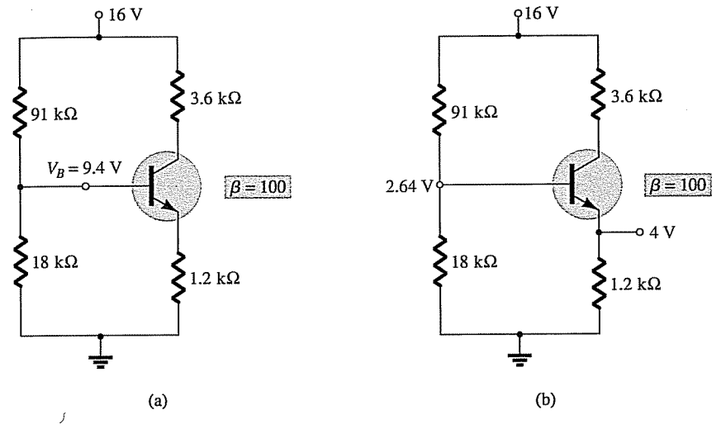


FIG. 4.110
Problem 40.

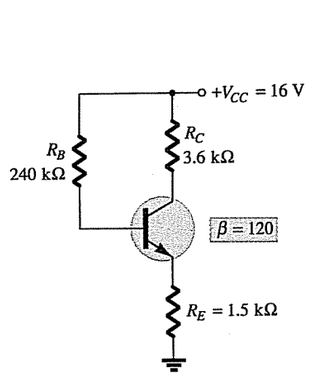


FIG. 4.111
Problem 41.

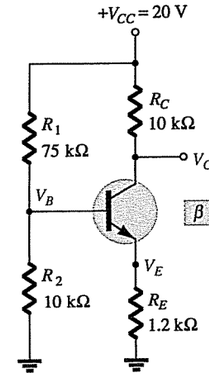


FIG. 4.112
Problem 42.

42. Answer the following questions about the circuit of Fig. 4.112:
- **a.** What happens to the voltage V_C if the transistor is replaced by one having a larger value of β?
- **b.** What happens to the voltage V_{CE} if the ground leg of resistor R_{B_2} opens (does not connect to ground)?
- **c.** What happens to I_C if the supply voltage is low?
- **d.** What voltage V_{CE} would occur if the transistor base–emitter junction fails by becoming open?
- **e.** What voltage V_{CE} would result if the transistor base–emitter junction fails by becoming a short?

***43.** Answer the following questions about the circuit of Fig. 4.113:
- **a.** What happens to the voltage V_C if the resistor R_B is open?
- **b.** What should happen to V_{CE} if β increases due to temperature?
- **c.** How will V_E be affected when replacing the collector resistor with one whose resistance is at the lower end of the tolerance range?
- **d.** If the transistor collector connection becomes open, what will happen to V_E?
- **e.** What might cause V_{CE} to become nearly 18 V?

4.11 *pnp* Transistors

44. Determine V_C, V_{CE}, and I_C for the network of Fig. 4.114.

45. Determine V_C and I_B for the network of Fig. 4.115.

46. Determine I_E and V_C for the network of Fig. 4.116.

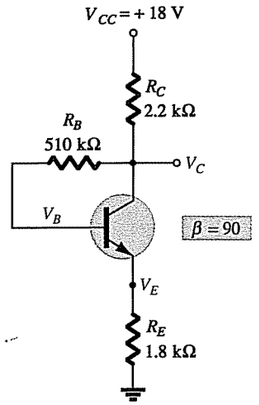


FIG. 4.113
Problem 43.

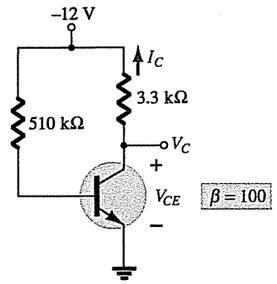


FIG. 4.114
Problem 44.

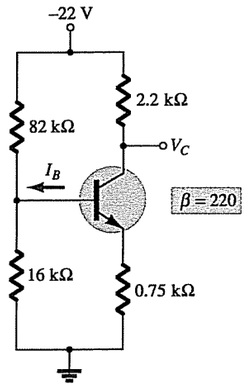


FIG. 4.115
Problem 45.

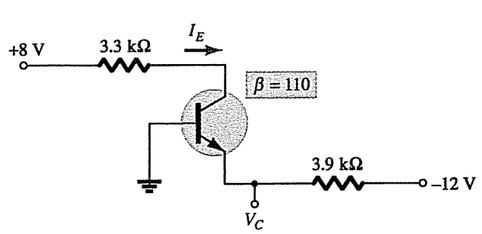


FIG. 4.116
Problem 46.

4.12 Bias Stabilization

47. Determine the following for the network of Fig. 4.86:
- **a.** $S(I_{CO})$.
- **b.** $S(V_{BE})$.
- **c.** $S(\beta)$, using T_1 as the temperature at which the parameter values are specified and $\beta(T_2)$ as 25% more than $\beta(T_1)$.
- **d.** Determine the net change in I_C if a change in operating conditions results in I_{CO} increasing from 0.2 μA to 10 μA, V_{BE} drops from 0.7 V to 0.5 V, and β increases 25%.

***48.** For the network of Fig. 4.90, determine:
- **a.** $S(I_{CO})$.
- **b.** $S(V_{BE})$.
- **c.** $S(\beta)$, using T_1 as the temperature at which the parameter values are specified and $\beta(T_2)$ as 25% more than $\beta(T_1)$.
- **d.** Determine the net change in I_C if a change in operating conditions results in I_{CO} increasing from 0.2 μA to 10 μA, V_{BE} drops from 0.7 V to 0.5 V, and β increases 25%.

***49.** For the network of Fig. 4.93, determine:
- **a.** $S(I_{CO})$.
- **b.** $S(V_{BE})$.
- **c.** $S(\beta)$, using T_1 as the temperature at which the parameter values are specified and $\beta(T_2)$ as 25% more than $\beta(T_1)$.
- **d.** Determine the net change in I_C if a change in operating conditions results in I_{CO} increasing from 0.2 μA to 10 μA, V_{BE} drops from 0.7 V to 0.5 V, and β increases 25%.

***50.** For the network of Fig. 4.102, determine:
- **a.** $S(I_{CO})$.
- **b.** $S(V_{BE})$.
- **c.** $S(\beta)$, using T_1 as the temperature at which the parameter values are specified and $\beta(T_2)$ as 25% more than $\beta(T_1)$.
- **d.** Determine the net change in I_C if a change in operating conditions results in I_{CO} increasing from 0.2 μA to 10 μA, V_{BE} drops from 0.7 V to 0.5 V, and β increases 25%.

***51.** Compare the relative values of stability for Problems 47 through 50. The results for Exercises 47 and 49 can be found in Appendix E. Can any general conclusions be derived from the results?

***52.**
- **a.** Compare the levels of stability for the fixed-bias configuration of Problem 47.
- **b.** Compare the levels of stability for the voltage-divider configuration of Problem 49.
- **c.** Which factors of parts (a) and (b) seem to have the most influence on the stability of the system, or is there no general pattern to the results?

4.15 Computer Analysis

53. Perform a PSpice analysis of the network of Fig. 4.86. That is, determine I_C, V_{CE}, and I_B.

54. Repeat Problem 53 for the network of Fig. 4.90.

55. Repeat Problem 53 for the network of Fig. 4.93.

56. Repeat Problem 53 for the network of Fig. 4.97.

57. Repeat Problem 53 using Multisim.

58. Repeat Problem 54 using Multisim.

59. Repeat Problem 55 using Multisim.

60. Repeat Problem 56 using Multisim.

5 BJT AC Analysis

CHAPTER OUTLINE

5.1 Introduction
5.2 Amplification in the AC Domain
5.3 BJT Transistor Modeling
5.4 The r_e Transistor Model
5.5 The Hybrid Equivalent Model
5.6 Hybrid π Model
5.7 Variations of Transistor Parameters
5.8 Common-Emitter Fixed-Bias Configuration
5.9 Voltage-Divider Bias
5.10 CE Emitter-Bias Configuration
5.11 Emitter-Follower Configuration
5.12 Common-Base Configuration
5.13 Collector Feedback Configuration
5.14 Collector DC Feedback Configuration
5.15 Determining the Current Gain
5.16 Effect of R_L and R_s
5.17 Two-Port Systems Approach
5.18 Summary Table
5.19 Cascaded Systems
5.20 Darlington Connection
5.21 Feedback Pair
5.22 Current Mirror Circuits
5.23 Current Source Circuits
5.24 Approximate Hybrid Equivalent Circuit
5.25 Complete Hybrid Equivalent Model
5.26 Troubleshooting
5.27 Practical Applications
5.28 Summary
5.29 Computer Analysis

5.1 INTRODUCTION

The basic construction, appearance, and characteristics of the transistor were introduced in Chapter 3. The dc biasing of the device was then examined in detail in Chapter 4. We now begin to examine the ac response of the BJT amplifier by reviewing the *models* most frequently used to represent the transistor in the sinusoidal ac domain.

One of our first concerns in the sinusoidal ac analysis of transistor networks is the magnitude of the input signal. It will determine whether *small-signal* or *large-signal* techniques should be applied. There is no set dividing line between the two, but the application—and the magnitude of the variables of interest relative to the scales of the device characteristics—will usually make it quite clear which method is appropriate. The small-signal technique is introduced in this chapter, and large-signal applications are examined in Chapter 12.

There are three models commonly used in the small-signal ac analysis of transistor networks: the r_e model, the hybrid π model, and the *hybrid equivalent* model. This chapter introduces all three but emphasizes the r_e model.

5.2 AMPLIFICATION IN THE AC DOMAIN

It was demonstrated in Chapter 3 that the transistor can be employed as an amplifying device. That is, the output sinusoidal signal is greater than the input signal, or, stated another way, the output ac power is greater than the input ac power. The question then arises as to how the ac power output can be greater than the input ac power. Conservation of energy dictates that over time the total power output, P_o, of a system cannot be greater than its power input, P_i, and that the efficiency defined by $\eta = P_o/P_i$ cannot be greater than 1. The factor missing from the discussion above that permits an ac power output greater than the input ac power is the applied dc power. It is a contributor to the total output power even though part of it is dissipated by the device and resistive elements. In other words, there is an "exchange" of dc power to the ac domain that permits establishing a higher output ac power. In fact, a *conversion efficiency* is defined by $\eta = P_{o(\text{ac})}/P_{i(\text{dc})}$, where $P_{o(\text{ac})}$ is the ac power to the load and $P_{i(\text{dc})}$ is the dc power supplied.

Perhaps the role of the dc supply can best be described by first considering the simple dc network of Fig. 5.1. The resulting direction of flow is indicated in the figure with a plot of the current i versus time. Let us now insert a control mechanism such as that shown in Fig. 5.2. The control mechanism is such that the application of a relatively small signal to the control mechanism can result in a substantial oscillation in the output circuit.

That is, for this example,

$$i_{\text{ac(p-p)}} \gg i_{c\text{(p-p)}}$$

and amplification in the ac domain has been established. The peak-to-peak value of the output current far exceeds that of the control current.

For the system of Fig. 5.2, the peak value of the oscillation in the output circuit is controlled by the established dc level. Any attempt to exceed the limit set by the dc level will result in a "clipping" (flattening) of the peak region at the low end of the output signal. In general, therefore, proper amplification design requires that the dc and ac components be sensitive to each other's requirements and limitations.

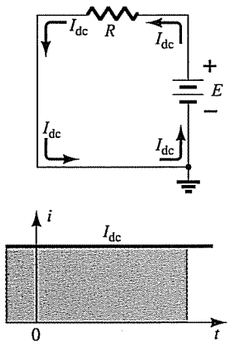


FIG. 5.1
Steady current established by a dc supply.

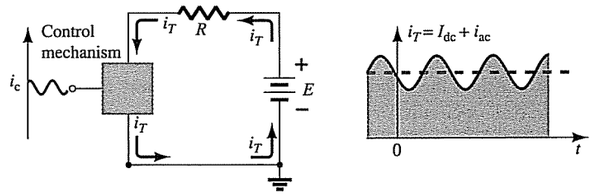


FIG. 5.2
Effect of a control element on the steady-state flow of the electrical system of Fig. 5.1.

However, it is extremely helpful to realize that:

The superposition theorem is applicable for the analysis and design of the dc and ac components of a BJT network, permitting the separation of the analysis of the dc and ac responses of the system.

In other words, one can make a complete dc analysis of a system before considering the ac response. Once the dc analysis is complete, the ac response can be determined using a completely ac analysis. It happens, however, that one of the components appearing in the ac analysis of BJT networks will be determined by the dc conditions, so there is still an important link between the two types of analysis.

5.3 BJT TRANSISTOR MODELING

The key to transistor small-signal analysis is the use of the equivalent circuits (models) to be introduced in this chapter.

A model is a combination of circuit elements, properly chosen, that best approximates the actual behavior of a semiconductor device under specific operating conditions.

Once the ac equivalent circuit is determined, the schematic symbol for the device can be replaced by this equivalent circuit and the basic methods of circuit analysis applied to determine the desired quantities of the network.

In the formative years of transistor network analysis the *hybrid equivalent network* was employed the most frequently. Specification sheets included the parameters in their listing, and analysis was simply a matter of inserting the equivalent circuit with the listed values. The drawback to using this equivalent circuit, however, is that it is defined for a set of operating conditions that might not match the actual operating conditions. In most cases, this is not a serious flaw because the actual operating conditions are relatively close to the chosen operating conditions on the data sheets. In addition, there is always a variation in actual resistor values and given transistor beta values, so as an approximate approach it was quite reliable. Manufacturers continue to specify the hybrid parameter values for a particular operating point on their specification sheets. They really have no choice. They want to give the user some idea of the value of each important parameter so comparisons can be made between transistors, but they really do not know the user's actual operating conditions.

In time the use of the r_e *model* became the more desirable approach because an important parameter of the equivalent circuit was determined by the actual operating conditions rather than using a data sheet value that in some cases could be quite different. Unfortunately, however, one must still turn to the data sheets for some of the other parameters of the equivalent circuit. The r_e model also failed to include a feedback term, which is some cases can be important if not simply troublesome.

The r_e model is really a reduced version of the *hybrid* π *model* used almost exclusively for high-frequency analysis. This model also includes a connection between output and input to include the feedback effect of the output voltage and the input quantities. The full hybrid model is introduced in Chapter 9.

Throughout the text the r_e model is the model of choice unless the discussion centers on the description of each model or a region of examination that predetermines the model that should be used. Whenever possible, however, a comparison between models will be discussed to show how closely related they really are. It is also important that once you gain a proficiency with one model it will carry over to an investigation using a different model, so moving from one to another will not be a dramatic undertaking.

In an effort to demonstrate the effect that the ac equivalent circuit will have on the analysis to follow, consider the circuit of Fig. 5.3. Let us assume for the moment that the small-signal ac equivalent circuit for the transistor has already been determined. Since we are interested only in the ac response of the circuit, all the dc supplies can be replaced by a zero-potential equivalent (short circuit) since they determine only the dc (quiescent level) of the output voltage and not the magnitude of the swing of the ac output. This is clearly demonstrated by Fig. 5.4. The dc levels were simply important for determining the proper Q-point of operation. Once determined, the dc levels can be ignored in the ac analysis of the network. In addition, the coupling capacitors C_1 and C_2 and bypass capacitor C_3 were

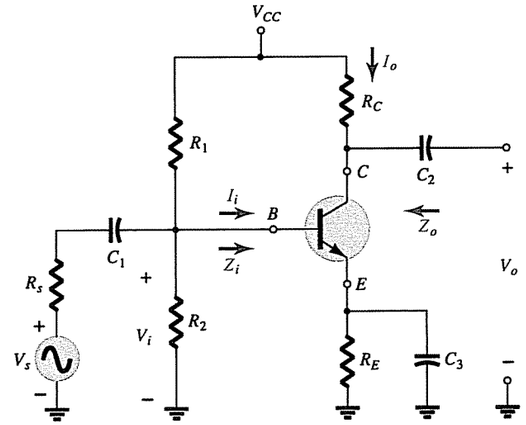


FIG. 5.3
Transistor circuit under examination in this introductory discussion.

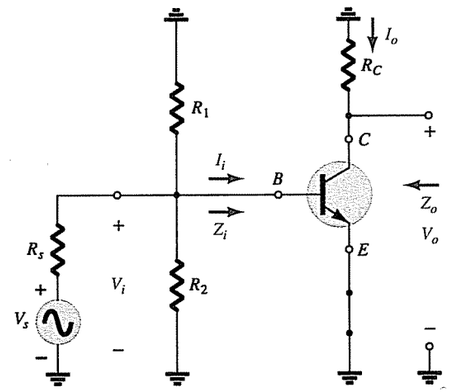


FIG. 5.4
The network of Fig. 5.3 following removal of the dc supply and insertion of the short-circuit equivalent for the capacitors.

chosen to have a very small reactance at the frequency of application. Therefore, they, too, may for all practical purposes be replaced by a low-resistance path or a short circuit. Note that this will result in the "shorting out" of the dc biasing resistor R_E. Recall that capacitors assume an "open-circuit" equivalent under dc steady-state conditions, permitting an isolation between stages for the dc levels and quiescent conditions.

It is important as you progress through the modifications of the network to define the ac equivalent that the parameters of interest such as Z_i, Z_o, I_i, and I_o be carried through properly. Even though the network appearance may change, you want to be sure the quantities you find in the reduced network are the same as defined by the original network. In both networks the input impedance is defined from base to ground, the input current as the base current of the transistor, the output voltage as the voltage from collector to ground, and the output current as the current through the load resistor R_C.

If we establish a common ground and rearrange the elements of Fig. 5.4, R_1 and R_2 will be in parallel and R_C will appear from collector to emitter as shown in Fig. 5.5. Since the components of the transistor equivalent circuit appearing in Fig. 5.5 employ familiar components such as resistors and independent controlled sources, analysis techniques such as superposition, Thévenin's theorem, and so on, can be applied to determine the desired quantities.

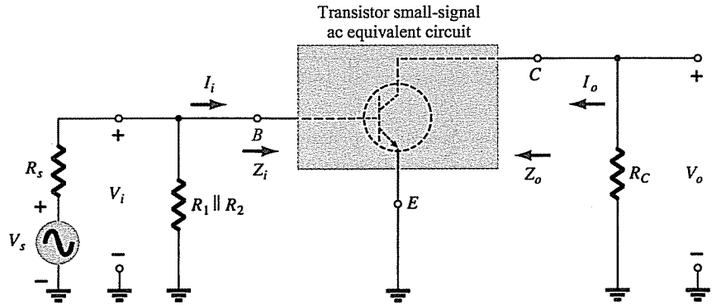


FIG. 5.5
Circuit of Fig. 5.4 redrawn for small-signal ac analysis.

Let us further examine Fig. 5.5 and identify the important quantities to be determined for the system. Since we know that the transistor is an amplifying device, we would expect some indication of how the output voltage V_o is related to the input voltage V_i—the *voltage gain*. Note in Fig. 5.5 for this configuration that $I_i = I_b$ and $I_o = I_c$, which define the *current gain* $A_i = I_o/I_i$. The input impedance Z_i and the output impedance Z_o will prove particularly important in the analysis to follow. A great deal more will be offered about these parameters in the sections to follow.

In summary, therefore, the ac equivalent of a network is obtained by:

1. Setting all dc sources to zero and replacing them by a short-circuit equivalent
2. Replacing all capacitors by a short-circuit equivalent
3. Removing all elements bypassed by the short-circuit equivalents introduced by steps 1 and 2
4. Redrawing the network in a more convenient and logical form

In the sections to follow, a transistor equivalent model will be introduced to complete the ac analysis of the network of Fig. 5.5.

5.4 THE r_e TRANSISTOR MODEL

The r_e model for the CB, CE, and CC BJT transistor configurations will now be introduced with a short description of why each is a good approximation to the actual behavior of a BJT transistor.

Common-Base Configuration

The common-base BJT transistor of Fig. 5.6a has been replaced by the r_e model for this configuration in Fig. 5.6b. Take immediate note of the fact the transistor action in this configuration has been replaced by a single diode between emitter and base terminals and a

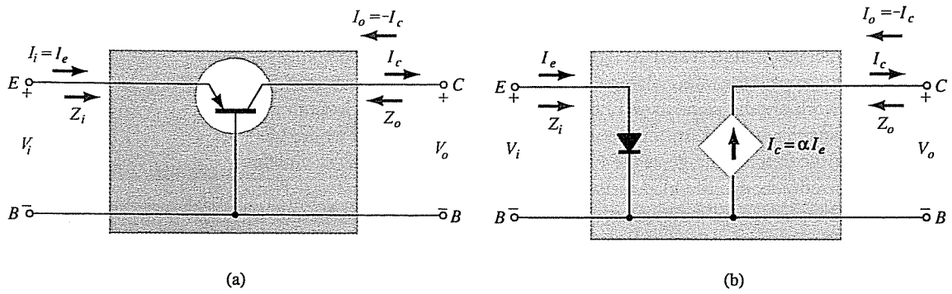


FIG. 5.6
(a) Common-base BJT transistor; (b) r_e model for the configuration of (a).

controlled current source between base and collector terminals. In general, this is a rather simple equivalent circuit for a device that might have appeared a lot more complicated in Chapter 4. However, when one compares the *p–n* junction at the input of a common-base transistor in Chapter 4 to the use of a *p–n* junction diode in Fig. 5.6b the equivalence on the input side seems appropriate. Since α is typically very close to one, the controlled source is simply stating that the output collector current is approximately equal to the input emitter current, conforming with the basic response of a transistor. That is, the collector characteristics of a CB transistor in Chapter 4 clearly reveal through the horizontal lines that the collector current is very close to the emitter current for the full range of collector-to-base voltages. It is also important to note that there is an isolation between the output collector side of the equivalent circuit of Fig. 5.6b and the input emitter circuit, limiting the interaction between input and output sections to the controlled source. Take particular note of the diamond-shaped enclosure defining the controlled source in Fig. 5.6b. Any controlled source will employ the diamond shape, whereas all fixed dc current sources will continue to employ the circle representation. In this case the collector current is "controlled" by the level of emitter current.

For the ac response, the diode can be replaced by its equivalent ac resistance. Recall from Chapter 1 that the ac resistance of a diode can be determined by the equation $r_{ac} = 26\,\text{mV}/I_D$, where I_D is the dc current through the diode at the Q (quiescent) point. This same equation can be used to find the ac resistance of the diode of Fig. 5.6b if we simply substitute the emitter current as follows:

$$r_e = \frac{26\,\text{mV}}{I_E} \tag{5.1}$$

The subscript e of r_e was chosen to emphasize that it is the dc level of emitter current that determines the ac level of the resistance of the diode of Fig. 5.6b. Substituting the resulting value of r_e in Fig. 5.6b results in the very useful model of Fig. 5.7.

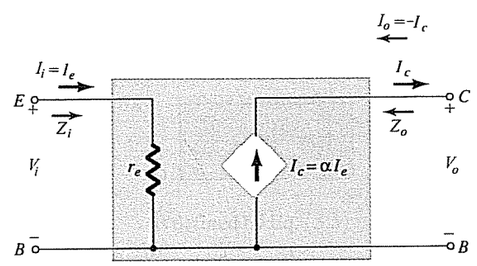


FIG. 5.7
Common-base r_e equivalent circuit.

Due to the isolation that exists between input and output circuits of Fig. 5.7, it should be fairly obvious that the input impedance Z_i for the common-base configuration of a transistor is simply r_e. That is,

$$Z_i = r_e \quad \text{CB} \tag{5.2}$$

For the common-base configuration, typical values of Z_i range from a few ohms to a maximum of about 50 Ω.

For the output impedance, if we set the signal to zero, then $I_e = 0\,\text{A}$ and $I_c = \alpha I_e = \alpha(0\,\text{A}) = 0\,\text{A}$, resulting in an open-circuit equivalence at the output terminals. The result is that for the model of Fig. 5.7,

$$Z_o \cong \infty\ \Omega \quad \text{CB} \tag{5.3}$$

In actuality:

For the common-base configuration, typical values of Z_o are in the megohm range.

The output resistance of the common-base configuration is determined by the slope of the characteristic lines of the output characteristics as shown in Fig. 5.8. Assuming the lines to be perfectly horizontal (an excellent approximation) would result in the conclusion of Eq. (5.3). If care were taken to measure Z_o graphically or experimentally, levels typically in the range 1 MΩ to 2 MΩ would be obtained.

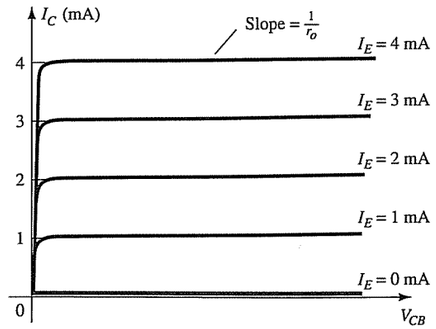


FIG. 5.8
Defining Z_o.

In general, for the common-base configuration the input impedance is relatively small and the output impedance quite high.

The voltage gain will now be determined for the network of Fig. 5.9. We have

$$V_o = -I_o R_L = -(-I_c)R_L = \alpha I_e R_L$$

and

$$V_i = I_i Z_i = I_e Z_i = I_e r_e$$

so that

$$A_v = \frac{V_o}{V_i} = \frac{\alpha I_e R_L}{I_e r_e}$$

and

$$\boxed{A_v = \frac{\alpha R_L}{r_e} \cong \frac{R_L}{r_e}} \quad CB \tag{5.4}$$

For the current gain,

$$A_i = \frac{I_o}{I_i} = \frac{-I_c}{I_e} = -\frac{\alpha I_e}{I_e}$$

and

$$\boxed{A_i = -\alpha \cong -1} \quad CB \tag{5.5}$$

The fact that the polarity of the voltage V_o as determined by the current I_c is the same as defined by Fig. 5.9 (i.e., the negative side is at ground potential) reveals that V_o and V_i are *in phase* for the common-base configuration. For an *npn* transistor in the common-base configuration, the equivalence appears as shown in Fig. 5.10.

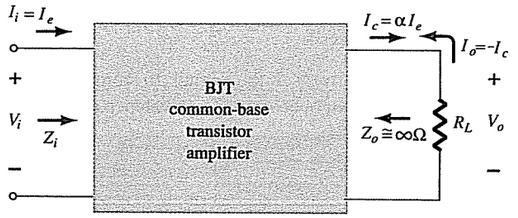


FIG. 5.9
Defining $A_v = V_o/V_i$ for the common-base configuration.

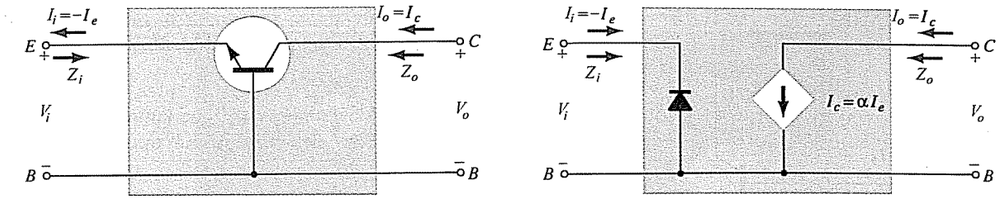


FIG. 5.10
Approximate model for a common-base npn transistor configuration.

EXAMPLE 5.1 For a common-base configuration of Fig. 5.7 with $I_E = 4$ mA, $\alpha = 0.98$, and an ac signal of 2 mV applied between the base and emitter terminals:

a. Determine the input impedance.
b. Calculate the voltage gain if a load of 0.56 kΩ is connected to the output terminals.
c. Find the output impedance and current gain.

Solution:

a. $$r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{4\text{ mA}} = \mathbf{6.5\ \Omega}$$

b. $$I_i = I_e = \frac{V_i}{Z_i} = \frac{2\text{ mV}}{6.5\ \Omega} = 307.69\ \mu\text{A}$$

$$V_o = I_c R_L = \alpha I_e R_L = (0.98)(307.69\ \mu\text{A})(0.56\text{ k}\Omega)$$
$$= 168.86\text{ mV}$$

and $$A_v = \frac{V_o}{V_i} = \frac{168.86\text{ mV}}{2\text{ mV}} = \mathbf{84.43}$$

or from Eq. (5.4),

$$A_v = \frac{\alpha R_L}{r_e} = \frac{(0.98)(0.56\text{ k}\Omega)}{6.5\ \Omega} = \mathbf{84.43}$$

c. $Z_o \cong \infty\ \Omega$

$$A_i = \frac{I_o}{I_i} = -\alpha = \mathbf{-0.98} \qquad \text{as defined by Eq. (5.5)}$$

Common-Emitter Configuration

For the common-emitter configuration of Fig. 5.11a, the input terminals are the base and emitter terminals, but the output set is now the collector and emitter terminals. In addition, the emitter terminal is now common between the input and output ports of the amplifier. Substituting the r_e equivalent circuit for the *npn* transistor results in the configuration of Fig. 5.11b. Note that the controlled-current source is still connected between the collector and base terminals and the diode between the base and emitter terminals. In this configuration, the base current is the input current, whereas the output current is still I_c. Recall from Chapter 3 that the base and collector currents are related by the following equation:

$$\boxed{I_c = \beta I_b} \tag{5.6}$$

The current through the diode is therefore determined by

$$I_e = I_c + I_b = \beta I_b + I_b$$

and

$$\boxed{I_e = (\beta + 1)I_b} \tag{5.7}$$

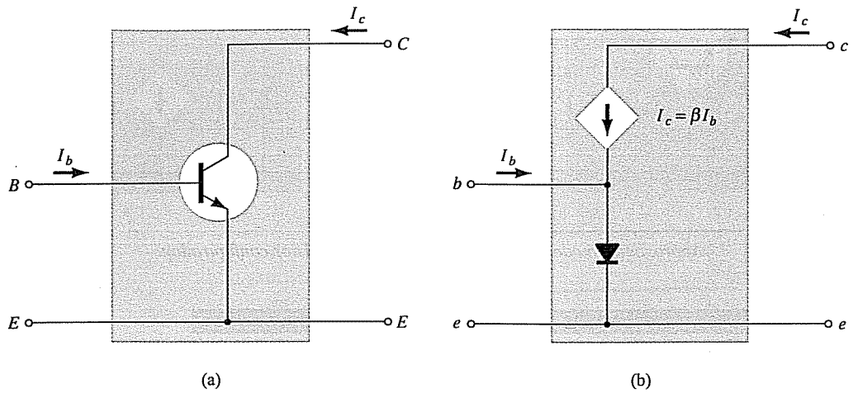


FIG. 5.11
(a) Common-emitter BJT transistor; (b) approximate model for the configuration of (a).

However, since the ac beta is typically much greater than 1, we will use the following approximation for the current analysis:

$$\boxed{I_e \cong \beta I_b} \tag{5.8}$$

The input impedance is determined by the following ratio:

$$Z_i = \frac{V_i}{I_i} = \frac{V_{be}}{I_b}$$

The voltage V_{be} is across the diode resistance as shown in Fig. 5.12. The level of r_e is still determined by the dc current I_E. Using Ohm's law gives

$$V_i = V_{be} = I_e r_e = (I_c + I_b)r_e = (\beta I_b + I_b)r_e = (\beta + 1)I_b r_e$$

Substituting yields

$$Z_i = \frac{V_{be}}{I_b} = \frac{(\beta + 1)I_b r_e}{I_b} = (\beta + 1)r_e$$

However, β is usually sufficiently larger than one to permit the approximation $\beta + 1 \cong \beta$, so that

$$\boxed{Z_i \cong \beta r_e}_{CE} \tag{5.9}$$

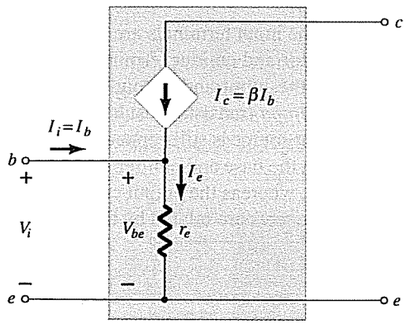


FIG. 5.12
Determining Z_i using the approximate model.

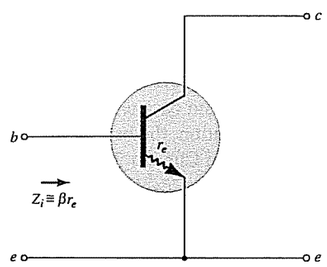


FIG. 5.13
Effect of r_e on input impedance.

In essence, Eq. (5.9) states that the input impedance for a situation such as shown in Fig. 5.13 is beta times the value of r_e. In other words, a resistive element in the emitter leg

is reflected into the input circuit by a multiplying factor β. For instance, if $r_e = 6.5\ \Omega$ as in Example 5.1 and $\beta = 160$ (quite typical), the input impedance increases to a level of

$$Z_i \cong \beta r_e = (160)(6.5\ \Omega) = \mathbf{1.04\ k\Omega}$$

For the common-emitter configuration, typical values of Z_i defined by βr_e range from a few hundred ohms to the kilohm range, with maxima of about 6 kΩ to 7 kΩ.

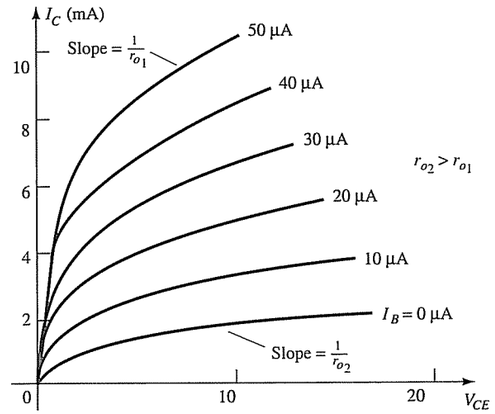


FIG. 5.14
Defining r_o for the common-emitter configuration.

For the output impedance, the characteristics of interest are the output set of Fig. 5.14. Note that the slope of the curves increases with increase in collector current. The steeper the slope, the less is the level of output impedance (Z_o). The r_e model of Fig. 5.11 does not include an output impedance, but if available from a graphical analysis or from data sheets, it can be included as shown in Fig. 5.15.

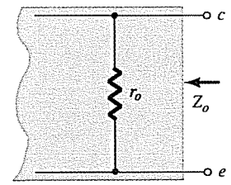


FIG. 5.15
Including r_o in the transistor equivalent circuit.

For the common-emitter configuration, typical values of Z_o are in the range of 40 kΩ to 50 kΩ.

For the model of Fig. 5.15, if the applied signal is set to zero, the current I_c is 0 A and the output impedance is

$$\boxed{Z_o = r_o}_{CE} \tag{5.10}$$

Of course, if the contribution due to r_o is ignored as in the r_e model, the output impedance is defined by $Z_o = \infty\ \Omega$.

The voltage gain for the common-emitter configuration will now be determined for the configuration of Fig. 5.16 using the assumption that $Z_o = \infty\ \Omega$. The effect of including r_o will be considered later in the chapter. For the defined direction of I_o and polarity of V_o,

$$V_o = -I_o R_L$$

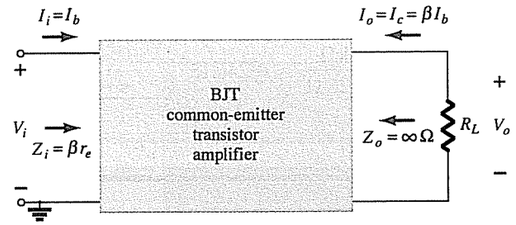


FIG. 5.16
Determining the voltage and current gain for the common-emitter transistor amplifier.

The minus sign simply reflects the fact that the direction of I_o in Fig. 5.16 would establish a voltage V_o with the opposite polarity. Continuing gives

$$V_o = -I_o R_L = -I_c R_L = -\beta I_b R_L$$

and

$$V_i = I_i Z_i = I_b \beta r_e$$

so that

$$A_v = \frac{V_o}{V_i} = -\frac{\beta I_b R_L}{I_b \beta r_e}$$

and

$$\boxed{A_v = -\frac{R_L}{r_e}}_{CE, r_o = \infty\Omega} \qquad \textbf{(5.11)}$$

The resulting minus sign for the voltage gain reveals that the output and input voltages are 180° out of phase.

The current gain for the configuration of Fig. 5.16 is given by

$$A_i = \frac{I_o}{I_i} = \frac{I_c}{I_b} = \frac{\beta I_b}{I_b}$$

and

$$\boxed{A_i = \beta}_{CE, r_o = \infty\Omega} \qquad \textbf{(5.12)}$$

Using the facts that the input impedance is βr_e, the collector current is βI_b, and the output impedance is r_o, we find that the equivalent model of Fig. 5.17 can be an effective tool in the analysis to follow. For typical parameter values, the common-emitter configuration can be considered to have a moderate level of input impedance, a high voltage and current gain, and an output impedance that may have to be included in the network analysis.

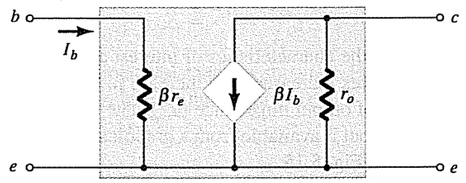


FIG. 5.17
r_e model for the common-emitter transistor configuration.

EXAMPLE 5.2 Given $\beta = 120$ and $I_E = 3.2\,\text{mA}$ for a common-emitter configuration with $r_o = \infty\ \Omega$, determine:

a. Z_i.
b. A_v if a load of $2\,\text{k}\Omega$ is applied.
c. A_i with the 2-kΩ load.

Solution:

a. $r_e = \dfrac{26\,\text{mV}}{I_E} = \dfrac{26\,\text{mV}}{3.2\,\text{mV}} = 8.125\ \Omega$

and $Z_i = \beta r_e = (120)(8.125\ \Omega) = \mathbf{975\ \Omega}$

b. Eq. (5.11): $A_v = -\dfrac{R_L}{r_e} = -\dfrac{2\,\text{k}\Omega}{8.125\ \Omega} = \mathbf{-246.15}$

c. $A_i = \dfrac{I_o}{I_i} = \beta = \mathbf{120}$

Common-Collector Configuration

For the common-collector configuration, the model defined for the common-emitter configuration of Fig. 5.11 is normally applied rather than defining a model for the common-collector configuration. In subsequent chapters, a number of common-collector configurations will be investigated, and the effect of using the same model will become quite apparent.

5.5 THE HYBRID EQUIVALENT MODEL

It was clearly pointed out in the previous section that the r_e model for a transistor is sensitive to the dc level of operation of the amplifier. The result is an input resistance that will vary with the dc operating point.

For the hybrid equivalent model the parameters are defined at an operating point that may or may not reflect the actual operating conditions of the amplifier.

This is due to the fact that specification sheets cannot provide parameters for an equivalent circuit at every possible operating point. They must choose operating conditions that they believe reflect the most common use of the device. The hybrid parameters as shown in Fig. 5.18 are derived from the specification sheet for the 2N4400 transistor described in Chapter 3. The values are provided at a dc collector current of 1 mA and a collector-to-emitter voltage of 10 V. In addition, a range of values is provided for each parameter for guidance in the initial design or analysis of a system. One obvious advantage of the specification sheet listing is the immediate knowledge of typical levels for the parameters of the device as compared to other transistors.

		Min.	Max.	
Input impedance (I_C = 1 mA dc, V_{CE} = 10 V dc, f = 1 kHz)	h_{ie}	0.5	7.5	kΩ
Voltage feedback ratio (I_C = 1 mA dc, V_{CE} = 10 V dc, f = 1 kHz)	h_{re}	0.1	8.0	$\times 10^{-4}$
Small-signal current gain (I_C = 1 mA dc, V_{CE} = 10 V dc, f = 1 kHz)	h_{fe}	20	250	—
Output admittance (I_C = 1 mA dc, V_{CE} = 10 V dc, f = 1 kHz)	h_{oe}	1.0	30	1 μS

FIG. 5.18
Hybrid parameters for the 2N4400 transistor.

The quantities h_{ie}, h_{re}, h_{fe}, and h_{oe} of Fig. 5.18 are called the hybrid parameters and are the components of a small-signal equivalent circuit to be described shortly. For years, the hybrid model with all its parameters was the chosen model for the educational and industrial communities. At present, however, the r_e model is applied more frequently, but often with the h_{oe} parameter of the hybrid equivalent model to provide some measure for the output impedance. Since specification sheets do provide the hybrid parameters and the hybrid model continues to receive a good measure of attention, it is quite important that the hybrid model be covered in some detail in this book. Once developed, the similarities between the r_e and hybrid models will be quite apparent. In fact, once the components of one are defined for a particular operating point, the parameters of the other model are immediately available.

Our description of the hybrid equivalent model will begin with the general two-port system of Fig. 5.19. The following set of equations (5.13) and (5.14) is only one of a number of

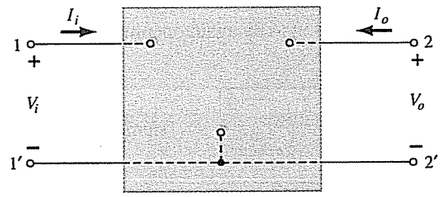


FIG. 5.19
Two-port system.

ways in which the four variables of Fig. 5.19 can be related. It is the most frequently employed in transistor circuit analysis, however, and therefore is discussed in detail in this chapter.

$$V_i = h_{11}I_i + h_{12}V_o \tag{5.13}$$

$$I_o = h_{21}I_i + h_{22}V_o \tag{5.14}$$

The parameters relating the four variables are called *h-parameters*, from the word "hybrid." The term *hybrid* was chosen because the mixture of variables (V and I) in each equation results in a "hybrid" set of units of measurement for the h-parameters. A clearer understanding of what the various h-parameters represent and how we can determine their magnitude can be developed by isolating each and examining the resulting relationship.

If we arbitrarily set $V_o = 0$ (short circuit the output terminals) and solve for h_{11} in Eq. (5.13), we find

$$h_{11} = \left.\frac{V_i}{I_i}\right|_{V_o=0} \quad \text{ohms} \tag{5.15}$$

The ratio indicates that the parameter h_{11} is an impedance parameter with the units of ohms. Since it is the ratio of the *input* voltage to the *input* current with the output terminals *shorted*, it is called the *short-circuit input-impedance parameter*. The subscript 11 of h_{11} refers to the fact that the parameter is determined by a ratio of quantities measured at the input terminals.

If I_i is set equal to zero by opening the input leads, the following results for h_{12}:

$$h_{12} = \left.\frac{V_i}{V_o}\right|_{I_i=0} \quad \text{unitless} \tag{5.16}$$

The parameter h_{12}, therefore, is the ratio of the input voltage to the output voltage with the input current equal to zero. It has no units since it is a ratio of voltage levels, and is called the *open-circuit reverse transfer voltage ratio parameter*. The subscript 12 of h_{12} indicates that the parameter is a transfer quantity determined by a ratio of input to output measurements. The first integer of the subscript defines the measured quantity to appear in the numerator; the second integer defines the source of the quantity to appear in the denominator. The term *reverse* is included because the ratio is an input voltage over an output voltage rather than the reverse ratio typically of interest.

If in Eq. (5.14) V_o is set equal to zero by again shorting the output terminals, the following results for h_{21}:

$$h_{21} = \left.\frac{I_o}{I_i}\right|_{V_o=0} \quad \text{unitless} \tag{5.17}$$

Note that we now have the ratio of an output quantity to an input quantity. The term *forward* will now be used rather than *reverse* as indicated for h_{12}. The parameter h_{21} is the ratio of the output current to the input current with the output terminals shorted. This parameter, like h_{12}, has no units since it is the ratio of current levels. It is formally called the *short-circuit forward transfer current ratio parameter*. The subscript 21 again indicates that it is a transfer parameter with the output quantity in the numerator and the input quantity in the denominator.

The last parameter, h_{22}, can be found by again opening the input leads to set $I_1 = 0$ and solving for h_{22} in Eq. (5.14):

$$h_{22} = \left.\frac{I_o}{V_o}\right|_{I_i=0} \quad \text{siemens} \tag{5.18}$$

Since it is the ratio of the output current to the output voltage, it is the output conductance parameter, and it is measured in siemens (S). It is called the *open-circuit output admittance parameter*. The subscript 22 indicates that it is determined by a ratio of output quantities.

Since each term of Eq. (5.13) has the unit volt, let us apply Kirchhoff's voltage law "in reverse" to find a circuit that "fits" the equation. Performing this operation results in the circuit of Fig. 5.20. Since the parameter h_{11} has the unit ohm, it is represented by a resistor in Fig. 5.20. The quantity h_{12} is dimensionless and therefore simply appears as a multiplying factor of the "feedback" term in the input circuit.

Since each term of Eq. (5.21) has the units of current, let us now apply Kirchhoff's current law "in reverse" to obtain the circuit of Fig. 5.21. Since h_{22} has the units of admittance, which for the transistor model is conductance, it is represented by the resistor symbol. Keep in mind, however, that the resistance in ohms of this resistor is equal to the reciprocal of conductance ($1/h_{22}$).

The complete "ac" equivalent circuit for the basic three-terminal linear device is indicated in Fig. 5.22 with a new set of subscripts for the h-parameters. The notation of Fig. 5.22 is of a more practical nature since it relates the h-parameters to the resulting ratio obtained in the last few paragraphs. The choice of letters is obvious from the following listing:

$h_{11} \rightarrow$ *i*nput resistance $\rightarrow h_i$

$h_{12} \rightarrow$ *r*everse transfer voltage ratio $\rightarrow h_r$

$h_{21} \rightarrow$ *f*orward transfer current ratio $\rightarrow h_f$

$h_{22} \rightarrow$ *o*utput conductance $\rightarrow h_o$

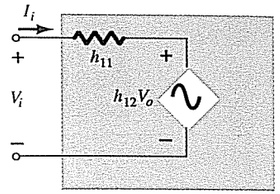


FIG. 5.20
Hybrid input equivalent circuit.

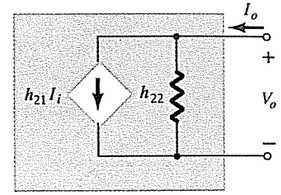


FIG. 5.21
Hybrid output equivalent circuit.

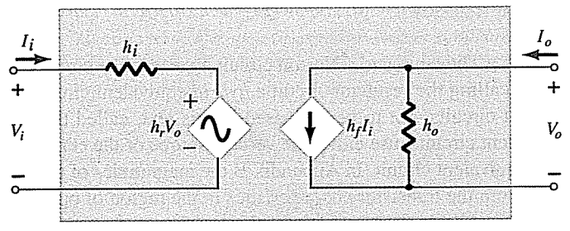


FIG. 5.22
Complete hybrid equivalent circuit.

The circuit of Fig. 5.22 is applicable to any linear three-terminal electronic device or system with no internal independent sources. For the transistor, therefore, even though it has three basic configurations, *they are all three-terminal configurations*, so that the resulting equivalent circuit will have the same format as shown in Fig. 5.22. In each case, the bottom of the input and output sections of the network of Fig. 5.22 can be connected as shown in Fig. 5.23 since the potential level is the same. Essentially, therefore, the transistor model is a three-terminal two-port system. The h-parameters, however, will change with each configuration. To distinguish which parameter has been used or which is available, a second subscript has been added to the h-parameter notation. For the common-base configuration, the lowercase letter b was added, whereas for the common-emitter and common-collector

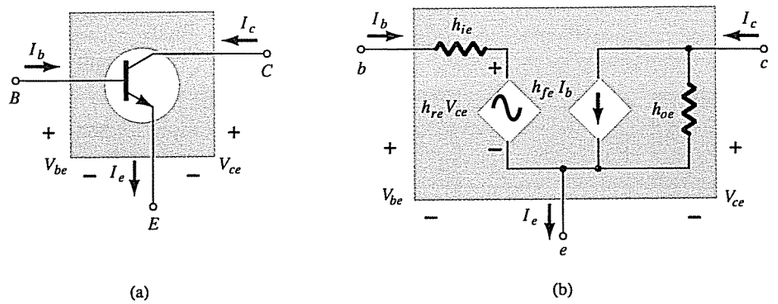


FIG. 5.23
Common-emitter configuration: (a) graphical symbol; (b) hybrid equivalent circuit.

configurations, the letters *e* and *c* were added, respectively. The hybrid equivalent network for the common-emitter configuration appears with the standard notation in Fig. 5.23. Note that $I_i = I_b$, $I_o = I_c$, and, through an application of Kirchhoff's current law, $I_e = I_b + I_c$. The input voltage is now V_{be}, with the output voltage V_{ce}. For the common-base configuration of Fig. 5.24, $I_i = I_e$, $I_o = I_c$ with $V_{eb} = V_i$ and $V_{cb} = V_o$. The networks of Figs. 5.23 and 5.24 are applicable for *pnp* or *npn* transistors.

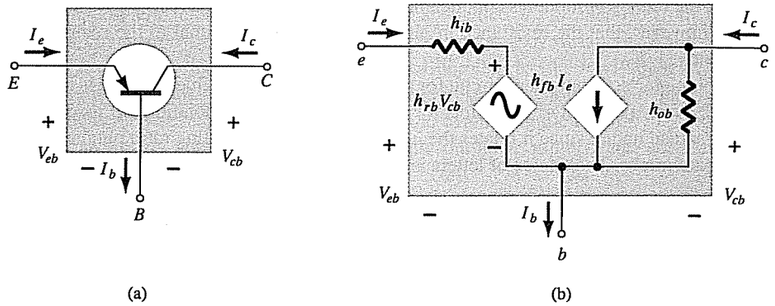


FIG. 5.24
Common-base configuration: (a) graphical symbol; (b) hybrid equivalent circuit.

The fact that both a Thévenin and a Norton circuit appear in the circuit of Fig. 5.22 was further impetus for calling the resultant circuit a *hybrid* equivalent circuit. Two additional transistor equivalent circuits, not to be discussed in this text, called the **z**-parameter and **y**-parameter equivalent circuits, use either the voltage source or the current source, but not both, in the same equivalent circuit. In Appendix B the magnitudes of the various parameters will be found from the transistor characteristics in the region of operation resulting in the desired *small-signal equivalent network* for the transistor.

For the common-emitter and common-base configurations, the magnitude of h_r and h_o is often such that the results obtained for the important parameters such as Z_i, Z_o, A_v, and A_i are only slightly affected if h_r and h_o are not included in the model.

Since h_r is normally a relatively small quantity, its removal is approximated by $h_r \cong 0$ and $h_r V_o = 0$, resulting in a short-circuit equivalent for the feedback element as shown in Fig. 5.25. The resistance determined by $1/h_o$ is often large enough to be ignored in comparison to a parallel load, permitting its replacement by an open-circuit equivalent for the CE and CB models, as shown in Fig. 5.25.

The resulting equivalent of Fig. 5.26 is quite similar to the general structure of the common-base and common-emitter equivalent circuits obtained with the r_e model. In fact, the hybrid equivalent and the r_e models for each configuration are repeated in Fig. 5.27 for comparison. It should be reasonably clear from Fig. 5.27a that

$$\boxed{h_{ie} = \beta r_e} \tag{5.19}$$

and

$$\boxed{h_{fe} = \beta_{ac}} \tag{5.20}$$

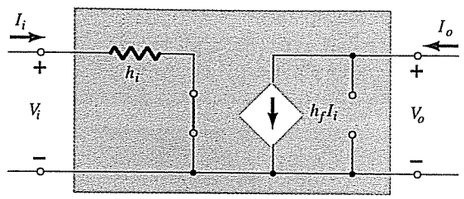


FIG. 5.25
Effect of removing h_{re} and h_{oe} from the hybird equivalent circuit.

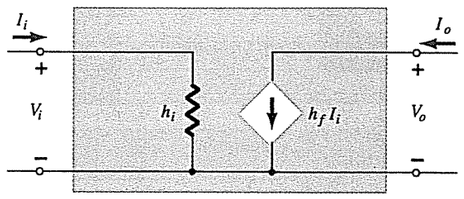


FIG. 5.26
Approximate hybrid equivalent model.

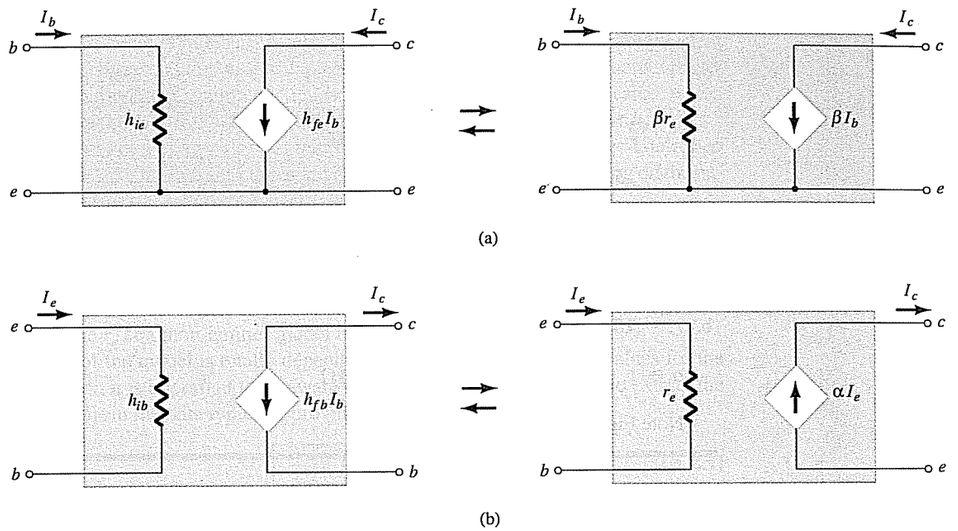


FIG. 5.27
Hybrid versus r_e model: (a) common-emitter configuration; (b) common-base configuration.

From Fig. 5.27b,

$$\boxed{h_{ib} = r_e} \tag{5.21}$$

and

$$\boxed{h_{fb} = -\alpha \cong -1} \tag{5.22}$$

In particular, note that the minus sign in Eq. (5.22) accounts for the fact that the current source of the standard hybrid equivalent circuit is pointing down rather than in the actual direction as shown in the r_e model of Fig. 5.27b.

EXAMPLE 5.3 Given $I_E = 2.5\,\text{mA}$, $h_{fe} = 140$, $h_{oe} = 20\,\mu\text{S}$ (μmho), and $h_{ob} = 0.5\,\mu\text{S}$, determine:

a. The common-emitter hybrid equivalent circuit.
b. The common-base r_e model.

Solution:

a. $$r_e = \frac{26\,\text{mV}}{I_E} = \frac{26\,\text{mV}}{2.5\,\text{mA}} = \mathbf{10.4\,\Omega}$$

$$h_{ie} = \beta r_e = (140)(10.4\,\Omega) = \mathbf{1.456\,k\Omega}$$

$$r_o = \frac{1}{h_{oe}} = \frac{1}{20\,\mu\text{S}} = \mathbf{50\,k\Omega}$$

Note Fig. 5.28.

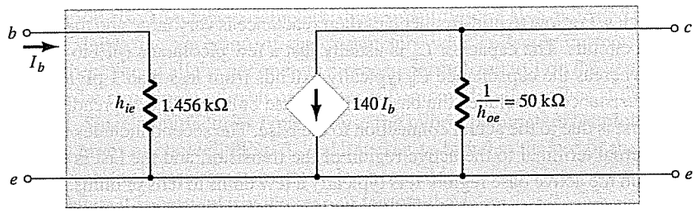


FIG. 5.28
Common-emitter hybrid equivalent circuit for the parameters of Example 5.3.

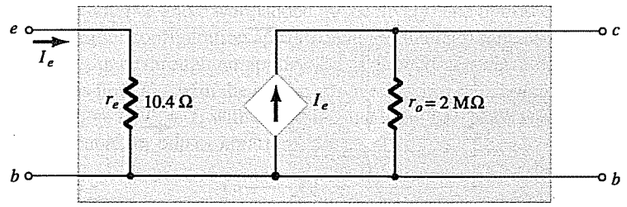


FIG. 5.29
Common-base r_e model for the parameters of Example 5.3.

b. $r_e = \mathbf{10.4\ \Omega}$

$\alpha \cong 1, \qquad r_o = \dfrac{1}{h_{ob}} = \dfrac{1}{0.5\ \mu\text{S}} = \mathbf{2\ M\Omega}$

Note Fig. 5.29.

A series of equations relating the parameters of each configuration for the hybrid equivalent circuit is provided in Appendix B. In Section 5.6 it is demonstrated that the hybrid parameter h_{fe} (β_{ac}) is the least sensitive of the hybrid parameters to a change in collector current. Assuming, therefore, that $h_{fe} = \beta$ is a constant for the range of interest, is a fairly good approximation. It is $h_{ie} = \beta r_e$ that will vary significantly with I_C and should be determined at operating levels, since it can have a real effect on the gain levels of a transistor amplifier.

5.6 HYBRID π MODEL

The hybrid π model includes parameters that do not appear in the other two models primarily to provide a more accurate model for high-frequency effects. For lower frequencies approximations to the model can be made with the result that the r_e model introduced earlier will result. The hybrid π model appears in Fig. 5.30 with all the parameters necessary for a full-frequency analysis.

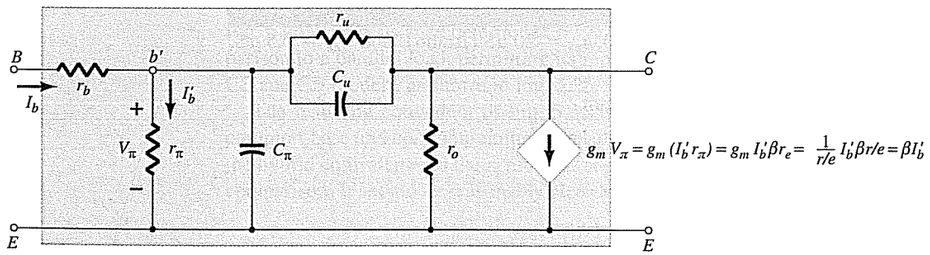


FIG. 5.30
Giacoletto (or hybrid π) high-frequency transistor small-signal ac equivalent circuit.

All the capacitors that appear in Fig. 5.30 are stray parasitic capacitors between the various junctions of the device. They are all capacitive effects that really only come into play at high frequencies. For low to mid-frequencies their reactance is very large and they can be considered open circuits. The capacitor C_u is usually just a few picofarads (pF) to a few tens of picofarads, whereas the capacitance C_u typically extends from less than 1 pF to a few picofarads. The resistance r_b includes the base contact, base bulk, and base spreading resistance levels. The first is due to the actual connection to the base. The second includes the resistance from the external terminal to the active region of the transistor, and the last is the actual resistance within the active base region. It is typically a few ohms to tens of ohms. The resistors r_π, r_u, and r_o are the resistances between the indicated terminals of the device when the device is in the active region. The resistance r_π (using the symbol π to agree with the hybrid π terminology) is simply βr_e as introduced for the common-emitter r_e model. The resistance r_u (the subscript u refers to the *union* it provides between collector and base terminals) is a very large resistance, and provides a feedback path from output to input circuits in the equivalent model. It is typically larger than βr_o, which places it in the megohm range. The output resistance r_o is the output resistance normally appearing across an applied load. Its value, which typically lies between 5 kΩ and 40 kΩ, is determined from the hybrid parameter h_{oe}.

It is important to note in Fig. 5.30 that the controlled source can be a voltage-controlled current source (VCCS) or a current-controlled current source (CCCS), depending on the parameters employed.

For the broad range of low- to mid-frequency analysis, the effect of the stray capacitive effects can be ignored due to the very high reactance levels associated with each. The resistance r_b is usually so small it can be replaced by a short-circuit equivalent, and the resistance r_u is usually so large it can be ignored for most applications. The result is an equivalent network similar to the r_e common-emitter model introduced earlier.

Since the use of the model is totally dependent on finding the parameter values for the equivalent network, it is important to be aware of the following relationships to extract the parameter values from the data typically provided:

$$\boxed{r_\pi = \beta r_e} \tag{5.23}$$

$$\boxed{g_m = \frac{1}{r_e}} \tag{5.24}$$

$$\boxed{r_o = \frac{1}{h_{oe}}} \tag{5.25}$$

$$\boxed{h_{re} = \frac{r_\pi}{r_\pi + r_u} \cong \frac{r_\pi}{r_\mu}} \tag{5.26}$$

The equivalence between the two sources of Fig. 5.30 is demonstrated in the figure using Eqs. (5.23) and (5.24).

The hybrid π model will not appear in the small-signal analysis of this chapter since it is primarily used to investigate high-frequency effects. It will appear again in the discussion of high-frequency effects in Chapter 9.

5.7 VARIATIONS OF TRANSISTOR PARAMETERS

There are a variety of curves that can be drawn to show the variations of the transistor parameters with temperature, frequency, voltage, and current. The most interesting and useful at this stage of the development include the variations with junction temperature and collector voltage and current.

The effect of the collector current on the h-parameters is shown in Fig. 5.31. Take careful note of the logarithmic scale on the vertical and horizontal axes. Logarithmic scales will be examined in detail in Chapter 9. The parameters have all been normalized to unity so that the relative change in magnitude with collector current can easily be determined. On each set of curves, such as in Figs. 5.31 to 5.33, the operating point at which the parameters were determined is always indicated. For this particular situation, the quiescent point is at the fairly typical values of $V_{CE} = 5.0$ V and $I_C = 1.0$ mA. Since the frequency and temperature of operation also affect the parameters, these quantities are also indicated on the curves. Figure 5.31 shows the variation of the parameters with collector current. Note that at $I_C = 1$ mA the value of all the parameters has been normalized to 1 on the vertical axis. The result is that the magnitude of each parameter is compared to the values at the defined operating point. Since manufactures typically use the hybrid parameters for plots of this type, they are the curves of choice in Fig. 5.31. However, to broaden the use of the curves the r_e and hybrid π equivalent parameters have also been added.

At first glance it is particularly interesting to note that:

The parameter h_{fe} (β) varies the least of all the parameters of a transistor equivalent circuit when plotted against variations in collector current.

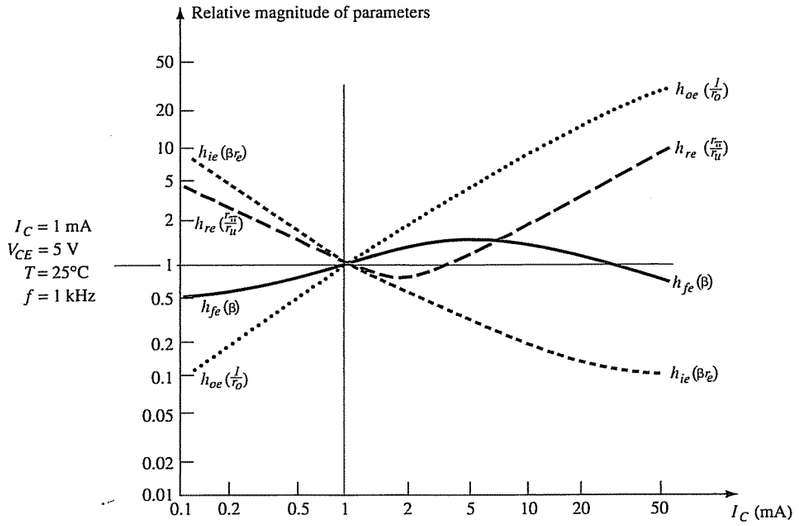


FIG. 5.31
Hybrid parameter variations with collector current.

Figure 5.31 clearly reveals that for the full range of collector current the parameter $h_{fe}(\beta)$ varies from 0.5 of its Q-point value to a peak of about 1.5 times that value at a current of about 6 mA. For a transistor with a β of 100, it therefore varies from about 50 to 150. This seems like quite a bit, but look at h_{oe}, which jumps to almost 40 times its Q-point value at a collector current of 50 mA.

Figure 5.31 also shows that $h_{oe}(1/r_o)$ and $h_{ie}(\beta r_e)$ vary the most for the chosen current range. The parameter h_{ie} varies from about 10 times its Q-point value down to about one tenth of Q-point the value at 50 mA. This variation, however, should be expected because we know that the value of r_e is directly related to the emitter current by $r_e = 26\,\text{mV}/I_E$. As $I_E(\cong I_C)$ increases, the value of r_e and therefore βr_e will decrease, as shown in Fig. 5.31.

Keep in mind as you review the curve of h_{oe} versus current that the actual output resistance r_o is $1/h_{oe}$. Therefore, as the curve increases with current, the value of r_o becomes less and less. Since r_o is a parameter that normally appears in parallel with the applied load, decreasing values of r_o can become a critical problem. The fact that r_o has dropped to almost 1/40 of its value at the Q-point could spell a real reduction in gain at 50 mA.

The parameter h_{re} varies quite a bit, but because its Q-point value is usually small enough to permit ignoring its effect, it is a parameter that is only of concern for collector currents that are much less, or quite a bit more, than the Q-point level.

This may seem like an extensive description of a set of characteristic curves. However, experience has revealed that graphs of this nature are too often reviewed without taking the time to fully appreciate the broad impact of what they are providing. These plots reveal a lot of information that could be extremely useful in the design process.

Figure 5.32 shows the variation in magnitude of the parameters due to changes in collector-to-emitter voltage. This set of curves is normalized at the same operating point as the curves of Fig. 5.31 to permit comparisons between the two. In this case, however, the vertical scale is in percent rather than whole numbers. The 200% level defines a set of parameters twice that at the 100% level. A level of 1000% would reflect a 10:1 change. Note that h_{fe} and h_{ie} are relatively steady in magnitude with variations in collector-to-emitter voltage, whereas for changes in collector current the variation is a great deal more significant. In other words, if you want a parameter such as $h_{ie}(\beta r_e)$ to remain fairly steady, keep the variation of I_C to a minimum while worrying less about variations in the collector-to-emitter voltage. The variation of h_{oe} and h_{ie} remains significant for the indicated range of collector-to-emitter voltage.

In Fig. 5.33, the variation in parameters is plotted for changes in junction temperature. The normalization value is taken to be room temperature, $T = 25°\text{C}$. The horizontal scale

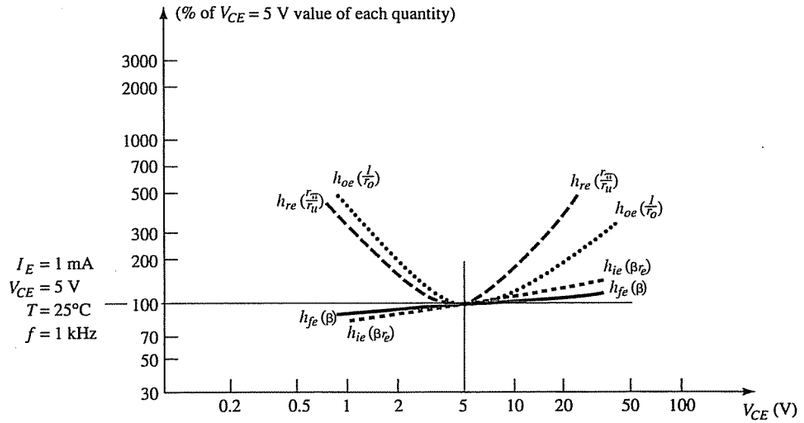


FIG. 5.32
Hybrid parameter variations with collector–emitter potential.

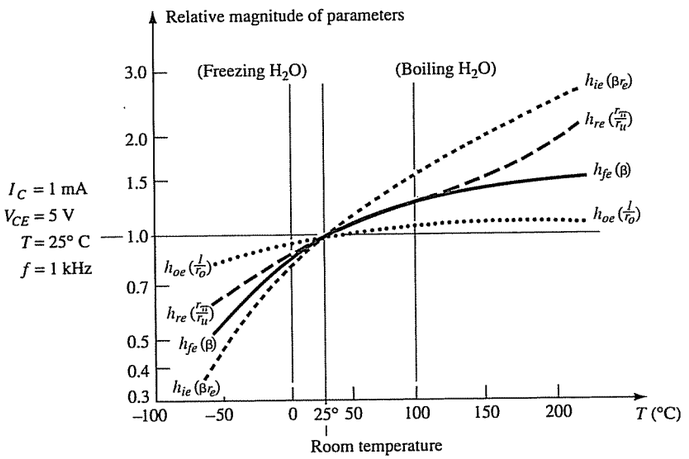


FIG. 5.33
Hybrid parameter variations with temperature.

is now a linear scale rather than the logarithmic scale employed in the two previous figures. In general:

All the parameters of a hybrid transistor equivalent circuit increase with temperature.

However, again keep in mind that the actual output resistance r_o is inversely related to h_{oe}, so its value drops with an increase in h_{oe}. The greatest change is in h_{ie}, although note that the range of the vertical scale is considerably less than in the other plots. At a temperature of 200°C the value of h_{ie} is almost 3 times its Q-point value, but in Fig. 5.31 parameters jumped to almost 40 times the Q-point value.

Of the three parameters, therefore, the variation in collector current has by far the greatest effect on the parameters of a transistor equivalent circuit. Temperature is always a factor, but the effect of the collector current can be significant.

5.8 COMMON-EMITTER FIXED-BIAS CONFIGURATION

The transistor models just introduced will now be used to perform a small-signal ac analysis of a number of standard transistor network configurations. The networks analyzed represent the majority of those appearing in practice. Modifications of the standard configurations

will be relatively easy to examine once the content of this chapter is reviewed and understood. For each configuration, the effect of an output impedance is examined as provided by the h_{oe} parameter of the hybrid equivalent model. To demonstrate the similarities in analysis that exist between models, a section is devoted to the small-signal analysis of BJT networks using solely the hybrid equivalent model.

The computer analysis section includes a brief description of the transistor model employed in the PSpice and Multisim software packages. It demonstrates the range and depth of the available computer analysis systems and how relatively easy it is to enter a complex network and print out the desired results. The first configuration to be analyzed in detail is the common-emitter *fixed-bias* network of Fig. 5.34. Note that the input signal V_i is applied to the base of the transistor, whereas the output V_o is off the collector. In addition, recognize that the input current I_i is not the base current, but the source current, and the output current I_o is the collector current. The small-signal ac analysis begins by removing the dc effects of V_{CC} and replacing the dc blocking capacitors C_1 and C_2 by short-circuit equivalents, resulting in the network of Fig. 5.35.

Note in Fig. 5.35 that the common ground of the dc supply and the transistor emitter terminal permits the relocation of R_B and R_C in parallel with the input and output sections of the transistor, respectively. In addition, note the placement of the important network parameters Z_i, Z_o, I_i, and I_o on the redrawn network. Substituting the r_e model for the common-emitter configuration of Fig. 5.35 results in the network of Fig. 5.36.

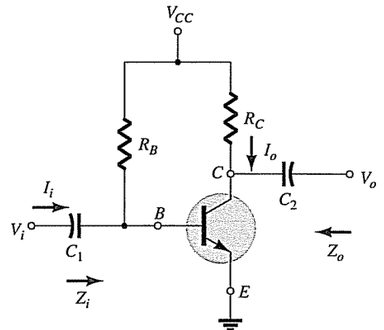


FIG. 5.34
Common-emitter fixed-bias configuration.

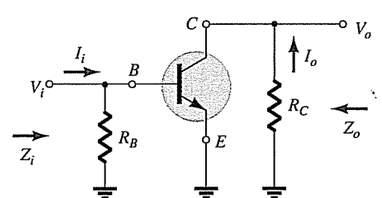


FIG. 5.35
Network of Fig. 5.34 following the removal of the effects of V_{CC}, C_1, and C_2.

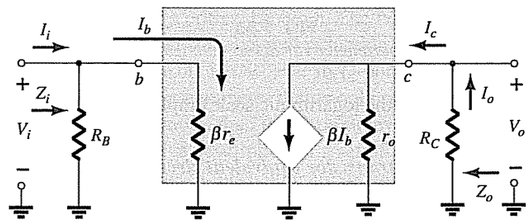


FIG. 5.36
Substituting the r_e model into the network of Fig. 5.35.

The next step is to determine β, r_e, and r_o. The magnitude of β is typically obtained from a specification sheet or by direct measurement using a curve tracer or transistor testing instrument. The value of r_e must be determined from a dc analysis of the system, and the magnitude of r_o is typically obtained from the specification sheet or characteristics. Assuming that β, r_e, and r_o have been determined will result in the following equations for the important two-port characteristics of the system.

Z_i Figure 5.36 clearly shows that

$$\boxed{Z_i = R_B \| \beta r_e} \quad \text{ohms} \tag{5.27}$$

For the majority of situations R_B is greater than βr_e by more than a factor of 10 (recall from the analysis of parallel elements that the total resistance of two parallel resistors is always less than the smallest and very close to the smallest if one is much larger than the other), permitting the following approximation:

$$\boxed{Z_i \cong \beta r_e}_{R_B \geq 10\beta r_e} \quad \text{ohms} \tag{5.28}$$

Z_o Recall that the output impedance of any system is defined as the impedance Z_o determined when $V_i = 0$. For Fig. 5.36, when $V_i = 0$, $I_i = I_b = 0$, resulting in an open-circuit equivalence for the current source. The result is the configuration of Fig. 5.37. We have

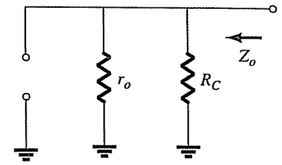


FIG. 5.37
Determining Z_o for the network of Fig. 5.36.

$$\boxed{Z_o = R_C \| r_o} \quad \text{ohms} \tag{5.29}$$

If $r_o \geq 10R_C$, the approximation $R_C \| r_o \cong R_C$ is frequently applied, and

$$\boxed{Z_o \cong R_C}_{r_o \geq 10R_C} \tag{5.30}$$

A_v The resistors r_o and R_C are in parallel, and

$$V_o = -\beta I_b (R_C \| r_o)$$

but

$$I_b = \frac{V_i}{\beta r_e}$$

so that

$$V_o = -\beta \left(\frac{V_i}{\beta r_e} \right) (R_C \| r_o)$$

and

$$\boxed{A_v = \frac{V_o}{V_i} = -\frac{(R_C \| r_o)}{r_o}} \tag{5.31}$$

If $r_o \geq 10R_C$,

$$\boxed{A_v = -\frac{R_C}{r_e}}_{r_o \geq 10R_C} \tag{5.32}$$

Note the explicit absence of β in Eqs. (5.31) and (5.32), although we recognize that β must be utilized to determine r_e.

Phase Relationship The negative sign in the resulting equation for A_v reveals that a 180° phase shift occurs between the input and output signals, as shown in Fig. 5.38.

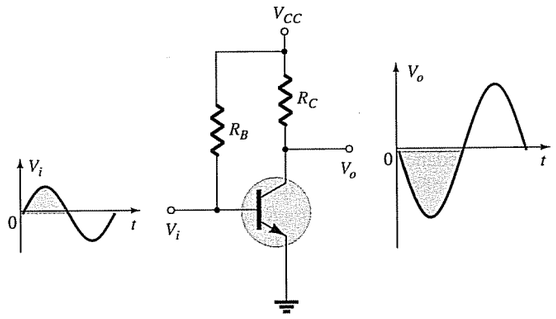


FIG. 5.38
Demonstrating the 180° phase shift between input and output waveforms.

EXAMPLE 5.4 For the network of Fig. 5.39:

Multisim PSpice

a. Determine r_e.
b. Find Z_i (with $r_o = \infty\ \Omega$).
c. Calculate Z_o (with $r_o = \infty\ \Omega$).
d. Determine A_v (with $r_o = \infty\ \Omega$).
e. Repeat parts (c) and (d) including $r_o = 50\ \text{k}\Omega$ in all calculations and compare results.

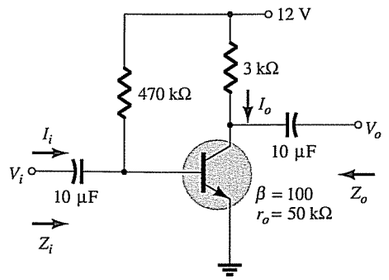


FIG. 5.39
Example 5.4.

Solution:

a. DC analysis:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12\ \text{V} - 0.7\ \text{V}}{470\ \text{k}\Omega} = 24.04\ \mu\text{A}$$

$$I_E = (\beta + 1)I_B = (101)(24.04\ \mu\text{A}) = 2.428\ \text{mA}$$

$$r_e = \frac{26\ \text{mV}}{I_E} = \frac{26\ \text{mV}}{2.428\ \text{mA}} = \mathbf{10.71\ \Omega}$$

b. $\beta r_e = (100)(10.71\ \Omega) = 1.071\ \text{k}\Omega$

$Z_i = R_B \| \beta r_e = 470\ \text{k}\Omega \| 1.071\ \text{k}\Omega = \mathbf{1.07\ k\Omega}$

c. $Z_o = R_C = \mathbf{3\ k\Omega}$

d. $A_v = -\frac{R_C}{r_e} = -\frac{3\ \text{k}\Omega}{10.71\ \Omega} = \mathbf{-280.11}$

e. $Z_o = r_o \| R_C = 50\ \text{k}\Omega \| 3\ \text{k}\Omega = \mathbf{2.83\ k\Omega}$ vs. $3\ \text{k}\Omega$

$A_v = -\frac{r_o \| R_C}{r_e} = \frac{2.83\ \text{k}\Omega}{10.71\ \Omega} = \mathbf{-264.24}$ vs. -280.11

5.9 VOLTAGE-DIVIDER BIAS

The next configuration to be analyzed is the *voltage-divider* bias network of Fig. 5.40. Recall that the name of the configuration is a result of the voltage-divider bias at the input side to determine the dc level of V_B.

Substituting the r_e equivalent circuit results in the network of Fig. 5.41. Note the absence of R_E due to the low-impedance shorting effect of the bypass capacitor, C_E. That is, at the frequency (or frequencies) of operation, the reactance of the capacitor is so small compared to R_E that it is treated as a short circuit across R_E. When V_{CC} is set to zero, it places one end of R_1 and R_C at ground potential as shown in Fig. 5.41. In addition, note that R_1 and R_2 remain part of the input circuit while R_C is part of the output circuit. The parallel combination of R_1 and R_2 is defined by

$$R' = R_1 \| R_2 = \frac{R_1 R_2}{R_1 + R_2} \tag{5.33}$$

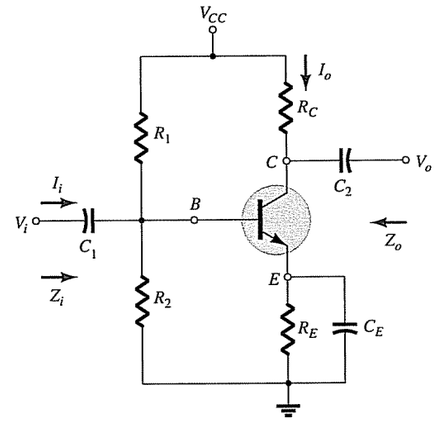


FIG. 5.40
Voltage-divider bias configuration.

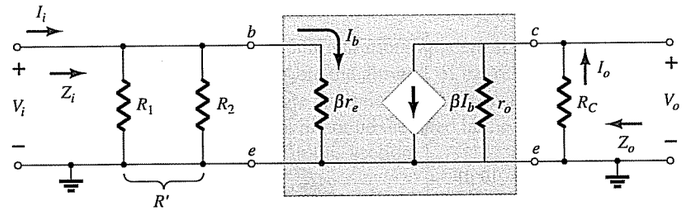


FIG. 5.41
Substituting the r_e equivalent circuit into the ac equivalent network of Fig. 5.40.

$\boldsymbol{Z_i}$ From Fig. 5.41

$$Z_i = R' \| \beta r_e \tag{5.34}$$

$\boldsymbol{Z_o}$ From Fig. 5.41 with V_i set to 0 V, resulting in $I_b = 0\ \mu\text{A}$ and $\beta I_b = 0\ \text{mA}$,

$$Z_o = R_C \| r_o \tag{5.35}$$

If $r_o \geq 10R_C$,

$$Z_o \cong R_C \quad (r_o \geq 10R_C) \tag{5.36}$$

$\boldsymbol{A_v}$ Since R_C and r_o are in parallel,

$$V_o = -(\beta I_b)(R_C \| r_o)$$

and

$$I_b = \frac{V_i}{\beta r_e}$$

so that

$$V_o = -\beta\left(\frac{V_i}{\beta r_e}\right)(R_C \| r_o)$$

and

$$A_v = \frac{V_o}{V_i} = \frac{-R_C \| r_o}{r_e} \tag{5.37}$$

which you will note is an exact duplicate of the equation obtained for the fixed-bias configuration.

For $r_o \geq 10R_C$,

$$A_v = \frac{V_o}{V_i} \cong -\frac{R_C}{r_e} \qquad r_o \geq 10R_C \qquad \textbf{(5.38)}$$

Phase Relationship The negative sign of Eq. (5.37) reveals a 180° phase shift between V_o and V_i.

EXAMPLE 5.5 For the network of Fig. 5.42, determine:

a. r_e.
b. Z_i.
c. Z_o ($r_o = \infty\,\Omega$).
d. A_v ($r_o = \infty\,\Omega$).
e. The parameters of parts (b) through (d) if $r_o = 1/h_{oe} = 50\,\text{k}\Omega$ and compare results.

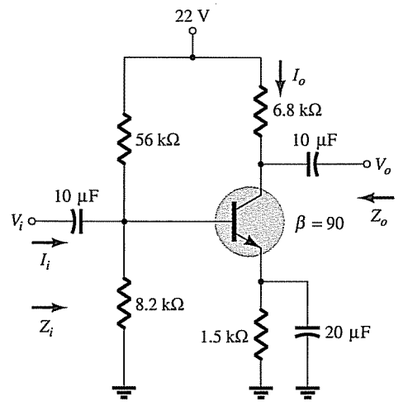


FIG. 5.42
Example 5.5.

Solution:

a. DC: Testing $\beta R_E > 10R_2$,

$$(90)(1.5\,\text{k}\Omega) > 10(8.2\,\text{k}\Omega)$$
$$135\,\text{k}\Omega > 82\,\text{k}\Omega \ (\textit{satisfied})$$

Using the approximate approach, we obtain

$$V_B = \frac{R_2}{R_1 + R_2}V_{CC} = \frac{(8.2\,\text{k}\Omega)(22\,\text{V})}{56\,\text{k}\Omega + 8.2\,\text{k}\Omega} = 2.81\,\text{V}$$
$$V_E = V_B - V_{BE} = 2.81\,\text{V} - 0.7\,\text{V} = 2.11\,\text{V}$$
$$I_E = \frac{V_E}{R_E} = \frac{2.11\,\text{V}}{1.5\,\text{k}\Omega} = 1.41\,\text{mA}$$
$$r_e = \frac{26\,\text{mV}}{I_E} = \frac{26\,\text{mV}}{1.41\,\text{mA}} = \mathbf{18.44\,\Omega}$$

b. $R' = R_1 \| R_2 = (56\,\text{k}\Omega)\|(8.2\,\text{k}\Omega) = 7.15\,\text{k}\Omega$
$Z_i = R' \| \beta r_e = 7.15\,\text{k}\Omega \| (90)(18.44\,\Omega) = 7.15\,\text{k}\Omega \| 1.66\,\text{k}\Omega$
$= \mathbf{1.35\,k\Omega}$

c. $Z_o = R_C = \mathbf{6.8\,k\Omega}$

d. $A_v = -\dfrac{R_C}{r_e} = -\dfrac{6.8\,\text{k}\Omega}{18.44\,\Omega} = \mathbf{-368.76}$

e. $Z_i = \mathbf{1.35\,k\Omega}$
$Z_o = R_C \| r_o = 6.8\,\text{k}\Omega \| 50\,\text{k}\Omega = \mathbf{5.98\,k\Omega}$ vs. $6.8\,\text{k}\Omega$
$A_v = -\dfrac{R_C \| r_o}{r_e} = -\dfrac{5.98\,\text{k}\Omega}{18.44\,\Omega} = \mathbf{-324.3}$ vs. -368.76

There was a measurable difference in the results for Z_o and A_v, because the condition $r_o \geq 10R_C$ was *not* satisfied.

5.10 CE EMITTER-BIAS CONFIGURATION

The networks examined in this section include an emitter resistor that may or may not be bypassed in the ac domain. We first consider the unbypassed situation and then modify the resulting equations for the bypassed configuration.

Unbypassed

The most fundamental of unbypassed configurations appears in Fig. 5.43. The r_e equivalent model is substituted in Fig. 5.44, but note the absence of the resistance r_o. The effect of r_o is to make the analysis a great deal more complicated, and considering the fact that in most situations its effect can be ignored, it will not be included in the present analysis. However, the effect of r_o will be discussed later in this section.

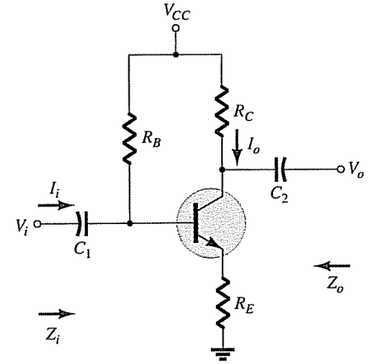


FIG. 5.43
CE emitter-bias configuration.

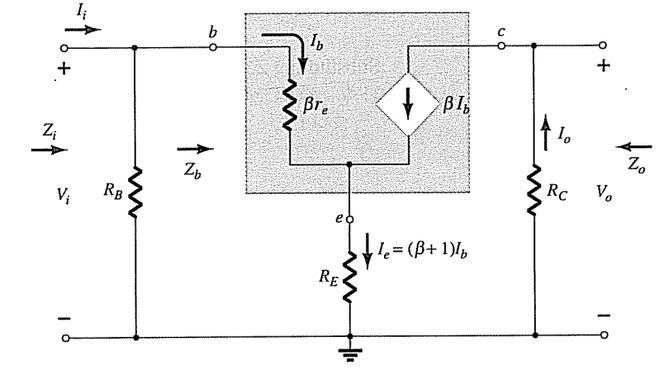


FIG. 5.44
Substituting the r_e equivalent circuit into the ac equivalent network of Fig. 5.43.

Applying Kirchhoff's voltage law to the input side of Fig. 5.44 results in

$$V_i = I_b\beta r_e + I_e R_E$$

or

$$V_i = I_b\beta r_e + (\beta + I)I_b R_E$$

and the input impedance looking into the network to the right of R_B is

$$Z_b = \frac{V_i}{I_b} = \beta r_e + (\beta + 1)R_E$$

The result as displayed in Fig. 5.45 reveals that the input impedance of a transistor with an unbypassed resistor R_E is determined by

$$\boxed{Z_b = \beta r_e + (\beta + 1)R_E} \qquad \textbf{(5.39)}$$

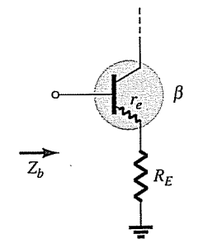


FIG. 5.45
Defining the input impedance of a transistor with an unbypassed emitter resistor.

Since β is normally much greater than 1, the approximate equation is

$$Z_b \cong \beta r_e + \beta R_E$$

and

$$\boxed{Z_b \cong \beta(r_e + R_E)} \tag{5.40}$$

Since R_E is often much greater than r_e, Eq. (5.40) can be further reduced to

$$\boxed{Z_b \cong \beta R_E} \tag{5.41}$$

Z_i Returning to Fig. 5.44, we have

$$\boxed{Z_i = R_B \| Z_b} \tag{5.42}$$

Z_o With V_i set to zero, $I_b = 0$, and βI_b can be replaced by an open-circuit equivalent. The result is

$$\boxed{Z_o = R_C} \tag{5.43}$$

A_v

$$I_b = \frac{V_i}{Z_b}$$

and

$$V_o = -I_o R_C = -\beta I_b R_C$$
$$= -\beta\left(\frac{V_i}{Z_b}\right)R_C$$

with

$$\boxed{A_v = \frac{V_o}{V_i} = -\frac{\beta R_C}{Z_b}} \tag{5.44}$$

Substituting $Z_b = \beta(r_e + R_E)$ gives

$$\boxed{A_v = \frac{V_o}{V_i} = -\frac{R_C}{r_e + R_E}} \tag{5.45}$$

and for the approximation $Z_b \cong \beta R_E$,

$$\boxed{A_v = \frac{V_o}{V_i} \cong -\frac{R_C}{R_E}} \tag{5.46}$$

Note again the absence of β from the equation for A_v.

Phase Relationship The negative sign in Eq. (5.44) again reveals a 180° phase shift between V_o and V_i.

Effect of *r_o* The equations appearing below will clearly reveal the additional complexity resulting from including r_o in the analysis. Note in each case, however, that when certain conditions are met, the equations return to the form just derived. The derivation of each equation is beyond the needs of this text and is left as an exercise for the reader. Each equation can be derived through *careful* application of the basic laws of circuit analysis such as Kirchhoff's voltage and current laws, source conversions. Thévenin's theorem, and so on. The equations were included to remove the nagging question of the effect of r_o on the important parameters of a transistor configuration.

Z_i

$$\boxed{Z_b = \beta r_e + \left[\frac{(\beta + 1) + R_C/r_o}{1 + (R_C + R_E)/r_o}\right]R_E} \tag{5.47}$$

Since the ratio R_C/r_o is always much less than $(\beta + 1)$,

$$Z_b \cong \beta r_e + \frac{(\beta + 1)R_E}{1 + (R_C + R_E)/r_o}$$

For $r_o \geq 10(R_C + R_E)$,

$$Z_b \cong \beta r_e + (\beta + 1)R_E$$

which compares directly with Eq. (5.39).

In other words, if $r_o \geq 10(R_C + R_E)$, all the equations derived earlier result. Since $\beta + 1 \cong \beta$, the following equation is an excellent one for most applications:

$$\boxed{Z_b \cong \beta(r_e + R_E)}_{r_o \geq 10(R_C + R_E)} \tag{5.48}$$

Z_o

$$\boxed{Z_o = R_C \| \left[r_o + \frac{\beta(r_o + r_e)}{1 + \dfrac{\beta r_e}{R_E}} \right]} \tag{5.49}$$

However, $r_o \gg r_e$, and

$$Z_o \cong R_C \| r_o \left[1 + \frac{\beta}{1 + \dfrac{\beta r_e}{R_E}} \right]$$

which can be written as

$$Z_o \cong R_C \| r_o \left[1 + \frac{1}{\dfrac{1}{\beta} + \dfrac{r_e}{R_E}} \right]$$

Typically $1/\beta$ and r_e/R_E are less than one with a sum usually less than one. The result is a multiplying factor for r_o greater than one. For $\beta = 100$, $r_e = 10\ \Omega$, and $R_E = 1\ \text{k}\Omega$,

$$\frac{1}{\dfrac{1}{\beta} + \dfrac{r_e}{R_E}} = \frac{1}{\dfrac{1}{100} + \dfrac{10\ \Omega}{1000\ \Omega}} = \frac{1}{0.02} = 50$$

and

$$Z_o = R_C \| 51 r_o$$

which is certainly simply R_C. Therefore,

$$\boxed{Z_o \cong R_C}_{\text{Any level of } r_o} \tag{5.50}$$

which was obtained earlier.

A_v

$$\boxed{A_v = \frac{V_o}{V_i} = \frac{-\dfrac{\beta R_C}{Z_b}\left[1 + \dfrac{r_e}{r_o}\right] + \dfrac{R_C}{r_o}}{1 + \dfrac{R_C}{r_o}}} \tag{5.51}$$

The ratio $\dfrac{r_e}{r_o} \ll 1$, and

$$A_v = \frac{V_o}{V_i} \cong \frac{-\dfrac{\beta R_C}{Z_b} + \dfrac{R_C}{r_o}}{1 + \dfrac{R_C}{r_o}}$$

For $r_o \geq 10R_C$,

$$A_v = \frac{V_o}{V_i} \cong -\frac{\beta R_C}{Z_b} \qquad r_o \geq 10R_C \qquad (5.52)$$

as obtained earlier.

Bypassed

If R_E of Fig. 5.43 is bypassed by an emitter capacitor C_E, the complete r_e equivalent model can be substituted, resulting in the same equivalent network as Fig. 5.36. Equations (5.27) to (5.32) are therefore applicable.



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EXAMPLE 5.6 For the network of Fig. 5.46, without C_E (unbypassed), determine:

a. r_e.
b. Z_i.
c. Z_o.
d. A_v.

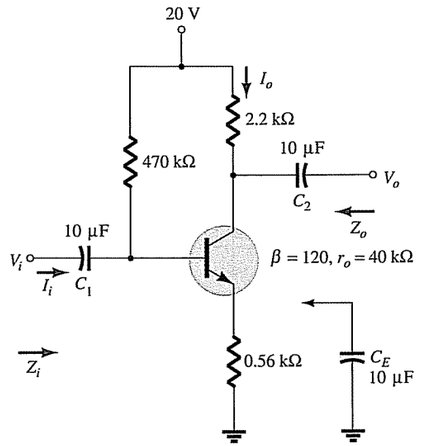


FIG. 5.46
Example 5.6.

Solution:

a. DC:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{20\,\text{V} - 0.7\,\text{V}}{470\,\text{k}\Omega + (121)0.56\,\text{k}\Omega} = 35.89\,\mu\text{A}$$

$$I_E = (\beta + 1)I_B = (121)(35.89\,\mu\text{A}) = 4.34\,\text{mA}$$

and $$r_e = \frac{26\,\text{mV}}{I_E} = \frac{26\,\text{mV}}{4.34\,\text{mA}} = \mathbf{5.99\,\Omega}$$

b. Testing the condition $r_o \geq 10(R_C + R_E)$, we obtain

$$40\,\text{k}\Omega \geq 10(2.2\,\text{k}\Omega + 0.56\,\text{k}\Omega)$$

$$40\,\text{k}\Omega \geq 10(2.76\,\text{k}\Omega) = 27.6\,\text{k}\Omega \ (\textit{satisfied})$$

Therefore,

$$Z_b \cong \beta(r_e + R_E) = 120(5.99\,\Omega + 560\,\Omega)$$

$$= 67.92\,\text{k}\Omega$$

and

$$Z_i = R_B \| Z_b = 470\,\text{k}\Omega \| 67.92\,\text{k}\Omega$$

$$= \mathbf{59.34\,k\Omega}$$

c. $Z_o = R_C = \mathbf{2.2\,k\Omega}$

d. $r_o \geq 10R_C$ is satisfied. Therefore,

$$A_v = \frac{V_o}{V_i} \cong -\frac{\beta R_C}{Z_b} = -\frac{(120)(2.2\,\text{k}\Omega)}{67.92\,\text{k}\Omega}$$

$$= \mathbf{-3.89}$$

compared to -3.93 using Eq. (5.46): $A_v \cong -R_C/R_E$.

Mathcad

The lengthy equations resulting from the analysis of the CE emitter-bias configuration demonstrate the value of becoming proficient in the use of the Mathcad software package.

Priorities do not permit a detailed description of each step of the process, but a few general comments can be made. First, all the parameters of the network that will appear in the equations must be defined as shown in Fig. 5.47. Next, the equations for each of the desired quantities are entered, being very careful to include parentheses in the proper places to ensure that the resulting equation is correct. Actually, more parentheses appear than necessary, but an effort was made to make the equations look as much like those in the text as possible. After each equation is defined, its value can be determined by simply entering the variable name again and pressing the equal sign. This is shown to the right of each equation

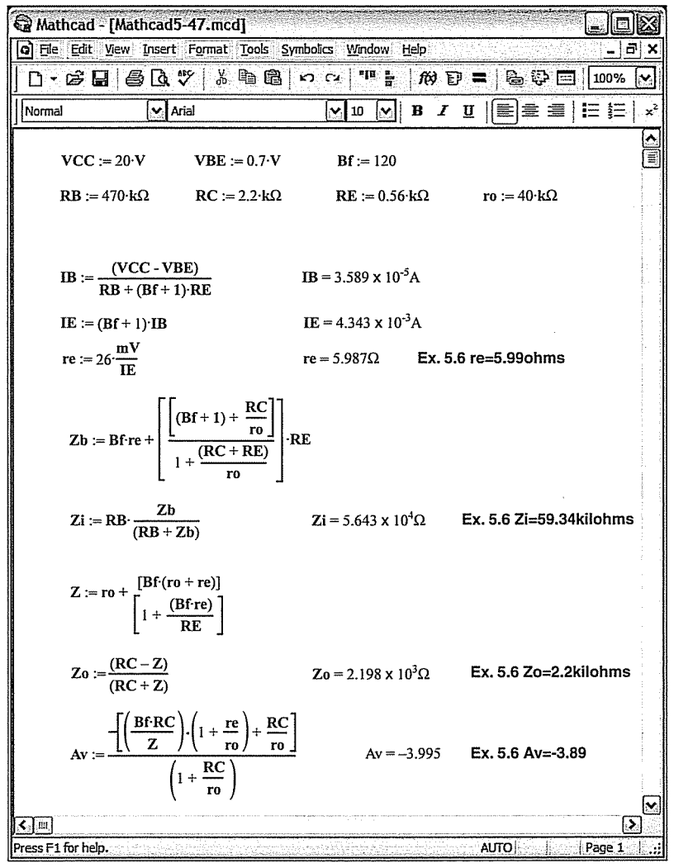


FIG. 5.47
Network parameters and equations for Example 5.6.

at a level just below the defining equation. For the base current, for example, once **IB** is entered and the equal sign pressed, the base current of 35.89 μA will appear. Note as you progress down the page that as a variable is determined, it can be used in the equations to follow. In fact, it is a necessary sequence if the continuing line of equations is to have the specific numbers to deal with.

For each of the quantities calculated, a text message is added to permit a comparison with the results of Example 5.6. There is excellent correspondence between results when one considers that a number of approximations were used in Example 5.6. The largest difference occurs for the input impedance, which has a lengthy equation for **Zb**. That difference is reflected in the current gain, which has a greater difference than that obtained for the output impedance and voltage gain.

The real beauty of having entered all these equations properly is that the file can be saved and recalled at any time. As the parameters appearing on the first two lines are changed, all the quantities on the following lines will be recalculated—there is no need to reenter any of the equations, and this sequence even does the dc analysis before determining the ac response.

EXAMPLE 5.7 Repeat the analysis of Example 5.6 with C_E in place.

Solution:

a. The dc analysis is the same, and $r_e = 5.99\ \Omega$.

b. R_E is "shorted out" by C_E for the ac analysis. Therefore,

$$Z_i = R_B \| Z_b = R_B \| \beta r_e = 470\,\text{k}\Omega \| (120)(5.99\ \Omega)$$
$$= 470\,\text{k}\Omega \| 718.8\ \Omega \cong \mathbf{717.70\ \Omega}$$

c. $Z_o = R_C = \mathbf{2.2\,k\Omega}$

d. $$A_v = -\frac{R_C}{r_e}$$
$$= -\frac{2.2\,\text{k}\Omega}{5.99\ \Omega} = \mathbf{-367.28}\ \text{(a significant increase)}$$

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EXAMPLE 5.8 For the network of Fig. 5.48, determine (using appropriate approximations):

a. r_e.
b. Z_i.
c. Z_o.
d. A_v.

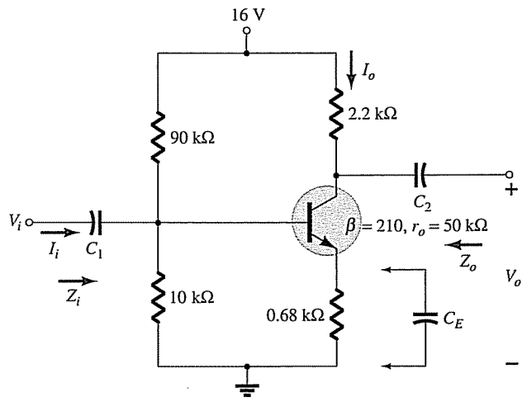


FIG. 5.48
Example 5.3.

Solution:

a. Testing $\beta R_E > 10R_2$,

$$(210)(0.68\,\text{k}\Omega) > 10(10\,\text{k}\Omega)$$
$$142.8\,\text{k}\Omega > 100\,\text{k}\Omega\ (\textit{satisfied})$$

we have

$$V_B = \frac{R_2}{R_1 + R_2} V_{CC} = \frac{10\,\text{k}\Omega}{90\,\text{k}\Omega + 10\,\text{k}\Omega}(16\,\text{V}) = 1.6\,\text{V}$$
$$V_E = V_B - V_{BE} = 1.6\,\text{V} - 0.7\,\text{V} = 0.9\,\text{V}$$
$$I_E = \frac{V_E}{R_E} = \frac{0.9\,\text{V}}{0.68\,\text{k}\Omega} = 1.324\,\text{mA}$$
$$r_e = \frac{26\,\text{mV}}{I_E} = \frac{26\,\text{mV}}{1.324\,\text{mA}} = \mathbf{19.64\ \Omega}$$

b. The ac equivalent circuit is provided in Fig. 5.49. The resulting configuration is different from Fig. 5.44 only by the fact that now

$$R_B = R' = R_1 \| R_2 = 9\,\text{k}\Omega$$

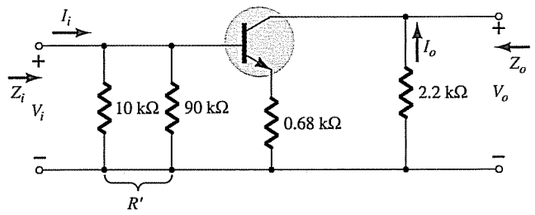


FIG. 5.49
The ac equivalent circuit of Fig. 5.48.

The testing conditions of $r_o \geq 10(R_C + R_E)$ and $r_o \geq 10R_C$ are both satisfied. Using the appropriate approximations yields

$$Z_b \cong \beta R_E = 142.8\,\text{k}\Omega$$
$$Z_i = R_B \| Z_b = 9\,\text{k}\Omega \| 142.8\,\text{k}\Omega$$
$$= \mathbf{8.47\,k\Omega}$$

c. $Z_o = R_C = \mathbf{2.2\,k\Omega}$

d. $$A_v = -\frac{R_C}{R_E} = -\frac{2.2\,\text{k}\Omega}{0.68\,\text{k}\Omega} = \mathbf{-3.24}$$

EXAMPLE 5.9 Repeat Example 5.8 with C_E in place.

Solution:

a. The dc analysis is the same, and $r_e = \mathbf{19.64\ \Omega}$.

b. $$Z_b = \beta r_e = (210)(19.64\ \Omega) \cong 4.12\,\text{k}\Omega$$
$$Z_i = R_B \| Z_b = 9\,\text{k}\Omega \| 4.12\,\text{k}\Omega$$
$$= \mathbf{2.83\,k\Omega}$$

c. $Z_o = R_C = \mathbf{2.2\,k\Omega}$

d. $$A_v = -\frac{R_C}{r_e} = -\frac{2.2\,\text{k}\Omega}{19.64\,\Omega} = \mathbf{-112.02}\ \text{(a significant increase)}$$

Another variation of an emitter-bias configuration is shown in Fig. 5.50. For the dc analysis, the emitter resistance is $R_{E_1} + R_{E_2}$, whereas for the ac analysis, the resistor R_E in the equations above is simply R_{E_1} with R_{E_2} bypassed by C_E.

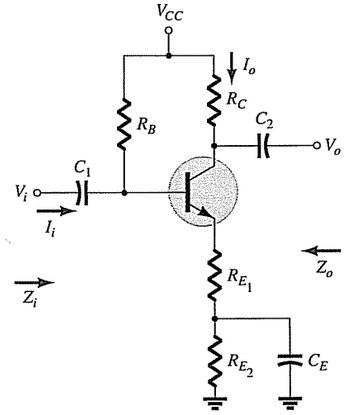


FIG. 5.50
An emitter-bias configuration with a portion of the emitter-bias resistance bypassed in the ac domain.

5.11 EMITTER-FOLLOWER CONFIGURATION

When the output is taken from the emitter terminal of the transistor as shown in Fig. 5.51, the network is referred to as an *emitter-follower*. The output voltage is always slightly less than the input signal due to the drop from base to emitter, but the approximation $A_v \cong 1$ is usually a good one. Unlike the collector voltage, the emitter voltage is in phase with the signal V_i. That is, both V_o and V_i attain their positive and negative peak values at the same time. The fact that V_o "follows" the magnitude of V_i with an in-phase relationship accounts for the terminology emitter-follower.

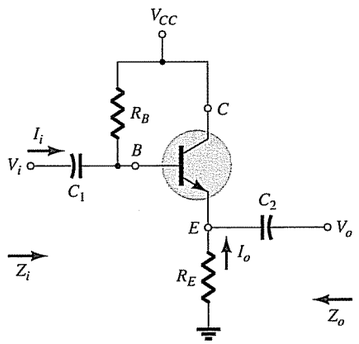


FIG. 5.51
Emitter-follower configuration.

The most common emitter-follower configuration appears in Fig. 5.51. In fact, because the collector is grounded for ac analysis, it is actually a *common-collector* configuration. Other variations of Fig. 5.51 that draw the output off the emitter with $V_o \cong V_i$ will appear later in this section.

The emitter-follower configuration is frequently used for impedance-matching purposes. It presents a high impedance at the input and a low impedance at the output, which is the direct opposite of the standard fixed-bias configuration. The resulting effect is much the same as that obtained with a transformer, where a load is matched to the source impedance for maximum power transfer through the system.

Substituting the r_e equivalent circuit into the network of Fig. 5.51 results in the network of Fig. 5.52. The effect of r_o will be examined later in the section:

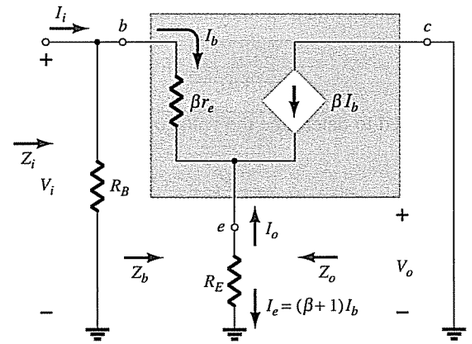


FIG. 5.52
Substituting the r_e equivalent circuit into the ac equivalent network of Fig. 5.51.

Z_i The input impedance is determined in the same manner as described in the preceding section:

$$Z_i = R_B \| Z_b \tag{5.53}$$

with

$$Z_b = \beta r_e + (\beta + 1) R_E \tag{5.54}$$

or

$$Z_b \cong \beta (r_e + R_E) \tag{5.55}$$

and

$$Z_b \cong \beta R_E \quad {}_{R_E \gg r_e} \tag{5.56}$$

Z_o The output impedance is best described by first writing the equation for the current I_b,

$$I_b = \frac{V_i}{Z_b}$$

and then multiplying by $(\beta + 1)$ to establish I_e. That is,

$$I_e = (\beta + 1) I_b = (\beta + 1) \frac{V_i}{Z_b}$$

Substituting for Z_b gives

$$I_e = \frac{(\beta + 1) V_i}{\beta r_e + (\beta + 1) R_E}$$

or

$$I_e = \frac{V_i}{[\beta r_e / (\beta + 1)] + R_E}$$

but

$$(\beta + 1) \cong \beta$$

and

$$\frac{\beta r_e}{\beta + 1} \cong \frac{\beta r_e}{\beta} = r_e$$

so that

$$I_e \cong \frac{V_i}{r_e + R_E} \tag{5.57}$$

If we now construct the network defined by Eq. (5.57), the configuration of Fig. 5.53 results.

To determine Z_o, V_i is set to zero and

$$Z_o = R_E \| r_e \tag{5.58}$$

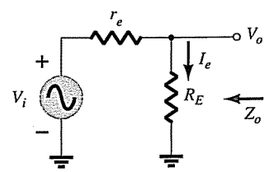


FIG. 5.53
Defining the output impedance for the emitter-follower configuration.

Since R_E is typically much greater than r_e, the following approximation is often applied:

$$\boxed{Z_o \cong r_e} \tag{5.59}$$

A_v Figure 5.53 can be used to determine the voltage gain through an application of the voltage-divider rule:

$$V_o = \frac{R_E V_i}{R_E + r_e}$$

and

$$\boxed{A_v = \frac{V_o}{V_i} = \frac{R_E}{R_E + r_e}} \tag{5.60}$$

Since R_E is usually much greater than r_e, $R_E + r_e \cong R_E$ and

$$\boxed{A_v = \frac{V_o}{V_i} \cong 1} \tag{5.61}$$

Phase Relationship As revealed by Eq. (5.60) and earlier discussions of this section, V_o and V_i are in phase for the emitter-follower configuration.

Effect of r_o

Z_i

$$\boxed{Z_b = \beta r_e + \frac{(\beta + 1)R_E}{1 + \frac{R_E}{r_o}}} \tag{5.62}$$

If the condition $r_o \geq 10R_E$ is satisfied,

$$Z_b = \beta r_e + (\beta + 1)R_E$$

which matches earlier conclusions with

$$\boxed{Z_b \cong \beta(r_e + R_E)}_{r_o \geq 10R_E} \tag{5.63}$$

Z_o

$$\boxed{Z_o = r_o \| R_E \| \frac{\beta r_e}{(\beta + 1)}} \tag{5.64}$$

Using $\beta + 1 \cong \beta$, we obtain

$$Z_o = r_o \| R_E \| r_e$$

and since $r_o \gg r_e$,

$$\boxed{Z_o \cong R_E \| r_e}_{\text{Any } r_o} \tag{5.65}$$

A_v

$$\boxed{A_v = \frac{(\beta + 1)R_E / Z_b}{1 + \frac{R_E}{r_o}}} \tag{5.66}$$

If the condition $r_o \geq 10R_E$ is satisfied and we use the approximation $\beta + 1 \cong \beta$, we find

$$A_v \cong \frac{\beta R_E}{Z_b}$$

But

$$Z_b \cong \beta(r_e + R_E)$$

so that

$$A_v \cong \frac{\beta R_E}{\beta(r_e + R_E)}$$

and

$$\boxed{A_v \cong \frac{R_E}{r_e + R_E}}_{r_o \geq 10R_E} \tag{5.67}$$

EXAMPLE 5.10 For the emitter-follower network of Fig. 5.54, determine:

a. r_e.
b. Z_i.
c. Z_o.
d. A_v.
e. Repeat parts (b) through (d) with $r_o = 25\,\text{k}\Omega$ and compare results.

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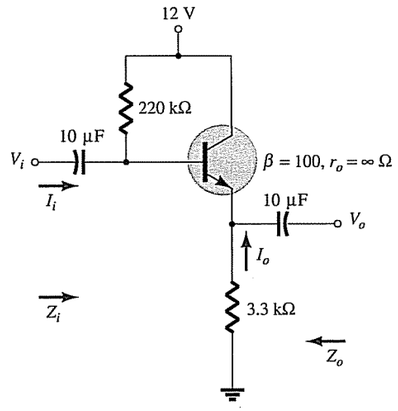


FIG. 5.54
Example 5.10.

Solution:

a. $$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$$
$$= \frac{12\,\text{V} - 0.7\,\text{V}}{220\,\text{k}\Omega + (101)3.3\,\text{k}\Omega} = 20.42\,\mu\text{A}$$
$$I_E = (\beta + 1)I_B$$
$$= (101)(20.42\,\mu\text{A}) = 2.062\,\text{mA}$$
$$r_e = \frac{26\,\text{mV}}{I_E} = \frac{26\,\text{mV}}{2.062\,\text{mA}} = \mathbf{12.61\ \Omega}$$

b. $$Z_b = \beta r_e + (\beta + 1)R_E$$
$$= (100)(12.61\,\Omega) + (101)(3.3\,\text{k}\Omega)$$
$$= 1.261\,\text{k}\Omega + 333.3\,\text{k}\Omega$$
$$= 334.56\,\text{k}\Omega \cong \beta R_E$$
$$Z_i = R_B \| Z_b = 220\,\text{k}\Omega \| 334.56\,\text{k}\Omega$$
$$= \mathbf{132.72\,k\Omega}$$

c. $$Z_o = R_E \| r_e = 3.3\,\text{k}\Omega \| 12.61\,\Omega$$
$$= \mathbf{12.56\ \Omega} \cong r_e$$

d. $$A_v = \frac{V_o}{V_i} = \frac{R_E}{R_E + r_e} = \frac{3.3\,\text{k}\Omega}{3.3\,\text{k}\Omega + 12.61\,\Omega}$$
$$= \mathbf{0.996} \cong \mathbf{1}$$

e. Checking the condition $r_o \geq 10R_E$, we have

$$25\,\text{k}\Omega \geq 10(3.3\,\text{k}\Omega) = 33\,\text{k}\Omega$$

which is *not* satisfied. Therefore,

$$Z_b = \beta r_e + \frac{(\beta + 1)R_E}{1 + \frac{R_E}{r_o}} = (100)(12.61\,\Omega) + \frac{(100 + 1)3.3\,\text{k}\Omega}{1 + \frac{3.3\,\text{k}\Omega}{25\,\text{k}\Omega}}$$

$$= 1.261\,\text{k}\Omega + 294.43\,\text{k}\Omega$$

$$= 295.7\,\text{k}\Omega$$

with $Z_i = R_B \| Z_b = 220\,\text{k}\Omega \| 295.7\,\text{k}\Omega$

$$= \mathbf{126.15\,k\Omega} \text{ vs. } 132.72\,\text{k}\Omega \quad \text{obtained earlier}$$

$$Z_o = R_E \| r_e = \mathbf{12.56\,\Omega} \quad \text{as obtained earlier}$$

$$A_v = \frac{(\beta + 1)R_E/Z_b}{\left[1 + \frac{R_E}{r_o}\right]} = \frac{(100 + 1)(3.3\,\text{k}\Omega)/295.7\,\text{k}\Omega}{\left[1 + \frac{3.3\,\text{k}\Omega}{25\,\text{k}\Omega}\right]}$$

$$= \mathbf{0.996} \cong \mathbf{1}$$

matching the earlier result.

In general, therefore, even though the condition $r_o \geq 10R_E$ is not satisfied, the results for Z_o and A_v are the same, with Z_i only slightly less. The results suggest that for most applications a good approximation for the actual results can be obtained by simply ignoring the effects of r_o for this configuration.

The network of Fig. 5.55 is a variation of the network of Fig. 5.51, which employs a voltage-divider input section to set the bias conditions. Equations (5.53) to (5.56) are changed only by replacing R_B by $R' = R_1 \| R_2$.

The network of Fig. 5.56 also provides the input/output characteristics of an emitter-follower, but includes a collector resistor R_C. In this case R_B is again replaced by the parallel combination of R_1 and R_2. The input impedance Z_i and output impedance Z_o are unaffected by R_C since it is not reflected into the base or emitter equivalent networks. In fact, the only effect of R_C is to determine the Q-point of operation.

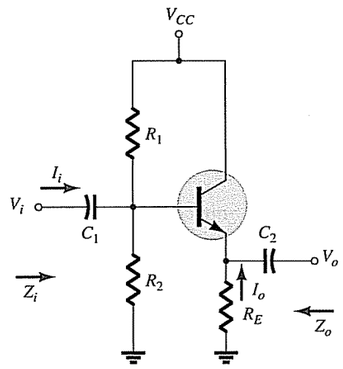


FIG. 5.55
Emitter-follower configuration with a voltage-divider biasing arrangement.

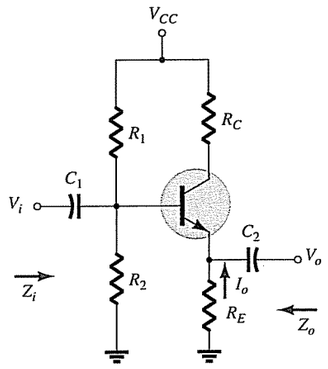


FIG. 5.56
Emitter-follower configuration with a collector resistor R_C.

5.12 COMMON-BASE CONFIGURATION

The common-base configuration is characterized as having a relatively low input and a high output impedance and a current gain less than 1. The voltage gain, however, can be quite large. The standard configuration appears in Fig. 5.57, with the common-base r_e equivalent model substituted in Fig. 5.58. The transistor output impedance r_o is not included for the common-base configuration because it is typically in the megohm range and can be ignored in parallel with the resistor R_C.

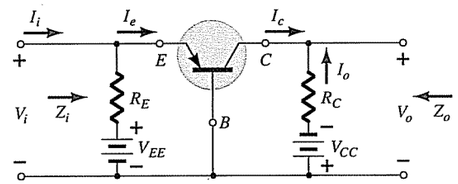


FIG. 5.57
Common-base configuration.

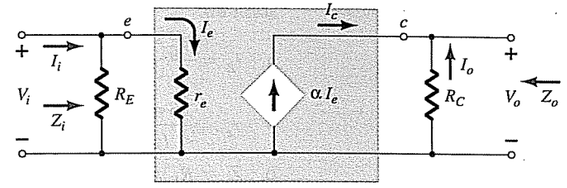


FIG. 5.58
Substituting the r_e equivalent circuit into the ac equivalent network of Fig. 5.57.

Z_i

$$\boxed{Z_i = R_E \| r_e} \tag{5.68}$$

Z_o

$$\boxed{Z_o = R_C} \tag{5.69}$$

A_v

$$V_o = -I_o R_C = -(-I_c)R_C = \alpha I_e R_C$$

with $$I_e = \frac{V_i}{r_e}$$

so that $$V_o = \alpha\left(\frac{V_i}{r_e}\right)R_C$$

and

$$\boxed{A_v = \frac{V_o}{V_i} = \frac{\alpha R_C}{r_e} \cong \frac{R_C}{r_e}} \tag{5.70}$$

A_i Assuming that $R_E \gg r_e$ yields

$$I_e = I_i$$

and $$I_o = -\alpha I_e = -\alpha I_i$$

with

$$\boxed{A_i = \frac{I_o}{I_i} = -\alpha \cong -1} \tag{5.71}$$

Phase Relationship The fact that A_v is a positive number shows that V_o and V_i are in phase for the common-base configuration.

Effect of r_o For the common-base configuration, $r_o = 1/h_{ob}$ is typically in the megohm range and sufficiently larger than the parallel resistance R_C to permit the approximation $r_o \| R_C \cong R_C$.

EXAMPLE 5.11 For the network of Fig. 5.59, determine:

a. r_e.
b. Z_i.
c. Z_o.
d. A_v.
e. A_i.

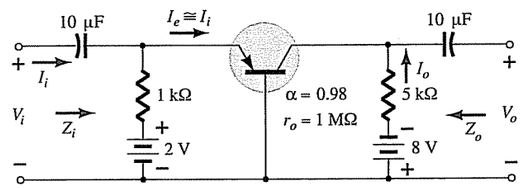


FIG. 5.59
Example 5.11.

Solution:

a. $I_E = \dfrac{V_{EE} - V_{BE}}{R_E} = \dfrac{2\text{ V} - 0.7\text{ V}}{1\text{ k}\Omega} = \dfrac{1.3\text{ V}}{1\text{ k}\Omega} = 1.3\text{ mA}$

$$r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{1.3\text{ mA}} = \mathbf{20\ \Omega}$$

b. $Z_i = R_E \| r_e = 1\text{ k}\Omega \| 20\ \Omega$

$$= \mathbf{19.61\ \Omega} \cong r_e$$

c. $Z_o = R_C = \mathbf{5\text{ k}\Omega}$

d. $A_v \cong \dfrac{R_C}{r_e} = \dfrac{5\text{ k}\Omega}{20\ \Omega} = \mathbf{250}$

e. $A_i = \mathbf{-0.98} \cong -1$

5.13 COLLECTOR FEEDBACK CONFIGURATION

The collector feedback network of Fig. 5.60 employs a feedback path from collector to base to increase the stability of the system as discussed in Section 4.6. However, the simple maneuver of connecting a resistor from base to collector rather than base to dc supply has a significant effect on the level of difficulty encountered when analyzing the network.

Some of the steps to be performed below are the result of experience working with such configurations. It is not expected that a new student of the subject would choose the sequence of steps described below without taking a wrong step or two. Substituting the equivalent circuit and redrawing the network results in the configuration of Fig. 5.61. The effects of a transistor output resistance r_o will be discussed later in the section.

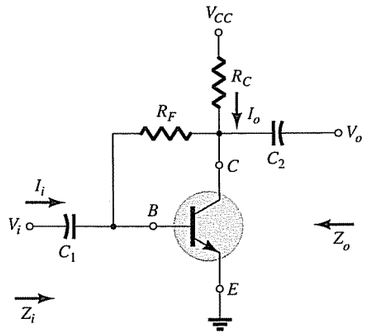


FIG. 5.60
Collector feedback configuration.

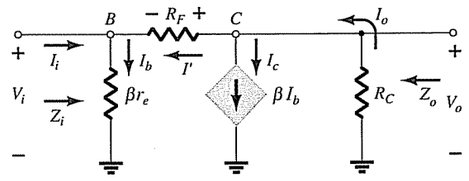


FIG. 5.61
Substituting the r_e equivalent circuit into the ac equivalent network of Fig. 5.60.

Z_i

$$I' = \frac{V_o - V_i}{R_F}$$

with $V_o = -I_o R_C$

and $I_o = \beta I_b + I'$

Since βI_b is normally much larger than I',

$$I_o \cong \beta I_b$$

and $V_o = -(\beta I_b)R_C = -\beta I_b R_C$

but $I_b = \dfrac{V_i}{\beta r_e}$

and $V_o = -\beta\left(\dfrac{V_i}{\beta r_e}\right)R_C = -\dfrac{R_C}{r_e}V_i$

Therefore,

$$I' = \frac{V_o - V_i}{R_F} = \frac{V_o}{R_F} - \frac{V_i}{R_F} = -\frac{R_C V_i}{r_e R_F} - \frac{V_i}{R_F} = -\frac{1}{R_F}\left[1 + \frac{R_C}{r_e}\right]V_i$$

The result is

$$V_i = I_b\beta r_e = (I_i + I')\beta r_e = I_i\beta r_e + I'\beta r_e$$

$$V_i = I_i\beta r_e - \frac{1}{R_F}\left[1 + \frac{R_C}{r_e}\right]\beta r_e V_i$$

or

$$V_i\left[1 + \frac{\beta r_e}{R_F}\left[1 + \frac{R_C}{r_e}\right]\right] = I_i\beta r_e$$

and

$$Z_i = \frac{V_i}{I_i} = \frac{\beta r_e}{1 + \dfrac{\beta r_e}{R_F}\left[1 + \dfrac{R_C}{r_e}\right]}$$

but R_C is usually much greater than r_e, and

$$1 + \frac{R_C}{r_e} \cong \frac{R_C}{r_e}$$

so that

$$Z_i = \frac{\beta r_e}{1 + \dfrac{\beta R_C}{R_F}}$$

or

$$\boxed{Z_i = \frac{r_e}{\dfrac{1}{\beta} + \dfrac{R_C}{R_F}}} \qquad \textbf{(5.72)}$$

Z_o If we set V_i to zero as required to define Z_o, the network will appear as shown in Fig. 5.62. The effect of βr_e is removed and R_F appears in parallel with R_C and

$$\boxed{Z_o \cong R_C \| R_F} \qquad \textbf{(5.73)}$$

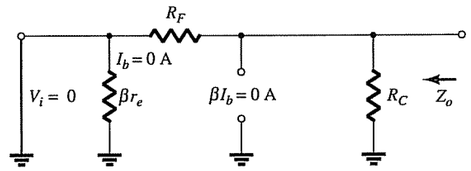


FIG. 5.62
Defining Z_o for the collector feedback configuration.

A_v At node C of Fig. 5.61,

$$I_o = \beta I_b + I'$$

For typical values, $\beta I_b \gg I'$ and $I_o \cong \beta I_b$. We have

$$V_o = -I_o R_C = -(\beta I_b)R_C$$

Substituting $I_b = V_i/\beta r_e$ gives

$$V_o = -\beta\frac{V_i}{\beta r_e}R_C$$

and

$$\boxed{A_v = \frac{V_o}{V_i} = -\frac{R_C}{r_e}} \qquad \textbf{(5.74)}$$

Phase Relationship The negative sign of Eq. (5.74) indicates a 180° phase shift between V_o and V_i.

Effect of r_o

Z_i A complete analysis without applying approximations results in

$$Z_i = \frac{1 + \dfrac{R_C \| r_o}{R_F}}{\dfrac{1}{\beta r_e} + \dfrac{1}{R_F} + \dfrac{R_C \| r_o}{R_F r_e}} \tag{5.75}$$

Recognizing that $1/R_F \cong 0$ and applying the condition $r_o \geq 10R_C$, we obtain

$$Z_i = \frac{1 + \dfrac{R_C}{R_F}}{\dfrac{1}{\beta r_e} + \dfrac{R_C}{R_F r_e}}$$

but typically $R_C/R_F \ll 1$, and

$$Z_i = \frac{1}{\dfrac{1}{\beta r_e} + \dfrac{R_C}{R_F r_e}}$$

or

$$Z_i \cong \frac{r_e}{\dfrac{1}{\beta} + \dfrac{R_C}{R_F}} \qquad r_o \geq 10R_C \tag{5.76}$$

as obtained earlier.

Z_o Including r_o in parallel with R_C in Fig. 5.62 results in

$$Z_o = r_o \| R_C \| R_F \tag{5.77}$$

For $r_o \geq 10R_C$,

$$Z_o \cong R_C \| R_F \qquad r_o \geq 10R_C \tag{5.78}$$

as obtained earlier. For the common condition of $R_F \gg R_C$,

$$Z_o \cong R_C \qquad r_o \geq 10R_C, R_F \gg R_C \tag{5.79}$$

A_v

$$A_v = -\frac{\left[\dfrac{1}{R_F} + \dfrac{1}{r_e}\right](r_o \| R_C)}{1 + \dfrac{r_o \| R_C}{R_F}} \tag{5.80}$$

Since $R_F \gg r_e$,

$$A_v \cong -\frac{\dfrac{r_o \| R_C}{r_e}}{1 + \dfrac{r_o \| R_C}{R_F}}$$

For $r_o \geq 10R_C$,

$$A_v \cong -\frac{\dfrac{R_C}{r_e}}{1 + \dfrac{R_C}{R_F}} \qquad r_o \geq 10R_C \tag{5.81}$$

and since R_C/R_F is typically much less than one,

$$A_v \cong -\frac{R_C}{r_e} \qquad r_o \geq 10R_C, R_F \gg R_C \tag{5.82}$$

as obtained earlier.

EXAMPLE 5.12 For the network of Fig. 5.63, determine:

a. r_e.
b. Z_i.
c. Z_o.
d. A_v.
e. Repeat parts (b) through (d) with $r_o = 20\,\text{k}\Omega$ and compare results.

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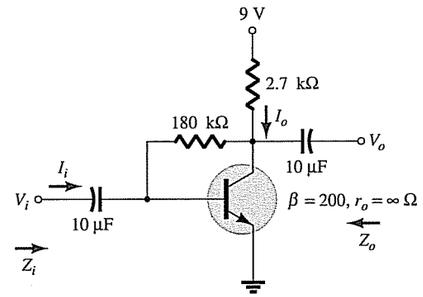


FIG. 5.63
Example 5.12.

Solution:

a. $$I_B = \frac{V_{CC} - V_{BE}}{R_F + \beta R_C} = \frac{9\,\text{V} - 0.7\,\text{V}}{180\,\text{k}\Omega + (200)2.7\,\text{k}\Omega}$$
$$= 11.53\,\mu\text{A}$$
$$I_E = (\beta + 1)I_B = (201)(11.53\,\mu\text{A}) = 2.32\,\text{mA}$$
$$r_e = \frac{26\,\text{mV}}{I_E} = \frac{26\,\text{mV}}{2.32\,\text{mA}} = \mathbf{11.21\,\Omega}$$

b. $$Z_i = \frac{r_e}{\dfrac{1}{\beta} + \dfrac{R_C}{R_F}} = \frac{11.21\,\Omega}{\dfrac{1}{200} + \dfrac{2.7\,\text{k}\Omega}{180\,\text{k}\Omega}} = \frac{11.21\,\Omega}{0.005 + 0.015}$$
$$= \frac{11.21\Omega}{0.02} = 50(11.21\,\Omega) = \mathbf{560.5\,\Omega}$$

c. $Z_o = R_C \| R_F = 2.7\,\text{k}\Omega \| 180\,\text{k}\Omega = \mathbf{2.66\,\text{k}\Omega}$

d. $$A_v = -\frac{R_C}{r_e} = -\frac{27\,\text{k}\Omega}{11.21\,\Omega} = \mathbf{-240.86}$$

e. Z_i: The condition $r_o \geq 10R_C$ is *not* satisfied. Therefore,

$$Z_i = \frac{1 + \dfrac{R_C \| r_o}{R_F}}{\dfrac{1}{\beta r_e} + \dfrac{1}{R_F} + \dfrac{R_C \| r_o}{R_F r_e}} = \frac{1 + \dfrac{2.7\,\text{k}\Omega \| 20\,\text{k}\Omega}{180\,\text{k}\Omega}}{\dfrac{1}{(200)(11.21)} + \dfrac{1}{180\,\text{k}\Omega} + \dfrac{2.7\,\text{k}\Omega \| 20\,\text{k}\Omega}{(180\,\text{k}\Omega)(11.21\,\Omega)}}$$
$$= \frac{1 + \dfrac{2.38\,\text{k}\Omega}{180\,\text{k}\Omega}}{0.45 \times 10^{-3} + 0.006 \times 10^{-3} + 1.18 \times 10^{-3}} = \frac{1 + 0.013}{1.64 \times 10^{-3}}$$
$$= \mathbf{617.7\,\Omega}\ \text{vs. } 560.5\,\Omega \text{ above}$$

Z_o:

$$Z_o = r_o \| R_C \| R_F = 20\,\text{k}\Omega \| 2.7\,\text{k}\Omega \| 180\,\text{k}\Omega$$
$$= \mathbf{2.35\,k\Omega} \text{ vs. } 2.66\,\text{k}\Omega \text{ above}$$

A_v:

$$A_v = \frac{-\left[\frac{1}{R_F} + \frac{1}{r_e}\right](r_o \| R_C)}{1 + \frac{r_o \| R_C}{R_F}} = \frac{-\left[\frac{1}{180\,\text{k}\Omega} + \frac{1}{11.21\Omega}\right](2.38\,\text{k}\Omega)}{1 + \frac{2.38\,\text{k}\Omega}{180\,\text{k}\Omega}}$$
$$= \frac{-[5.56 \times 10^{-6} - 8.92 \times 10^{-2}](2.38\,\text{k}\Omega)}{1 + 0.013}$$
$$= \mathbf{-209.56} \text{ vs. } -240.86 \text{ above}$$

For the configuration of Fig. 5.64, Eqs. (5.83) through (5.86) determine the variables of interest. The derivations are left as an exercise at the end of the chapter.

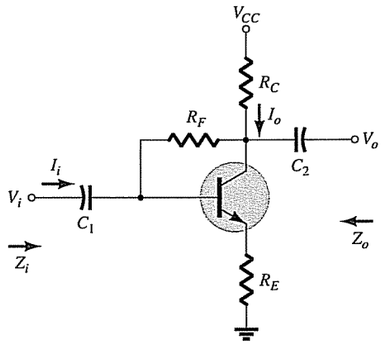


FIG. 5.64
Collector feedback configuration with an emitter resistor R_E.

Z_i

$$Z_i \cong \frac{R_E}{\left[\frac{1}{\beta} + \frac{(R_E + R_C)}{R_F}\right]} \tag{5.83}$$

Z_o

$$Z_o = R_C \| R_F \tag{5.84}$$

A_v

$$A_v \cong -\frac{R_C}{R_E} \tag{5.85}$$

5.14 COLLECTOR DC FEEDBACK CONFIGURATION

The network of Fig. 5.65 has a dc feedback resistor for increased stability, yet the capacitor C_3 will shift portions of the feedback resistance to the input and output sections of the network in the ac domain. The portion of R_F shifted to the input or output side will be determined by the desired ac input and output resistance levels.

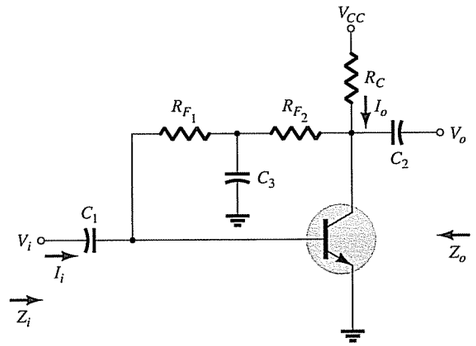


FIG. 5.65
Collector dc feedback configuration.

At the frequency or frequencies of operation, the capacitor will assume a short-circuit equivalent to ground due to its low impedance level compared to the other elements of the network. The small-signal ac equivalent circuit will then appear as shown in Fig. 5.66.

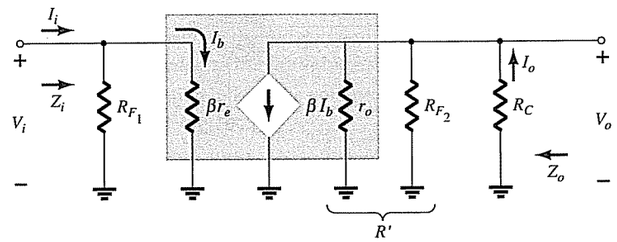


FIG. 5.66
Substituting the r_e equivalent circuit into the ac equivalent network of Fig. 5.65.

Z_i

$$Z_i = R_{F_1} \| \beta r_e \tag{5.86}$$

Z_o

$$Z_o = R_C \| R_{F_2} \| r_o \tag{5.87}$$

For $r_o \geq 10R_C$,

$$Z_o \cong R_C \| R_{F_2} \quad r_o \geq 10R_C \tag{5.88}$$

A_v

$$R' = r_o \| R_{F_2} \| R_C$$

and

$$V_o = -\beta I_b R'$$

but

$$I_b = \frac{V_i}{\beta r_e}$$

and

$$V_o = -\beta \frac{V_i}{\beta r_e} R'$$

so that

$$A_v = \frac{V_o}{V_i} = -\frac{r_o \| R_{F_2} \| R_C}{r_e} \tag{5.89}$$

For $r_o \geq 10R_C$,

$$A_v = \frac{V_o}{V_i} \cong -\frac{R_{F_2} \| R_C}{r_e} \qquad r_o \geq 10R_C \qquad \textbf{(5.90)}$$

Phase Relationship The negative sign in Eq. (5.89) clearly reveals a 180° phase shift between input and output voltages.

EXAMPLE 5.13 For the network of Fig. 5.67, determine:

a. r_e.
b. Z_i.
c. Z_o.
d. A_v.

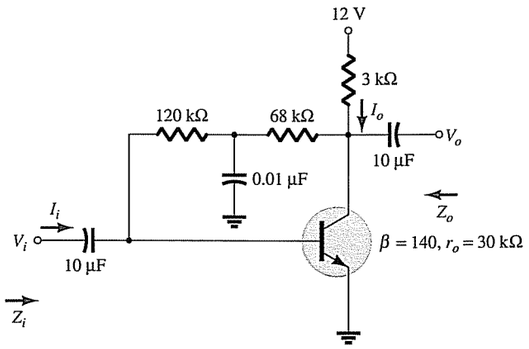


FIG. 5.67
Example 5.13.

Multisim

Solution:

a. DC: $I_B = \dfrac{V_{CC} - V_{BE}}{R_F + \beta R_C}$

$$= \frac{12\text{ V} - 0.7\text{ V}}{(120\text{ k}\Omega + 68\text{ k}\Omega) + (140)3\text{ k}\Omega}$$

$$= \frac{11.3\text{ V}}{608\text{ k}\Omega} = 18.6\,\mu\text{A}$$

$$I_E = (\beta + 1)I_B = (141)(18.6\,\mu\text{A})$$

$$= 2.62\text{ mA}$$

$$r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{2.62\text{ mA}} = \mathbf{9.92\ \Omega}$$

b. $\beta r_e = (140)(9.92\ \Omega) = 1.39\text{ k}\Omega$

The ac equivalent network appears in Fig. 5.68.

$Z_i = R_{F_1} \| \beta r_e = 120\text{ k}\Omega \| 1.39\text{ k}\Omega$

$\cong \mathbf{1.37\ k\Omega}$

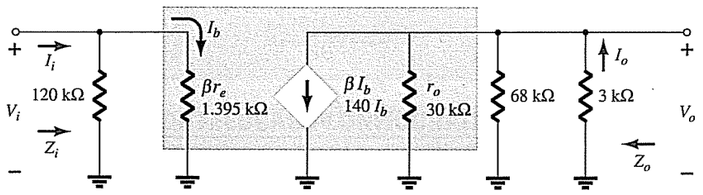


FIG. 5.68
Substituting the r_e equivalent circuit into the ac equivalent network of Fig. 5.67.

c. Testing the condition $r_o \geq 10R_C$, we find

$$30\text{ k}\Omega \geq 10(3\text{ k}\Omega) = 30\text{ k}\Omega$$

which is satisfied through the equals sign in the condition. Therefore,

$Z_o \cong R_C \| R_{F_2} = 3\text{ k}\Omega \| 68\text{ k}\Omega$

$= \mathbf{2.87\ k\Omega}$

d. $r_o \geq 10R_C$; therefore,

$$A_v \cong -\frac{R_{F_2} \| R_C}{r_e} = -\frac{68\text{ k}\Omega \| 3\text{ k}\Omega}{9.92\ \Omega}$$

$$\cong -\frac{2.87\text{ k}\Omega}{9.92\ \Omega}$$

$$\cong \mathbf{-289.3}$$

5.15 DETERMINING THE CURRENT GAIN

You may have noticed in the last seven sections that the current gain was not determined for each configuration. Earlier editions of this text did have the details of finding that gain, but in reality the voltage gain is usually the gain of most importance. The absence of the derivations should not cause concern because:

For each transistor configuration, the current gain can be determined directly from the voltage gain, the defined load, and the input impedance.

The derivation of the equation linking the voltage and current gains can be derived using the two-port configuration of Fig. 5.69.

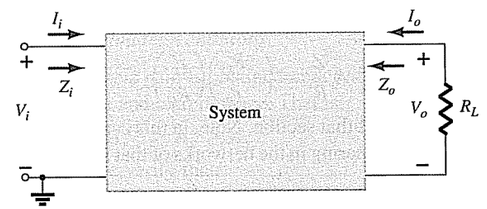


FIG. 5.69
Determining the current gain using the voltage gain.

The current gain is defined by

$$A_i = \frac{I_o}{I_i} \qquad \textbf{(5.91)}$$

Applying Ohm's law to the input and output circuits results in

$$I_i = \frac{V_i}{Z_i} \qquad \text{and} \qquad I_o = -\frac{V_o}{R_L}$$

The minus sign associated with the output equation is simply there to indicate that the polarity of the output voltage is determined by an output current having the opposite direction. By definition, the input and output currents have a direction entering the two-port configuration.

Substituting into Eq. (5.91) then results in

$$A_i = \frac{I_o}{I_i} = \frac{-\dfrac{V_o}{R_L}}{\dfrac{V_i}{Z_i}} = -\frac{V_o}{V_i} \cdot \frac{Z_i}{R_L}$$

and the following important equation:

$$A_i = -A_v \frac{Z_i}{R_L} \qquad \textbf{(5.92)}$$

The value of R_L is defined by the location of V_o and I_o.

To demonstrate the validity of Eq. (5.92), consider the voltage-divider bias configuration of Fig. 5.40. In this case the input impedance is

$$Z_i \cong \beta r_e$$

with $R_L = R_C$ (I_o defined as the current through R_C) and a voltage gain of

$$A_v \cong -\frac{R_C}{r_e}$$

Substituting into Eq. (5.92) results in

$$A_i = -A_v\frac{Z_i}{R_L} = -\left(-\frac{R_C}{r_e}\right)\left(\frac{\beta r_e}{R_C}\right) \cong \beta$$

which matches the long-hand solution. Note, in particular, that the gain is positive number, indicating that the directions defined for the input and output currents of Fig. 5.40 are the correct directions.

The solution to the current gain in terms of the network parameters will be more complicated for some configurations if a solution is desired in terms of the network parameters. However, if a numerical solution is all that is desired, it is simply a matter of substituting the value of the three parameters from an analysis of the voltage gain.

As a second example, consider the collector feedback bias configuration of Section 5.13. In this case the voltage gain is

$$A_v \cong \frac{R_C}{r_e}$$

and the input impedance is

$$Z_i \cong R_E \| r_e \cong r_e$$

with R_L defined as R_C due to the location of I_o.

The result is the following:

$$A_i = -A_v\frac{Z_i}{R_L} = \left(-\frac{R_C}{r_e}\right)\left(\frac{r_e}{R_C}\right) \cong -1$$

which agrees with the solution of that section. Note, in this case, that the output current has the opposite direction to that appearing in the networks of that section due to the minus sign.

5.16 EFFECT OF R_L AND R_s

All the parameters determined in the last few sections have been for an unloaded amplifier with the input voltage connected directly to a terminal of the transistor. In this section the effect of applying a load and the effect of using a source with an internal resistance will be investigated. The network of Fig. 5.70a is typical of those investigated in the previous section.

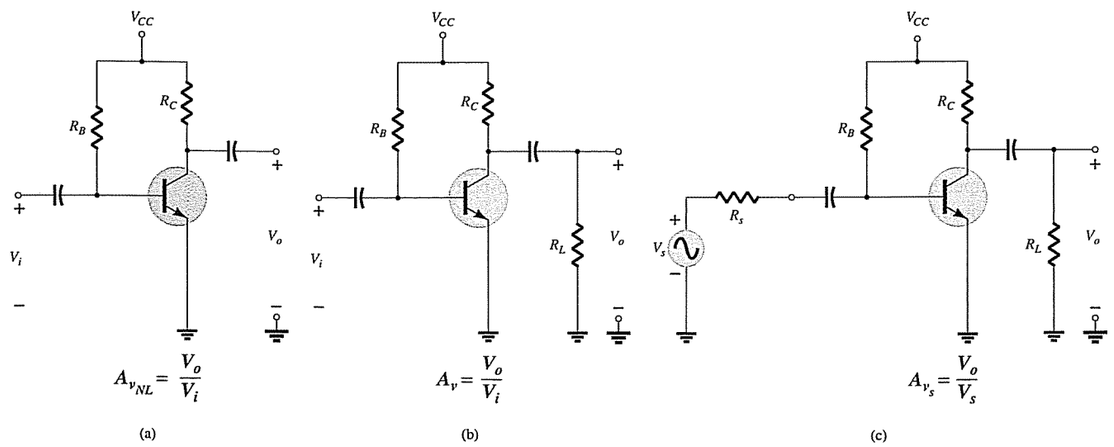


FIG. 5.70
Amplifier configurations: (a) unloaded; (b) loaded; (c) loaded with a source resistance.

Since a resistive load was not attached to the output terminal, the gain is commonly referred to as the no-load gain and given the following notation:

$$\boxed{A_{v_{NL}} = \frac{V_o}{V_i}} \qquad \textbf{(5.93)}$$

In Fig. 5.70b a load has been added in the form of a resistor R_L, which will change the overall gain of the system. This loaded gain is typically given the following notation:

$$\boxed{A_v = \frac{V_o}{V_i}}_{\text{with } R_L} \qquad \textbf{(5.94)}$$

In Fig. 5.70c both a load and a source resistance have been introduced, which will have an additional effect on the gain of the system. The resulting gain is typically given the following notation:

$$\boxed{A_{v_s} = \frac{V_o}{V_s}}_{\text{with } R_L \text{ and } R_s} \qquad \textbf{(5.95)}$$

The analysis to follow will show that:

The loaded voltage gain of an amplifier is always less than the no-load gain.

In other words, the addition of a load resistor R_L to the configuration of Fig. 5.70a will always have the effect of reducing the gain below the no-load level.

Furthermore:

The gain obtained with a source resistance in place will always be less than that obtained under loaded or unloaded conditions.

In total, therefore, the highest gain is obtained under no-load conditions and the lowest gain with a source impedance and load in place. That is:

For the same configuration $A_{v_{NL}} > A_v > A_{v_s}$.

It will also be interesting to verify that:

For a particular design, the larger the level of R_L***, the greater is the level of ac gain.***

In other words, the larger the load resistance, the closer it is to an open-circuit approximation that would result in the higher no-load gain.

In addition:

For a particular amplifier, the smaller the internal resistance of the signal source, the greater is the overall gain.

In other words, the closer the source resistance is to a short-circuit approximation, the greater is the gain since the effect of R_s will essentially be eliminated.

The conclusions listed above are all quite important in the amplifier design process. When one purchases a packaged amplifier, the listed gain and all the other parameters are for the *unloaded situation.* The gain that results due to the application of a load or source resistance can have a dramatic effect on all the amplifier parameters, as will be demonstrated in the examples to follow.

In general, there are two directions one can take to analyze networks with an applied load and/or source resistance. One approach is to simply insert the equivalent circuit, as was demonstrated in Section 5.14, and use methods of analysis to determine the quantities of interest. The second is to define a two-port equivalent model and use the parameters determined for the no-load situation. The analysis to follow in this section will use the first approach, leaving the second method for Section 5.17. Priorities do not permit a detailed analysis of each configuration as occurred in Section 5.14. However, the analysis to follow should be ample preparation to investigate any transistor amplifier with a load or source resistance.

For the fixed-bias transistor amplifier of Fig. 5.70c, substituting the r_e equivalent circuit for the transistor and removing the dc parameters results in the configuration of Fig. 5.71.

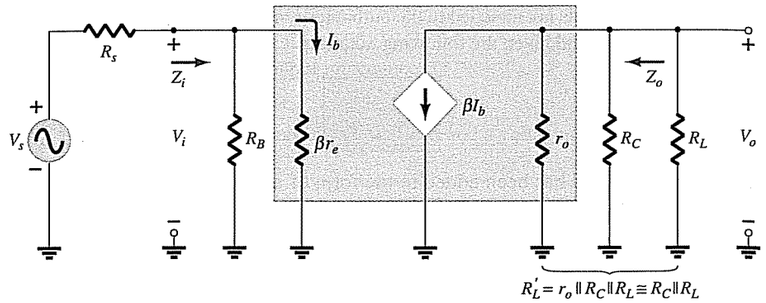


FIG. 5.71
The ac equivalent network for the network of Fig. 5.70c.

It is particularly interesting that Fig. 5.71 is exactly the same in appearance as Fig. 5.36 except that now there is a load resistance in parallel with R_C and a source resistance has been introduced in series with a source V_s.

The parallel combination of

$$R'_L = r_o \| R_C \| R_L \cong R_C \| R_L$$

and

$$V_o = -\beta I_b R'_L = -\beta I_b (R_C \| R_L)$$

with

$$I_b = \frac{V_i}{\beta r_e}$$

gives

$$V_o = -\beta \left(\frac{V_i}{\beta r_e} \right) (R_C \| R_L)$$

so that

$$\boxed{A_v = \frac{V_o}{V_i} = -\frac{R_C \| R_L}{r_e}} \qquad \textbf{(5.96)}$$

The only difference in the gain equation using V_i as the input voltage is the fact that R_C of Eq. (5.32) has been replaced by the parallel combination of R_C and R_L. This makes good sense since the output voltage of Fig. 5.71 is now across the parallel combination of the two resistors.

The input impedance is

$$\boxed{Z_i = R_B \| \beta r_e} \qquad \textbf{(5.97)}$$

as before, and the output impedance is

$$\boxed{Z_o = R_C \| r_o} \qquad \textbf{(5.98)}$$

as before.

If the overall gain from signal source V_s to output voltage V_o is desired, it is only necessary to apply the voltage-divider rule as follows:

$$V_i = \frac{Z_i V_s}{Z_i + R_s}$$

and

$$\frac{V_i}{V_s} = \frac{Z_i}{Z_i + R_s}$$

or

$$A_{v_s} = \frac{V_o}{V_s} = \frac{V_o}{V_i} \cdot \frac{V_i}{V_s} = A_v \frac{Z_i}{Z_i + R_s}$$

so that

$$\boxed{A_{v_s} = \frac{Z_i}{Z_i + R_s} \cdot A_v} \qquad \textbf{(5.99)}$$

Since the factor $Z_i/(Z_i + R_s)$ must always be less than one, Eq. (5.99) clearly supports the fact that the signal gain A_{v_s} is always less than the loaded gain A_v.

EXAMPLE 5.14 Using the parameter values for the fixed-bias configuration of Example 5.4 with an applied load of 4.7 kΩ and a source resistance of 0.3 kΩ, determine the following and compare to the no-load values:

a. A_v.
b. A_{v_s}.
c. Z_i.
d. Z_o.

Solution:

a. Eq. (5.96): $A_v = -\dfrac{R_C \| R_L}{r_e} = -\dfrac{3\,\text{k}\Omega \| 4.7\,\text{k}\Omega}{10.71\,\Omega} = -\dfrac{1.831\,\text{k}\Omega}{10.71\,\Omega} = \mathbf{-170.98}$

which is significantly less than the no-load gain of −280.11.

b. Eq. (5.99): $A_{v_s} = \dfrac{Z_i}{Z_i + R_s} \cdot A_v$

With $Z_i = 1.07\,\text{k}\Omega$ from Example 5.4, we have

$$A_{v_s} = \frac{1.07\,\text{k}\Omega}{1.07\,\text{k}\Omega + 0.3\,\text{k}\Omega} \cdot (-170.98) = \mathbf{-133.54}$$

which again is significantly less than $A_{v_{\text{NL}}}$ or A_v.

c. $Z_i = \mathbf{1.07\,k\Omega}$ as obtained for the no-load situation.

d. $Z_o = R_C = \mathbf{3\,k\Omega}$ as obtained for the no-load situation.

The example clearly demonstrates that $A_{v_{\text{NL}}} > A_v > A_{v_s}$.

For the voltage-divider configuration of Fig. 5.72 with an applied load and series source resistor the ac equivalent network is as shown in Fig. 5.73.

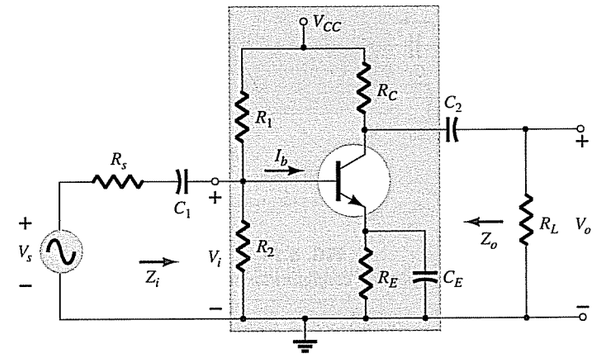


FIG. 5.72
Voltage-divider bias configuration with R_s and R_L.

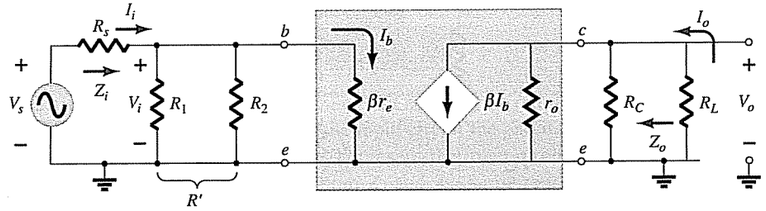


FIG. 5.73
Substituting the r_e equivalent circuit into the ac equivalent network of Fig. 5.72.

First note the strong similarities with Fig. 5.71, with the only difference being the parallel connection of R_1 and R_2 instead of just R_B. Everything else is exactly the same. The following equations result for the important parameters of the configuration:

$$A_v = \frac{V_o}{V_i} = -\frac{R_C \| R_L}{r_e} \tag{5.100}$$

$$Z_i = R_1 \| R_2 \| \beta r_e \tag{5.101}$$

$$Z_o = R_C \| r_o \tag{5.102}$$

For the emitter-follower configuration of Fig. 5.74 the small-signal ac equivalent network is as shown in Fig. 5.75. The only difference between Fig. 5.75 and the unloaded configuration of Fig. 5.52 is the parallel combination of R_E and R_L and the addition of the source resistor R_s. The equations for the quantities of interest can therefore be determined by simply replacing R_E by $R_E \| R_L$ wherever R_E appears. If R_E does not appear in an equation, the load resistor R_L does not affect that parameter. That is,

$$A_v = \frac{V_o}{V_i} = \frac{R_E \| R_L}{R_E \| R_L + r_e} \tag{5.103}$$

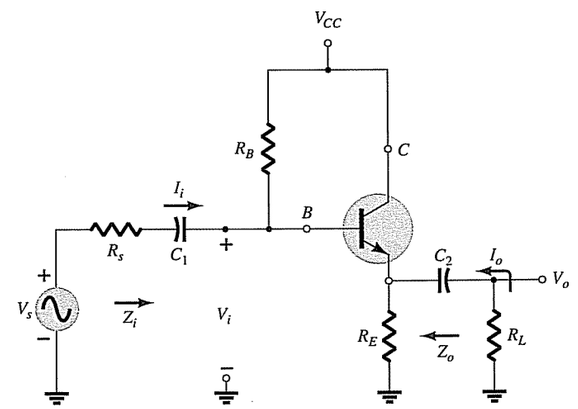


FIG. 5.74
Emitter-follower configuration with R_s and R_L.

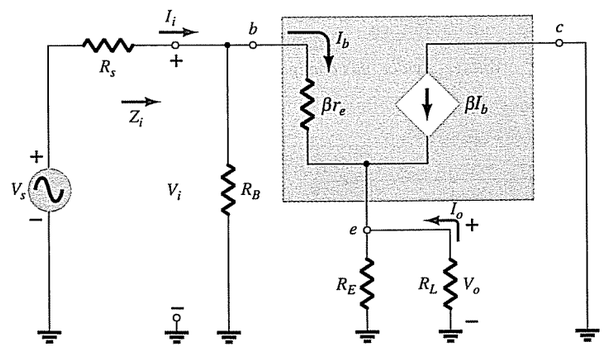


FIG. 5.75
Substituting the r_e equivalent circuit into the ac equivalent network of Fig. 5.74

$$Z_i = R_B \| Z_b \tag{5.104}$$

$$Z_b \cong \beta(R_E \| R_L) \tag{5.105}$$

$$Z_o \cong r_e \tag{5.106}$$

The effect of a load resistor and a source impedance on the remaining BJT configurations will not be examined in detail here, although Table 5.1 in Section 5.18 will review the results for each configuration.

5.17 TWO-PORT SYSTEMS APPROACH

This section introduces an alternative approach to the analysis of the previous section. It plays an important role in the design of today's systems where the designer works with packaged products rather than individual elements. In other words, a particular package may house an amplifier with all the components appearing in the no-load version of a configuration as described in Section 5.14. Along with that package are the gain, input, and output impedances. However, it is important to understand that those parameters are the no-load results, which the designer must know how to use effectively. In this section, the no-load or packaged results will be used to find the gain and various impedances under loaded conditions. The result is an elimination of the need to know the internal components of the package, and the effect of an applied load or source resistance can be found quickly and efficiently.

The discussion begins with an examination of the basic two port system of Fig. 5.76, in which all the important parameters of the system have been identified.

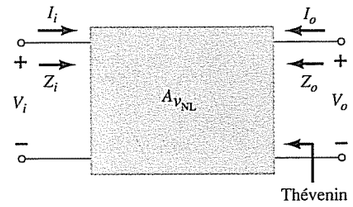


FIG. 5.76
Two-port system.

If we take a "Thévenin look" at the output terminals, we find, with V_i set to zero, that

$$Z_{\text{Th}} = Z_o = R_o \tag{5.107}$$

E_{Th} is the open-circuit voltage between the output terminals, identified as V_o. However,

$$A_{v_{NL}} = \frac{V_o}{V_i}$$

and

$$V_o = A_{v_{NL}} V_i$$

so that

$$E_{\text{Th}} = A_{v_{NL}} V_i \tag{5.108}$$

Substituting the Thévenin equivalent circuit between the output terminals results in the output configuration of Fig. 5.77. For the input circuit the parameters V_i and I_i are related by $Z_i = R_i$, permitting the use of R_i to represent the input circuit. Since our present interest is in BJT and FET amplifiers, both Z_o and Z_i can be represented by resistive elements.

Before continuing, let us check the results of Fig. 5.77 by finding Z_o and $A_{v_{NL}}$ in the usual manner. To find Z_o, V_i is set to zero, resulting in $A_{v_{NL}} V_i = 0$, permitting a short-circuit

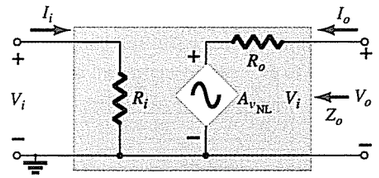


FIG. 5.77
Substituting the internal elements for the two-port system of Fig. 5.76.

equivalent for the source. The result is an output impedance equal to R_o as originally defined. The absence of a load will result in $I_o = 0$, and the voltage drop across the impedance R_o will be 0 V. The open-circuit output voltage is therefore $A_{v_{NL}}V_i$, as it should be. Before looking at an example, take note of the fact that A_i does not appear in the two-port model of Fig. 5.77, and in fact is seldom part of the two-port system analysis of active devices. This is not to say that the quantity is seldom calculated, but it is most frequently calculated from the expression $A_i = -A_v(Z_i/R_L)$, where R_L is the defined load for the analysis of interest.

A second format for Fig. 5.77, particularly popular with op-amps (operational amplifiers), appears in Fig. 5.78. The only change is the general appearance of the model.

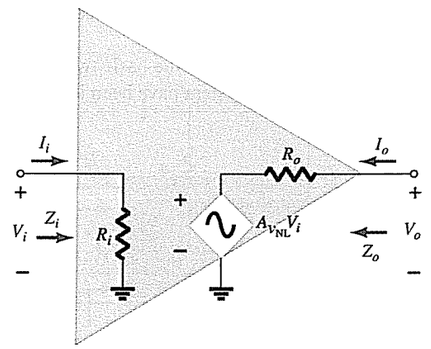


FIG. 5.78
Operational amplifier (op-amp) notation.

The effect of applying a load to a two-port system will result in the configuration of Fig. 5.79. Ideally, all the parameters of the model are unaffected by changing loads and levels of source resistance. However, for some transistor configurations the applied load can affect the input resistance, whereas for others the output resistance can be affected by the source resistance. In all cases, however, by simple definition, the no-load gain is unaffected by the application of any load. In any case, once $A_{v_{NL}}$, R_i, and R_o are defined for a particular configuration, the equations about to be derived can be employed.

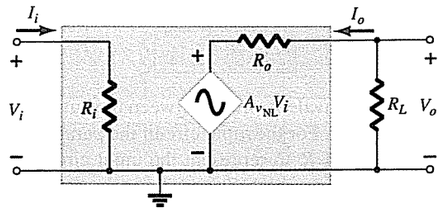


FIG. 5.79
Applying a load to the two-port system of Fig. 5.77.

Applying a load to the two-port system of Fig. 5.77 results in the configuration of Fig. 5.79. Applying the voltage-divider rule to the output circuit results in

$$V_o = \frac{R_L A_{v_{NL}} V_i}{R_L + R_o}$$

and

$$\boxed{A_v = \frac{V_o}{V_i} = \frac{R_L}{R_L + R_o} A_{v_{NL}}} \qquad \textbf{(5.109)}$$

Since the ratio $R_L/(R_L + R_o)$ is always less than 1, we have further evidence that the loaded voltage gain of an amplifier is always less than the no-load level.

The current gain is then determined by

$$A_i = \frac{I_o}{I_i} = \frac{-V_o/R_L}{V_i/Z_i} = -\frac{V_o}{V_i}\frac{Z_i}{R_L}$$

and

$$\boxed{A_i = -A_v \frac{Z_i}{R_L}} \qquad \textbf{(5.110)}$$

as obtained earlier. In general, therefore, the current gain can be obtained from the voltage gain and impedance parameters Z_i and R_L. The next example will demonstrate the usefulness and validity of Eqs. (5.109) and (5.110).

Our attention will now turn to the input side of the two-port system and the effect of an internal source resistance on the gain of an amplifier. In Fig. 5.80, a source with an internal resistance has been applied to the basic two-port system. The definitions of Z_i and $A_{v_{NL}}$ are such that:

The parameters Z_i and $A_{v_{NL}}$ of a two-port system are unaffected by the internal resistance of the applied source.

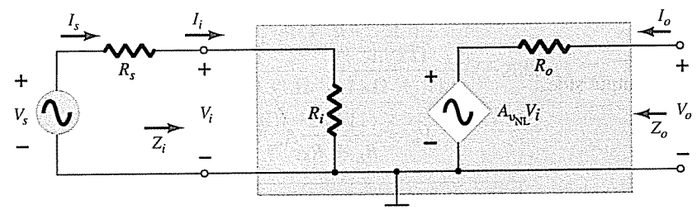


FIG. 5.80
Including the effects of the source resistance R_s.

However:

The output impedance may be affected by the magnitude of R_s.

The fraction of the applied signal reaching the input terminals of the amplifier of Fig. 5.80 is determined by the voltage-divider rule. That is,

$$\boxed{V_i = \frac{R_i V_s}{R_i + R_s}} \qquad \textbf{(5.111)}$$

Equation (5.111) clearly shows that the larger the magnitude of R_s, the lower is the voltage at the input terminals of the amplifier. In general, therefore, as mentioned earlier, for a particular amplifier, the larger the internal resistance of a signal source, the lower is the overall gain of the system.

For the two-port system of Fig. 5.80,

$$V_o = A_{v_{NL}} V_i$$

and

$$V_i = \frac{R_i V_s}{R_i + R_s}$$

so that $$V_o = A_{v_{NL}} \frac{R_i}{R_i + R_s} V_s$$

and $$\boxed{A_{v_s} = \frac{V_o}{V_s} = \frac{R_i}{R_i + R_s} A_{v_{NL}}} \qquad \textbf{(5.112)}$$

The effects of R_s and R_L have now been demonstrated on an individual basis. The next natural question is how the presence of both factors in the same network will affect the total gain. In Fig. 5.81, a source with an internal resistance R_s and a load R_L have been applied to a two-port system for which the parameters Z_i, $A_{v_{NL}}$, and Z_o have been specified. For the moment, let us assume that Z_i and Z_o are unaffected by R_L and R_s, respectively.

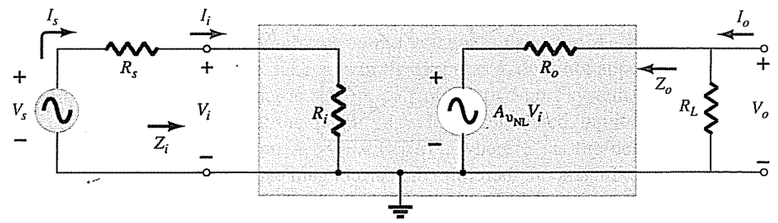


FIG. 5.81
Considering the effects of R_s and R_L on the gain of an amplifier.

At the input side we find

$$\text{Eq. (5.111):} \quad V_i = \frac{R_i V_s}{R_i + R_s}$$

or $$\boxed{\frac{V_i}{V_s} = \frac{R_i}{R_i + R_s}} \qquad \textbf{(5.113)}$$

and at the output side,

$$V_o = \frac{R_L}{R_L + R_o} A_{v_{NL}} V_i$$

or $$\boxed{A_v = \frac{V_o}{V_i} = \frac{R_L A_{v_{NL}}}{R_L + R_o} = \frac{R_L}{R_L + R_o} A_{v_{NL}}} \qquad \textbf{(5.114)}$$

For the total gain $A_{v_s} = V_o/V_s$, the following mathematical steps can be performed:

$$A_{v_s} = \frac{V_o}{V_s} = \frac{V_o}{V_i} \cdot \frac{V_i}{V_s} \qquad \textbf{(5.115)}$$

and substituting Eqs. (5.113) and (5.114) results in

$$\boxed{A_{v_s} = \frac{V_o}{V_s} = \frac{R_i}{R_i + R_s} \cdot \frac{R_L}{R_L + R_o} A_{v_{NL}}} \qquad \textbf{(5.116)}$$

Since $I_i = V_i/R_i$, as before,

$$\boxed{A_i = -A_v \frac{R_i}{R_L}} \qquad \textbf{(5.117)}$$

or, using $I_s = V_s/(R_s + R_i)$,

$$\boxed{A_{i_s} = -A_{v_s} \frac{R_s + R_i}{R_L}} \qquad \textbf{(5.118)}$$

However, $I_i = I_s$, so Eqs. (5.117) and (5.118) generate the same result. Equation (5.116) clearly reveals that both the source and the load resistance will reduce the overall gain of the system.

The two reduction factors of Eq. (5.116) form a product that has to be carefully considered in any design procedure. It is not sufficient to ensure that R_s is relatively small if the effect of the magnitude of R_L is ignored. For instance, in Eq. (5.116), if the first factor is 0.9 and the second factor is 0.2, the product of the two results in an overall reduction factor equal to $(0.9)(0.2) = 0.18$, which is close to the lower factor. The effect of the excellent 0.9 level was completely wiped out by the significantly lower second multiplier. If both were 0.9-level factors, the net result would be $(0.9)(0.9) = 0.81$, which is still quite high. Even if the first were 0.9 and the second 0.7, the net result of 0.63 would still be respectable. In general, therefore, for good overall gain the effects of R_s and R_L must be evaluated individually and as a product.

EXAMPLE 5.15 Determine A_v and A_{v_s} for the network of Example 5.14 and compare solutions. Example 5.4 showed that $A_{v_{NL}} = -280$, $Z_i = 1.07\,\text{k}\Omega$, and $Z_o = 3\,\text{k}\Omega$. In Example 5.14, $R_L = 4.7\,\text{k}\Omega$ and $R_s = 0.3\,\text{k}\Omega$.

Solution:

a. Eq. (5.109): $$A_v = \frac{R_L}{R_L + R_o} A_{v_{NL}}$$
$$= \frac{4.7\,\text{k}\Omega}{4.7\,\text{k}\Omega + 3\,\text{k}\Omega}(-280.11)$$
$$= \mathbf{-170.98}$$

as in Example 5.14.

b. Eq. (5.116): $$A_{v_s} = \frac{R_i}{R_i + R_s} \cdot \frac{R_L}{R_L + R_o} A_{v_{NL}}$$
$$= \frac{1.07\,\text{k}\Omega}{1.07\,\text{k}\Omega + 0.3\,\text{k}\Omega} \cdot \frac{4.7\,\text{k}\Omega}{4.7\,\text{k}\Omega + 3\,\text{k}\Omega}(-280.11)$$
$$= (0.781)(0.610)(-280.11)$$
$$= \mathbf{-133.45}$$

as in Example 5.14.

EXAMPLE 5.16 Given the packaged (no-entry-possible) amplifier of Fig. 5.82:

a. Determine the gain A_v and compare it to the no-load value with $R_L = 1.2\,\text{k}\Omega$.
b. Repeat part (a) with $R_L = 5.6\,\text{k}\Omega$ and compare solutions.
c. Determine A_{v_s} with $R_L = 1.2\,\text{k}\Omega$.
d. Find the current gain $A_i = \frac{I_o}{I_i} = \frac{I_o}{I_s}$ with $R_L = 5.6\,\text{k}\Omega$.

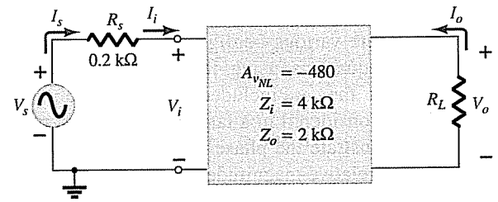


FIG. 5.82
Amplifier for Example 5.16.

Solution:

a. Eq. (5.109): $A_v = \dfrac{R_L}{R_L + R_o} A_{v_{NL}}$

$$= \frac{1.2\,\text{k}\Omega}{1.2\,\text{k}\Omega + 2\text{k}\Omega}(-480) = (0.375)(-480)$$

$$= \mathbf{-180}$$

which is a dramatic drop from the no-load value.

b. Eq. (5.109): $A_v = \dfrac{R_L}{R_L + R_o} A_{v_{NL}}$

$$= \frac{5.6\,\text{k}\Omega}{5.6\,\text{k}\Omega + 2\,\text{k}\Omega}(-480) = (0.737)(-480)$$

$$= \mathbf{-353.76}$$

which clearly reveals that the larger the load resistor, the better is the gain.

c. Eq. (5.116): $A_{v_s} = \dfrac{R_i}{R_i + R_s} \cdot \dfrac{R_L}{R_L + R_o} A_{v_{NL}}$

$$= \frac{4\,\text{k}\Omega}{4\,\text{k}\Omega + 0.2\,\text{k}\Omega} \cdot \frac{1.2\,\text{k}\Omega}{1.2\,\text{k}\Omega + 2\,\text{k}\Omega}(-480)$$

$$= (0.952)(0.375)(-480)$$

$$= \mathbf{-171.36}$$

which is fairly close to the loaded gain A_v because the input impedance is considerably more than the source resistance. In other words, the source resistance is relatively small compared to the input impedance of the amplifier.

d. $A_i = \dfrac{I_o}{I_i} = \dfrac{I_o}{I_s} = -A_v \dfrac{Z_i}{R_L}$

$$= -(-353.76)\left(\frac{4\,\text{k}\Omega}{5.6\,\text{k}\Omega}\right) = (-353.76)(0.714)$$

$$= \mathbf{-252.6}$$

It is important to realize that when using the two-port equations in some configurations the input impedance is sensitive to the applied load (such as the emitter-follower and collector feedback) and in some the output impedance is sensitive to the applied source resistance (such as the emitter-follower). In such cases the no-load parameters for Z_i and Z_o have to first be calculated before substituting into the two-port equations. For most packaged systems such as op-amps this sensitivity of the input and output parameters to the applied load or source resistance is minimized to eliminate the need to be concerned about changes from the no-load levels when using the two-port equations.

5.18 SUMMARY TABLE

The last few sections have included a number of derivations for unloaded and loaded BJT configurations. The material is so extensive that it seemed appropriate to review most of the conclusions for the various configurations in summary tables for quick comparisons. Although the equations using the hybrid parameters have not been discussed in detail at this point, they are included to make the tables complete. The use of hybrid parameters will be considered in a later section of this chapter. In each case the waveforms included demonstrate the phase relationship between input and output voltages. They also reveal the relative magnitude of the voltages at the input and output terminals.

Table 5.1 is for the unloaded situation, whereas Table 5.2 includes the effect of R_s and R_L.

TABLE 5.1
Unloaded BJT Transistor Amplifiers

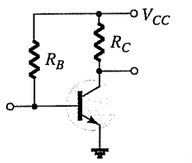
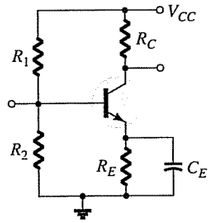
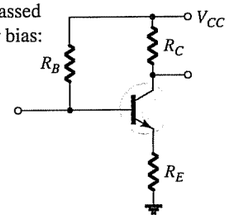
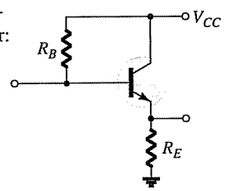
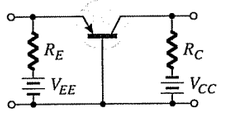
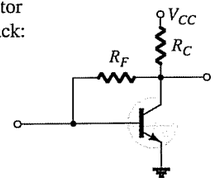
Configuration	Z_i	Z_o	A_v	A_i
Fixed-bias: 	Medium (1 kΩ) $= \boxed{R_B \| \beta r_e}$ $\cong \boxed{\beta r_e}$ $(R_B \geq 10\beta r_e)$	Medium (2 kΩ) $= \boxed{R_C \| r_o}$ $\cong \boxed{R_C}$ $(r_o \geq 10R_C)$	High (−200) $= \boxed{-\dfrac{(R_C \| r_o)}{r_e}}$ $\cong \boxed{-\dfrac{R_C}{r_e}}$ $(r_o \geq 10R_C)$	High (100) $= \boxed{\dfrac{\beta R_B r_o}{(r_o + R_C)(R_B + \beta r_e)}}$ $\cong \boxed{\beta}$ $(r_o \geq 10R_C, R_B \geq 10\beta r_e)$
Voltage-divider bias: 	Medium (1 kΩ) $= \boxed{R_1 \| R_2 \| \beta r_e}$	Medium (2 kΩ) $= \boxed{R_C \| r_o}$ $\cong \boxed{R_C}$ $(r_o \geq 10R_C)$	High (−200) $= \boxed{-\dfrac{R_C \| r_o}{r_e}}$ $\cong \boxed{-\dfrac{R_C}{r_e}}$ $(r_o \geq 10R_C)$	High (50) $= \boxed{\dfrac{\beta(R_1 \| R_2) r_o}{(r_o + R_C)(R_1 \| R_2 + \beta r_e)}}$ $\cong \boxed{\dfrac{\beta(R_1 \| R_2)}{R_1 \| R_2 + \beta r_e}}$ $(r_o \geq 10R_C)$
Unbypassed emitter bias: 	High (100 kΩ) $= \boxed{R_B \| Z_b}$ $Z_b \cong \beta(r_e + R_E)$ $\cong \boxed{R_B \| \beta R_E}$ $(R_E \gg r_e)$	Medium (2 kΩ) $= \boxed{R_C}$ (any level of r_o)	Low (−5) $= \boxed{-\dfrac{R_C}{r_e + R_E}}$ $\cong \boxed{-\dfrac{R_C}{R_E}}$ $(R_E \gg r_e)$	High (50) $\cong \boxed{-\dfrac{\beta R_B}{R_B + Z_b}}$
Emitter-follower: 	High (100 kΩ) $= \boxed{R_B \| Z_b}$ $Z_b \cong \beta(r_e + R_E)$ $\cong \boxed{R_B \| \beta R_E}$ $(R_E \gg r_e)$	Low (20 Ω) $= \boxed{R_E \| r_e}$ $\cong \boxed{r_e}$ $(R_E \gg r_e)$	Low ($\cong$ 1) $= \boxed{\dfrac{R_E}{R_E + r_e}}$ $\cong \boxed{1}$	High (−50) $\cong \boxed{-\dfrac{\beta R_B}{R_B + Z_b}}$
Common-base: 	Low (20 Ω) $= \boxed{R_E \| r_e}$ $\cong \boxed{r_e}$ $(R_E \gg r_e)$	Medium (2 kΩ) $= \boxed{R_C}$	High (200) $\cong \boxed{\dfrac{R_C}{r_e}}$	Low (−1) $\cong \boxed{-1}$
Collector feedback: 	Medium (1 kΩ) $= \boxed{\dfrac{r_e}{\frac{1}{\beta} + \frac{R_C}{R_F}}}$ $(r_o \geq 10R_C)$	Medium (2 kΩ) $\cong \boxed{R_C \| R_F}$ $(r_o \geq 10R_C)$	High (−200) $\cong \boxed{-\dfrac{R_C}{r_e}}$ $(r_o \geq 10R_C)$ $(R_F \gg R_C)$	High (50) $= \boxed{\dfrac{\beta R_F}{R_F + \beta R_C}}$ $\cong \boxed{\dfrac{R_F}{R_C}}$

TABLE 5.2

Loaded BJT Transistor Amplifiers Including the Effect of R_s

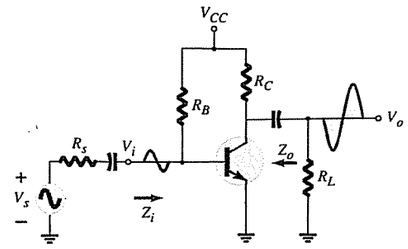
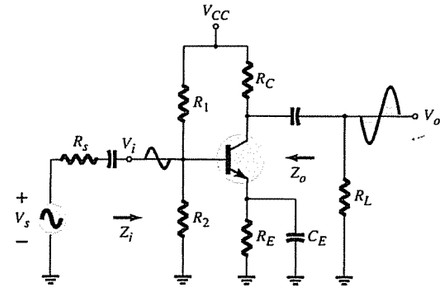
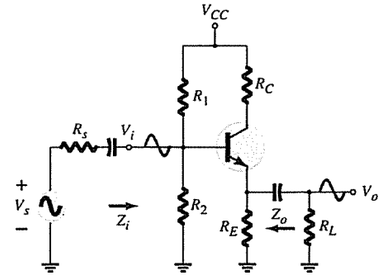
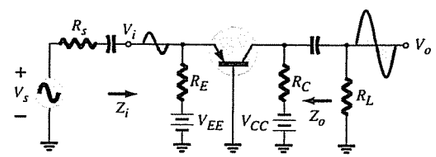
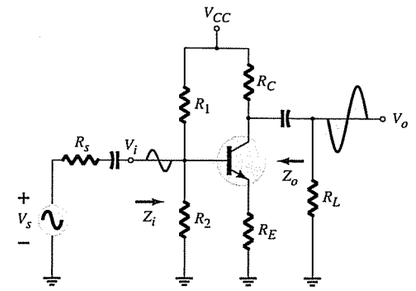
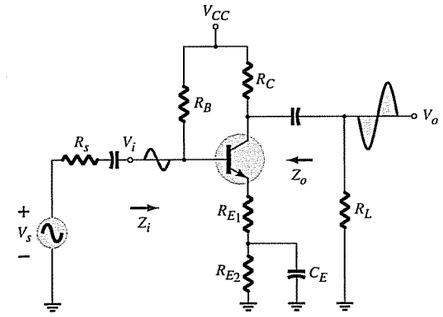
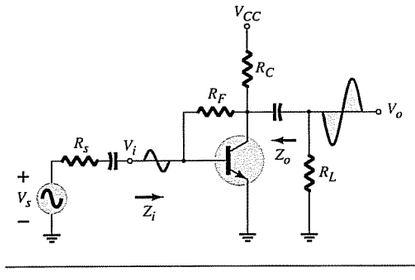
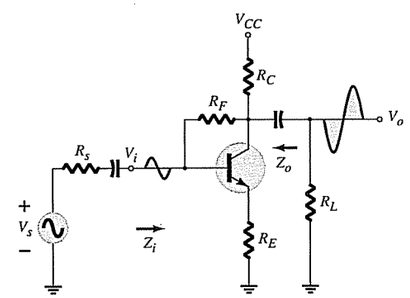
Configuration	$A_v = V_o/V_i$	Z_i	Z_o
	$\dfrac{-(R_L\|\|R_C)}{r_e}$	$R_B\|\|\beta r_e$	R_C
	hybrid: $\dfrac{-h_{fe}}{h_{ie}}(R_L\|\|R_C)$	$R_B\|\|h_{ie}$	R_C
	Including r_o: $\dfrac{-(R_L\|\|R_C\|\|r_o)}{r_e}$	$R_B\|\|\beta r_e$	$R_C\|\|r_o$
	$\dfrac{-(R_L\|\|R_C)}{r_e}$	$R_1\|\|R_2\|\|\beta r_e$	R_C
	hybrid: $\dfrac{-h_{fe}}{h_{ie}}(R_L\|\|R_C)$	$R_1\|\|R_2\|\|h_{ie}$	R_C
	Including r_o: $\dfrac{-(R_L\|\|R_C\|\|r_o)}{r_e}$	$R_1\|\|R_2\|\|\beta r_e$	$R_C\|\|r_o$
	$\cong 1$	$R'_E = R_L\|\|R_E$ $R_1\|\|R_2\|\|\beta(r_e + R'_E)$	$R'_s = R_s\|\|R_1\|\|R_2$ $R_E\|\|\left(\dfrac{R'_s}{\beta} + r_e\right)$
	hybrid: $\cong 1$	$R_1\|\|R_2\|\|(h_{ie} + h_{fe}R'_E)$	$R_E\|\|\left(\dfrac{R'_s + h_{ie}}{h_{fe}}\right)$
	Including r_o: $\cong 1$	$R_1\|\|R_2\|\|\beta(r_e + R'_E)$	$R_E\|\|\left(\dfrac{R'_s}{\beta} + r_e\right)$
	$\cong \dfrac{-(R_L\|\|R_C)}{r_e}$	$R_E\|\|r_e$	R_C
	hybrid: $\cong \dfrac{-h_{fb}}{h_{ib}}(R_L\|\|R_C)$	$R_E\|\|h_{ib}$	R_C
	Including r_o: $\cong \dfrac{-(R_L\|\|R_C\|\|r_o)}{r_e}$	$R_E\|\|r_e$	$R_C\|\|r_o$
	$\dfrac{-(R_L\|\|R_C)}{R_E}$	$R_1\|\|R_2\|\|\beta(r_e + R_E)$	R_C
	hybrid: $\dfrac{-(R_L\|\|R_C)}{R_E}$	$R_1\|\|R_2\|\|(h_{ie} + h_{fe}R_E)$	R_C
	Including r_o: $\dfrac{-(R_L\|\|R_C)}{R_E}$	$R_1\|\|R_2\|\|\beta(r_e + R_e)$	$\cong R_C$

TABLE 5.2

Loaded BJT Transistor Amplifiers Including the Effect of R_s

Configuration	$A_v = V_o/V_i$	Z_i	Z_o
	$\dfrac{-(R_L\|\|R_C)}{R_{E_1}}$	$R_B\|\|\beta(r_e + R_{E_1})$	R_C
	hybrid: $\dfrac{-(R_L\|\|R_C)}{R_{E_1}}$	$R_B\|\|(h_{ie} + h_{fe}R_{E_1})$	R_C
	Including r_o: $\dfrac{-(R_L\|\|R_C)}{R_{E_1}}$	$R_B\|\|\beta(r_e + R_E)$	$\cong R_C$
	$\dfrac{-(R_L\|\|R_C)}{r_e}$	$\beta r_e\|\|\dfrac{R_F}{\|A_v\|}$	R_C
	hybrid: $\dfrac{-h_{fe}}{h_{ie}}(R_L\|\|R_C)$	$h_{ie}\|\|\dfrac{R_F}{\|A_v\|}$	R_C
	Including r_o: $\dfrac{-(R_L\|\|R_C\|\|r_o)}{r_e}$	$\beta r_e\|\|\dfrac{R_F}{\|A_v\|}$	$R_C\|\|R_F\|\|r_o$
	$\dfrac{-(R_L\|\|R_C)}{R_E}$	$\beta R_E\|\|\dfrac{R_F}{\|A_v\|}$	$\cong R_C\|\|R_F$
	hybrid: $\dfrac{-(R_L\|\|R_C)}{R_E}$	$h_{fe}R_E\|\|\dfrac{R_F}{\|A_v\|}$	$\cong R_C\|\|R_F$
	Including r_o: $\cong \dfrac{-(R_L\|\|R_C)}{R_E}$	$\cong \beta R_E\|\|\dfrac{R_F}{\|A_v\|}$	$\cong R_C\|\|R_F$

5.19 CASCADED SYSTEMS

The two-port systems approach is particularly useful for cascaded systems such as that appearing in Fig. 5.83, where $A_{v_1}, A_{v_2}, A_{v_3}$, and so on, are the voltage gains of each stage *under loaded conditions*. That is, A_{v_1} is determined with the input impedance to A_{v_2} acting as the load on A_{v_1}. For A_{v_2}, A_{v_1} will determine the signal strength and source impedance at the input to A_{v_2}. The total gain of the system is then determined by the product of the individual gains as follows:

$$A_{v_T} = A_{v_1} \cdot A_{v_2} \cdot A_{v_3} \cdots \tag{5.113}$$

and the total current gain is given by

$$A_{i_T} = -A_{v_T}\frac{Z_{i_1}}{R_L} \tag{5.114}$$

No matter how perfect the system design, the application of a load to a two-port system will affect the voltage gain. Therefore, there is no possibility of a situation where A_{v_1}, A_{v_2}, and so on, of Fig. 5.83 are simply the no-load values. The loading of each succeeding stage

must be considered. The no-load parameters can be used to determine the loaded gains of Fig. 5.83, but Eq. (5.113) requires the loaded values.

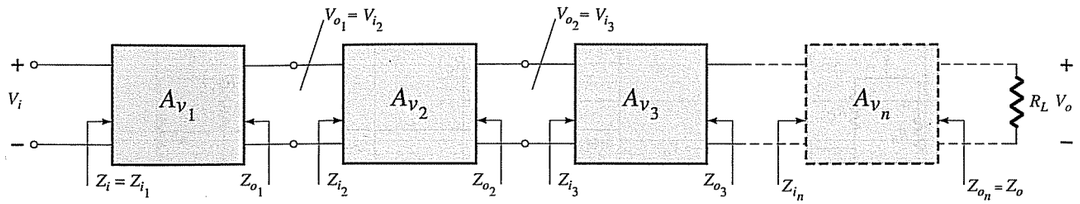


FIG. 5.83
Cascaded system.

EXAMPLE 5.17 The two-stage system of Fig. 5.84 employs a transistor emitter-follower configuration prior to a common-base configuration to ensure that the maximum percentage of the applied signal appears at the input terminals of the common-base amplifier. In Fig. 5.84, the no-load values are provided for each system, with the exception of Z_i and Z_o for the emitter-follower, which are the loaded values. For the configuration of Fig. 5.84, determine:

a. The loaded gain for each stage.
b. The total gain for the system, A_v and A_{v_s}.
c. The total current gain for the system.
d. The total gain for the system if the emitter-follower configuration were removed.

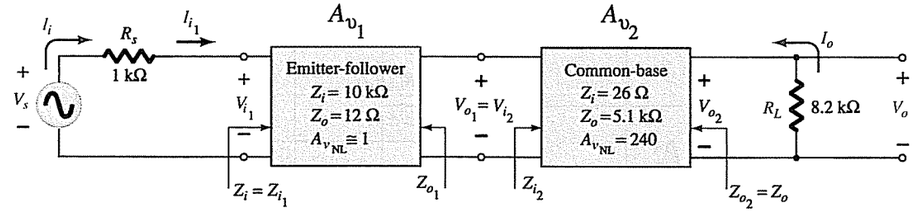


FIG. 5.84
Example 5.17.

Solution:

a. For the emitter-follower configuration, the loaded gain is

$$V_{o_1} = \frac{Z_{i_2}}{Z_{i_2} + Z_{o_1}} A_{v_{NL}} V_{i_1} = \frac{26\ \Omega}{26\ \Omega + 12\ \Omega}(1)\, V_{i_1} = 0.684\, V_{i_1}$$

and $$A_{V_i} = \frac{V_{o_1}}{V_{i_1}} = \mathbf{0.684}$$

For the common-base configuration,

$$V_{o_2} = \frac{R_L}{R_L + R_{o_2}} A_{v_{NL}} V_{i_2} = \frac{8.2\ \text{k}\Omega}{8.2\ \text{k}\Omega + 5.1\ \text{k}\Omega}(240)\, V_{i_2} = 147.97\, V_{i_2}$$

and $$A_{v_2} = \frac{V_{o_2}}{V_{i_2}} = \mathbf{147.97}$$

b. $$A_{v_T} = A_{v_1} A_{v_2}$$
$$= (0.684)(147.97)$$
$$= \mathbf{101.20}$$
$$A_{v_s} = \frac{Z_{i_1}}{Z_{i_1} + R_s} A_{v_T} = \frac{(10\ \text{k}\Omega)(101.20)}{10\ \text{k}\Omega + 1\ \text{k}\Omega}$$
$$= \mathbf{92}$$

c. $$A_{i_T} = -A_{v_T}\frac{Z_{i_1}}{R_L} = -(101.20)\left(\frac{10\ \text{k}\Omega}{8.2\ \text{k}\Omega}\right)$$
$$= \mathbf{-123.41}$$

d. $$V_i = \frac{Z_{i_{CB}}}{Z_{i_{CB}} + R_s} V_s = \frac{26\ \Omega}{26\ \Omega + 1\ \text{k}\Omega} V_s = 0.025\, V_s$$

and $$\frac{V_i}{V_s} = 0.025 \quad \text{with} \quad \frac{V_o}{V_i} = 147.97 \quad \text{from above}$$

and $$A_{v_s} = \frac{V_o}{V_s} = \frac{V_i}{V_s}\cdot\frac{V_o}{V_i} = (0.025)(147.97) = \mathbf{3.7}$$

In total, therefore, the gain is about 25 times greater with the emitter-follower configuration to draw the signal to the amplifier stages. Note, however, that it is also important that the output impedance of the first stage is relatively close to the input impedance of the second stage, otherwise the signal would have been "lost" again by the voltage-divider action.

RC-Coupled BJT Amplifiers

One popular connection of amplifier stages is the *RC*-coupled variety shown in Fig. 5.85 in the next example. The name is derived from the capacitive coupling capacitor C_c and the fact that the load on the first stage is an *RC* combination. The coupling capacitor isolates the two stages from a dc viewpoint but acts as a short-circuit equivalent for the ac response. The input impedance of the second stage acts as a load on the first stage, permitting the same approach to the analysis as described in the last two sections.

EXAMPLE 5.18



a. Calculate the no-load voltage gain and output voltage of the *RC*-coupled transistor amplifiers of Fig. 5.85.
b. Calculate the overall gain if a 10-kΩ load is applied to the second stage, and compare to the results of part (a).
c. Calculate the input impedance of the first stage and the output impedance of the second stage.

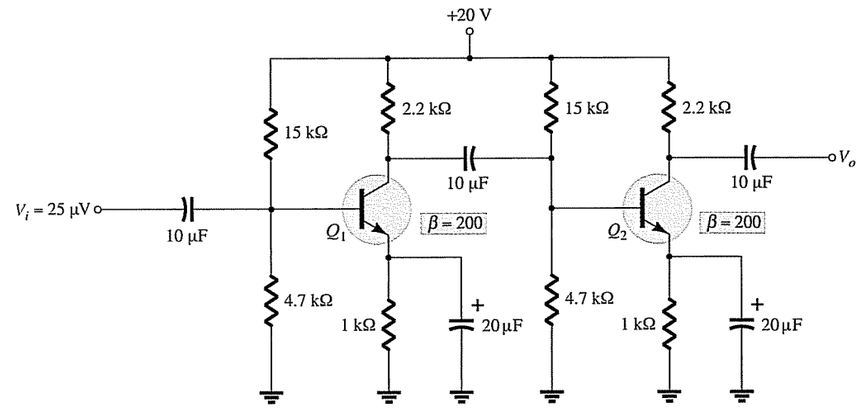


FIG. 5.85
RC-coupled BJT amplifier for Example 5.18.

Solution:

a. The dc bias analysis results in the following for each transistor:

$$V_B = 4.7\ \text{V}, \quad V_E = 4.0\ \text{V}, \quad V_C = 11\ \text{V}, \quad I_E = 4.0\ \text{mA}$$

At the bias point,

$$r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{4\text{ mA}} = 6.5\ \Omega$$

The loading of the second stage is

$$Z_{i_2} = R_1 \| R_2 \| \beta r_e$$

which results in the following gain for the first stage:

$$A_{v_1} = -\frac{R_C \| (R_1 \| R_2 \| \beta r_e)}{r_e}$$

$$= -\frac{(2.2\text{ k}\Omega) \| [15\text{ k}\Omega \| 4.7\text{ k}\Omega \| (200)(6.5\ \Omega)]}{6.5\ \Omega}$$

$$= -\frac{665.2\ \Omega}{6.5\ \Omega} = -102.3$$

For the unloaded second stage the gain is

$$A_{v_{2(\text{NL})}} = -\frac{R_C}{r_e} = -\frac{2.2\text{ k}\Omega}{6.5\ \Omega} = -338.46$$

resulting in an overall gain of

$$A_{v_{T(\text{NL})}} = A_{v_1} A_{v_{2(\text{NL})}} = (-102.3)(-338.46) \cong \mathbf{34.6 \times 10^3}$$

The output voltage is then

$$V_o = A_{v_{T(\text{NL})}} V_i = (34.6 \times 10^3)(25\ \mu\text{V}) \cong \mathbf{865\text{ mV}}$$

b. The overall gain with the 10-kΩ load applied is

$$A_{v_T} = \frac{V_o}{V_i} = \frac{R_L}{R_L + Z_o} A_{v_{T(\text{NL})}} = \frac{10\text{ k}\Omega}{10\text{ k}\Omega + 2.2\text{ k}\Omega}(34.6 \times 10^3) \cong \mathbf{28.4 \times 10^3}$$

which is relatively close to the unloaded gain because R_L is relatively large compared to R_C.

c. The input impedance of the first stage is

$$Z_{i_1} = R_1 \| R_2 \| \beta r_e = 4.7\text{ k}\Omega \| 15\text{ k}\Omega \| (200)(6.5\ \Omega) = \mathbf{953.6\ \Omega}$$

whereas the output impedance for the second stage is

$$Z_{o_2} = R_C = \mathbf{2.2\text{ k}\Omega}$$

Cascode Connection

The cascode configuration has one of two configurations. In each case the collector of the leading transistor is connected to the emitter of the following transistor. One possible arrangement appears in Fig. 5.86; the second is shown in Fig. 5.87 in the following example.

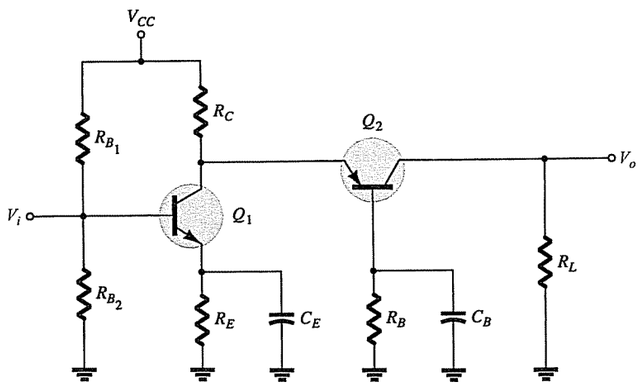


FIG. 5.86
Cascode configuration.

The arrangements provide a relatively high-input impedance with low voltage gain for the first stage to ensure the input Miller capacitance is at a minimum, whereas the following CB stage provides an excellent high-frequency response.

EXAMPLE 5.19 Calculate the no-load voltage gain for the cascode configuration of Fig. 5.87.



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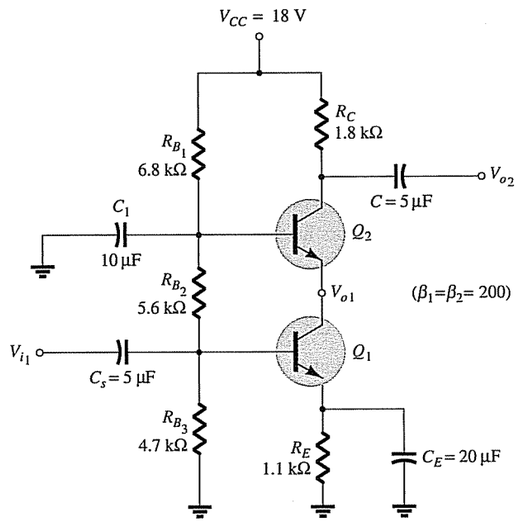


FIG. 5.87
Practical cascode circuit for Example 5.19.

Solution: The dc analysis results in

$$V_{B_1} = 4.9\text{ V}, \quad V_{B_2} = 10.8\text{ V}, \quad I_{C_1} \cong I_{C_2} = 3.8\text{ mA}$$

giving in a dynamic resistance for each transistor of

$$r_e = \frac{26\text{ mV}}{I_E} \cong \frac{26\text{ mV}}{3.8\text{ mA}} = 6.8\ \Omega$$

The loading on the transistor Q_1 is the input impedance of the Q_2 transistor in the CB configuration. The result is the replacement of R_C in the basic no-load equation for the gain of the CB configuration, with the input impedance of a CB configuration as follows:

$$A_{v_1} = -\frac{R_C}{r_e} = -\frac{r_e}{r_e} = -1$$

with the voltage gain for the second stage (common base) of

$$A_{v_2} = \frac{R_C}{r_e} = \frac{1.8\text{ k}\Omega}{6.8\ \Omega} = 265$$

The overall no-load gain is

$$A_{v_T} = A_{v_1} A_{v_2} = (-1)(265) = \mathbf{-265}$$

As expected, in Example 5.19, the CE stage provides a higher input impedance than can be expected from the CB stage. With a voltage gain of about 1 for the first stage, the Miller-effect input capacitance is kept quite low to support a good high-frequency response. A large voltage gain of 265 was provided by the CB stage to give the overall design a good input impedance level with desirable gain levels.

5.20 DARLINGTON CONNECTION

A very popular connection of two bipolar junction transistors for operation as one "super-beta" transistor is the Darlington connection shown in Fig. 5.88. The main feature of the Darlington connection is that the composite transistor acts as a single unit with a current

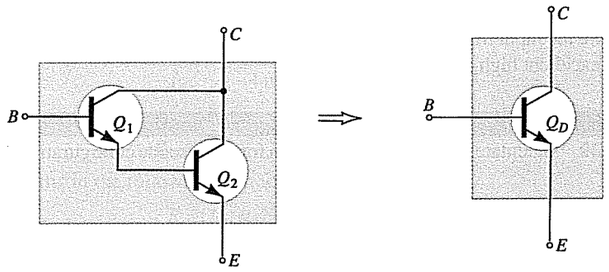


FIG. 5.88
Darlington combination.

gain that is the product of the current gains of the individual transistors. If the connection is made using two separate transistors having current gains of β_1 and β_2, the Darlington connection provides a current gain of

$$\boxed{\beta_D = \beta_1\beta_2} \tag{5.115}$$

If the two transistors are matched so that $\beta_1 = \beta_2 = \beta$, the Darlington connection provides a current gain of

$$\beta_D = \beta^2 \tag{5.116}$$

A Darlington transistor connection provides a transistor having a very large current gain, typically a few thousand.

Packaged Darlington Transistor

Because the Darlington connection is popular, one can obtain a single package containing two BJTs internally connected as a Darlington transistor. Figure 5.89 provides some specification sheet data on a typical Darlington pair. The current gain listed is that of the overall Darlington-connected transistor, the device providing externally only three terminals (base, emitter, and collector). One may consider the unit a single Darlington transistor having very high current gain when compared to other typical single transistors.

Parameter	Test Conditions	Min.	Max.
V_{BE}	$I_C = 100$ mA		1.8 V
h_{FE} (β_D)	$I_C = 10$ mA	4000	
	$I_C = 100$ mA	7000	70,000

FIG. 5.89
Specification information on an npn Darlington-connected silicon transistor package (2N999).

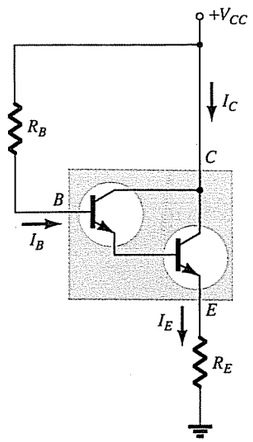


FIG. 5.90
Basic Darlington bias circuit.

DC Bias of Darlington Circuit

A basic Darlington circuit is shown in Fig. 5.90. A Darlington transistor having very high current gain β_D is used. The base current can be calculated from

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta_D R_E} \tag{5.117}$$

Although this equation is the same as for a regular transistor, the value of β_D is much greater and the value of V_{BE} is larger, as indicated by the data in the spec sheet of Fig. 5.89. The emitter current is then

$$I_E = (\beta_D + 1)I_B \approx \beta_D I_B \tag{5.118}$$

The dc voltages are

$$V_E = I_E R_E \tag{5.119}$$

$$V_B = V_E + V_{BE} \tag{5.120}$$

EXAMPLE 5.20 Calculate the dc bias voltages and currents in the circuit of Fig. 5.91.

Solution: The base current is

$$\text{Eq. (5.117):} \quad I_B = \frac{18\text{ V} - 1.6\text{ V}}{3.3\text{ M}\Omega + 8000(390\ \Omega)} \approx \mathbf{2.56\ \mu A}$$

The emitter current is then

$$\text{Eq. (5.118):} \quad I_E \approx 8000(2.56\ \mu\text{A}) = \mathbf{20.48\ mA} \approx I_C$$

The emitter dc voltage is

$$\text{Eq. (5.119):} \quad V_E = 20.48\text{ mA}(390\ \Omega) \approx \mathbf{8\ V}$$

and the base voltage is

$$\text{Eq. (5.120):} \quad V_B = 8\text{ V} + 1.6\text{ V} = \mathbf{9.6\ V}$$

The collector voltage is the supply value of

$$V_C = \mathbf{18\ V}$$

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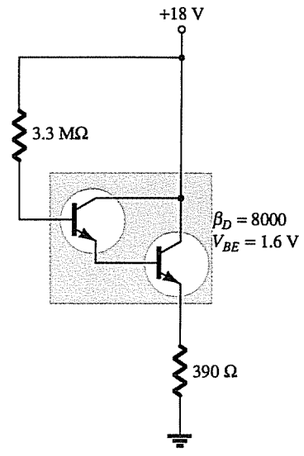


FIG. 5.91
Circuit for Example 5.20.

AC Equivalent Circuit

A Darlington emitter-follower circuit is shown in Fig. 5.92. The ac input signal is applied to the base of the Darlington transistor through capacitor C_1, with the ac output V_o obtained from the emitter through capacitor C_2. An ac equivalent circuit is drawn in Fig. 5.93. The Darlington transistor is replaced by an ac equivalent circuit made up of an input resistance r_i and an output current source $\beta_D I_b$.

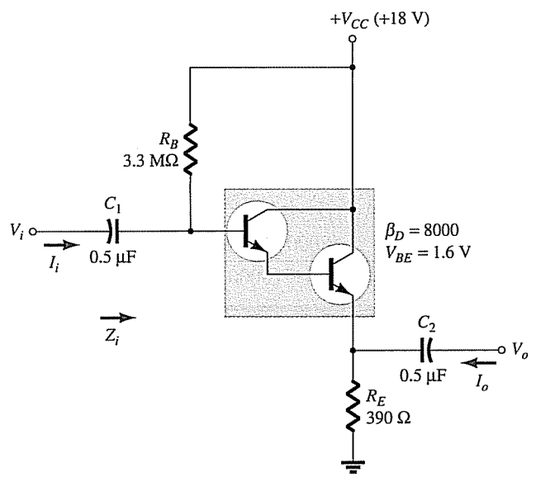


FIG. 5.92
Darlington emitter-follower circuit.

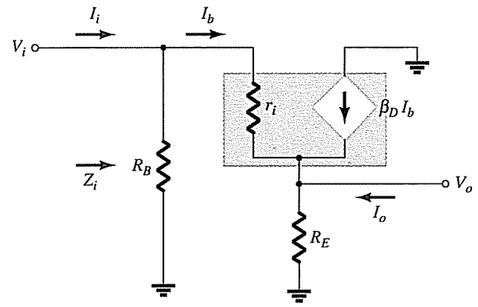


FIG. 5.93
AC equivalent circuit of a Darlington emitter-follower.

AC Input Impedance The ac base current through r_i is

$$I_b = \frac{V_i - V_o}{r_i} \tag{5.121}$$

Since

$$V_o = (I_b + \beta_D I_b)R_E \tag{5.122}$$

we can use Eq. (5.121) in Eq. (5.122) to obtain

$$I_b r_i = V_i - V_o = V_i - I_b(1 + \beta_D)R_E$$

Solving for V_i, we obtain

$$V_i = I_b[r_i + (1 + \beta_D)R_E] \approx I_b(r_i + \beta_D R_E)$$

The ac input impedance looking into the transistor base is then

$$\frac{V_i}{I_b} = r_i + \beta_D R_E$$

and that looking into the circuit is

$$\boxed{Z_i = R_B \| (r_i + \beta_D R_E)} \tag{5.123}$$

EXAMPLE 5.21 Calculate the input impedance of the circuit of Fig. 5.92 if $r_i = 5\,\text{k}\Omega$.

Solution:

Eq. (5.123): $Z_i = 3.3\,\text{M}\Omega \| [5\,\text{k}\Omega + (8000)(390\,\Omega)] = \mathbf{1.6\,M\Omega}$

AC Current Gain The ac output current through R_E is (see Fig. 5.93)

$$I_o = I_b + \beta_D I_b = (\beta_D + 1)I_b \approx \beta_D I_b$$

The transistor current gain is then

$$\frac{I_o}{I_b} = \beta_D$$

The ac current gain of the circuit is

$$A_i = \frac{I_o}{I_i} = \frac{I_o}{I_b} \cdot \frac{I_b}{I_i}$$

Applying the current-divider rule:

$$I_b = \frac{R_B}{(r_i + \beta_D R_E) + R_B} I_i \approx \frac{R_B}{R_B + \beta_D R_E} I_i$$

and the ac circuit current gain is

$$A_i = \frac{I_o}{I_b} \cdot \frac{I_b}{I_i} = \beta_D \frac{R_B}{R_B + \beta_D R_E} = \boxed{\frac{\beta_D R_B}{R_B + \beta_D R_E}} \tag{5.124}$$

EXAMPLE 5.22 Calculate the ac current gain of the circuit in Fig. 5.92.

Solution:

Eq. (12.16): $A_i = \dfrac{\beta_D R_B}{R_B + \beta_D R_E} = \dfrac{(8000)(3.3\,\text{M}\Omega)}{3.3\,\text{M}\Omega + (8000)(390\,\Omega)} = \mathbf{4112}$

AC Output Impedance The ac output impedance can be determined for the ac circuit shown in Fig. 5.94a. The output impedance seen by load R_L is determined by applying a voltage V_o and measuring the current I_o (with input V_i set to zero). Figure 5.94b shows this situation. Solving for I_o yields

$$I_o = I' - I_b' - \beta_D I_b = \frac{V_o}{R_E} - \left(\frac{-V_o}{r_i}\right) - \beta_D\left(\frac{-V_o}{r_i}\right)$$

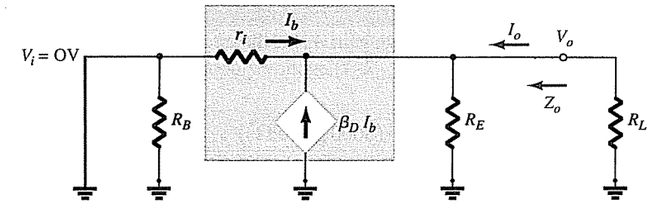
$$= \left(\frac{1}{R_E} + \frac{1}{r_i} + \frac{\beta_D}{r_i}\right)V_o$$

Solving for Z_o gives

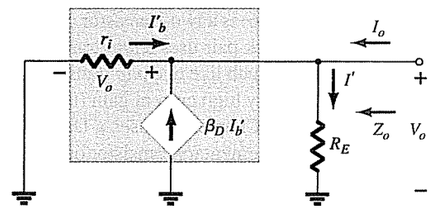
$$Z_o = \frac{V_o}{I_o} = \frac{1}{1/R_E + 1/r_i + \beta_D/r_i}$$

and

$$\boxed{Z_o = R_E \| r_i \| \frac{r_i}{\beta_D} \approx \frac{r_i}{\beta_D}} \tag{5.125}$$



(a)



(b)

FIG. 5.94
AC equivalent circuit for determining Z_o.

EXAMPLE 5.23 Calculate the output impedance of the circuit in Fig. 5.92.

Solution:

Eq. (5.125): $Z_o = 390\,\Omega \| 5\,\text{k}\Omega \| \dfrac{5\,\text{k}\Omega}{8000} \approx \dfrac{5\,\text{k}\Omega}{8000} = \mathbf{0.625\,\Omega}$

AC Voltage Gain The ac voltage gain for the circuit of Fig. 5.92 can be determined using the ac equivalent circuit of Fig. 5.95. Since

$$V_o = (I_b + \beta_D I_b)R_E = I_b(R_E + \beta_D R_E),$$

and

$$V_i = I_b r_i + (I_b + \beta_D I_b)R_E$$

from which we obtain

$$V_i = I_b(r_i + R_E + \beta_D R_E)$$

so that

$$V_o = \frac{V_i}{r_i + (R_E + \beta_D R_E)}(R_E + \beta_D R_E)$$

$$\boxed{A_v = \frac{V_o}{V_i} = \frac{R_E + \beta_D R_E}{r_i + (R_E + \beta_D R_E)} \approx 1} \tag{5.126}$$

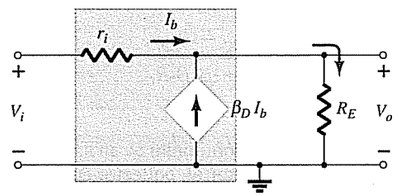


FIG. 5.95
AC equivalent circuit for determining A_v.

EXAMPLE 5.24 Calculate the ac voltage gain A_v for the circuit of Fig. 5.92.

Solution:

$$A_v = \frac{390\ \Omega + (8000)(390\ \Omega)}{5\ \text{k}\Omega + [390\ \Omega + (8000)(390\ \Omega)]} = \mathbf{0.998}$$

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5.21 FEEDBACK PAIR

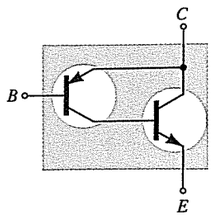


FIG. 5.96
Feedback pair connection.

The feedback pair connection (see Fig. 5.96) is a two-transistor circuit that operates like the Darlington circuit. Notice that the feedback pair uses a *pnp* transistor driving an *npn* transistor, the two devices acting effectively much like one *pnp* transistor. As with a Darlington connection, the feedback pair provides very high current gain (the product of the transistor current gains). A typical application (see Chapter 12) uses a Darlington connection and a feedback pair connection to provide complementary transistor operation. A practical circuit using a feedback pair is provided in Fig. 5.97. Some consideration of the dc bias and ac operation will provide better understanding of how the connection works.

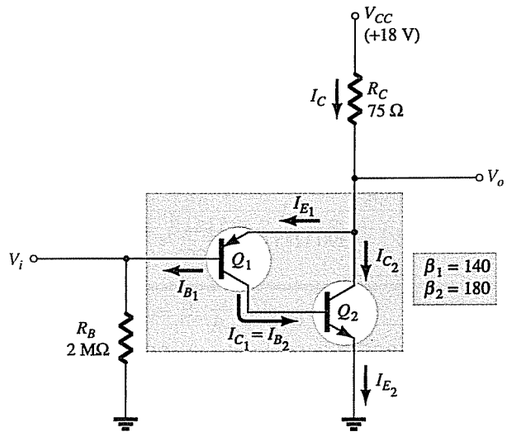


FIG. 5.97
Operation of a feedback pair.

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DC Bias

The dc bias calculations that follow use practical simplifications wherever possible to provide simpler results. From the Q_1 base–emitter loop, one obtains

$$V_{CC} - I_C R_C - V_{EB_1} - I_{B_1} R_B = 0$$
$$V_{CC} - \beta_1\beta_2 I_{B_1} R_C - V_{EB_1} - I_{B_1} R_B = 0$$

The base current is then

$$I_{B_1} = \frac{V_{CC} - V_{EB_1}}{R_B + \beta_1\beta_2 R_C} \tag{5.127}$$

The collector current of Q_1 is

$$I_{C_1} = \beta_1 I_{B_1} = I_{B_2}$$

which is also the base Q_2 current. The transistor Q_2 collector current is

$$I_{C_2} = \beta_2 I_{B_2} \approx I_{E_2}$$

so that the current through R_C is

$$I_C = I_{E_1} + I_{C_2} \approx I_{C_1} + I_{C_2} \approx I_{C_2} \tag{5.128}$$

EXAMPLE 5.25 Calculate the dc bias currents and voltages for the circuit of Fig. 5.97 to provide V_o at one-half the supply voltage ($I_C R_C = 9$ V).

Solution:

$$I_{B_1} = \frac{18\ \text{V} - 0.7\ \text{V}}{2\ \text{M}\Omega + (140)(180)(75\ \Omega)} = \frac{17.3\ \text{V}}{3.89 \times 10^6} = 4.45\ \mu\text{A}$$

The base Q_2 current is then

$$I_{B_2} = I_{C_1} = \beta_1 I_{B_1} = 140(4.45\ \mu\text{A}) = \mathbf{0.623\ mA}$$

resulting in a Q_2 collector current of

$$I_{C_2} = \beta_2 I_{B_2} = 180(0.623\ \text{mA}) = \mathbf{112.1\ mA}$$

and the current through R_C is then

$$\text{Eq. (5.128): } I_C = I_{E_1} + I_{C_2} = 0.623\ \text{mA} + 112.1\ \text{mA} \approx I_{C_2} = \mathbf{112.1\ mA}$$

The dc voltage at the output is thus

$$V_o(\text{dc}) = V_{CC} - I_C R_C = 18\ \text{V} - 112.1\ \text{mA}(75\ \Omega) = \mathbf{9.6\ V}$$

and

$$V_i(\text{dc}) = V_o(\text{dc}) - V_{BE} = 9.6\ \text{V} - 0.7\ \text{V} = \mathbf{8.9\ V}$$

AC Operation

The ac equivalent circuit for that of Fig. 5.97 is drawn in Fig. 5.98. The circuit is first drawn in Fig. 5.98a to show clearly each transistor and the base and collector resistor placement. The ac equivalent circuit is then redrawn in Fig. 5.98b to permit analysis.

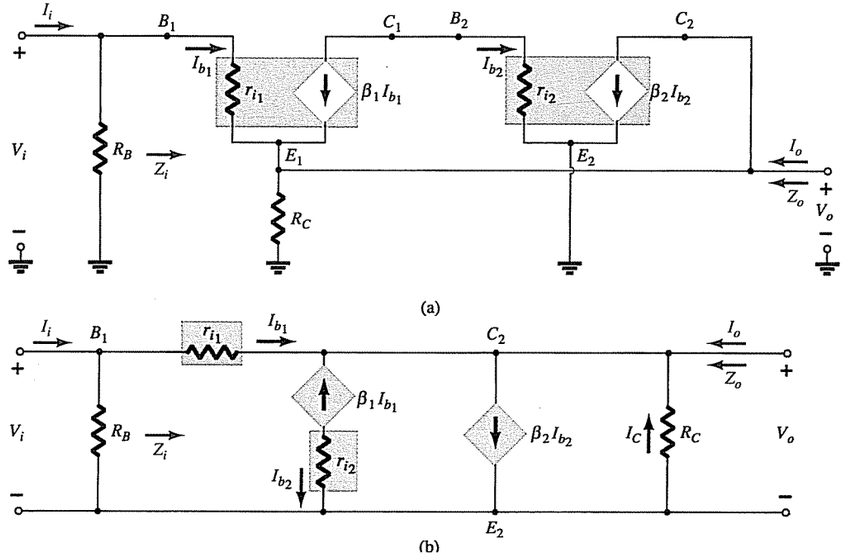


FIG. 5.98
AC equivalent of Fig. 5.97.

AC Input Impedance, Z_i The ac input impedance seen looking into the base of transistor Q_1 is determined (refer to Fig. 5.98b) as follows:

$$I_{b_1} = \frac{V_i - V_o}{r_{i_1}}$$

where

$$V_o = -I_C R_C \approx (-\beta_1 I_{b_1} + \beta_2 I_{b_2}) R_C \approx (\beta_2 I_{b_2}) R_C$$

so that

$$I_{b_1} r_{i_1} = V_i - V_o \approx V_i - \beta_2 I_{b_2} R_C$$
$$I_{b_1} r_{i_1} + \beta_2(\beta_1 I_{b_1}) R_C = V_i \quad (\text{Since } I_{b_2} = I_{C_1} = \beta_1 I_{b_1})$$
$$\frac{V_i}{I_{b_1}} = r_{i_1} + \beta_1\beta_2 R_C$$

Including the base-bias resistance, we obtain

$$\boxed{Z_i = R_B \| (r_{i_1} + \beta_1\beta_2 R_C)} \tag{5.129}$$

AC Current Gain, A_i The ac current gain can be determined as follows:

$$I_o = \beta_2 I_{b_2} - \beta_1 I_{b_1} - I_{b_1}$$
$$= \beta_2(\beta_1 I_{b_1}) - (1 + \beta_1) I_{b_1} \approx \beta_1\beta_2 I_{b_1}$$
$$\frac{I_o}{I_{b_1}} = \beta_1\beta_2$$

Including R_B, the current gain is

$$\boxed{A_i = \frac{I_o}{I_i} = \frac{I_o}{I_{b_1}} \cdot \frac{I_{b_1}}{I_i} = \beta_1\beta_2 \frac{R_B}{R_B + Z_i}} \tag{5.130}$$

AC Output Impedance, Z_o Z_o can be obtained by applying a voltage V_o with V_i set to 0. The resulting analysis gives

$$\boxed{Z_o = \frac{V_o}{I_o} = R_C \| r_{i_1} \| \frac{r_{i_1}}{\beta_1} \| \frac{r_{i_1}}{\beta_1\beta_2} \cong \frac{r_{i_1}}{\beta_1\beta_2}} \tag{5.131}$$

which results in a low output impedance.

AC Voltage Gain, A_v The output voltage V_o is

$$V_o = -I_C R_C \approx \beta_1\beta_2 I_{b_1} R_C$$

Since

$$I_{b_1} = \frac{V_i - V_o}{r_{i_1}}$$

and

$$V_o = V_i - I_{b_1} r_{i_1} = V_i - \frac{V_o}{\beta_1\beta_2 R_C} r_{i_1}$$

we obtain

$$\boxed{A_v = \frac{V_o}{V_i} = \frac{1}{1 + r_{i_1}/(\beta_1\beta_2 R_C)} = \frac{\beta_1\beta_2 R_C}{\beta_1\beta_2 R_C + r_{i_1}}} \tag{5.132}$$

EXAMPLE 5.26 Calculate the ac circuit values of Z_i, Z_o, A_i, and A_v for the circuit of Fig. 5.97. Assume that $r_{i_1} = 3\,\text{k}\Omega$.

Solution:

$$Z_i \approx R_B \| (r_{i_1} + \beta_1\beta_2 R_C) = 2\,\text{M}\Omega \| [3\,\text{k}\Omega + (140)(180)(75\,\Omega)]$$
$$\approx \mathbf{974\,k\Omega}$$
$$A_i = \beta_1\beta_2 \frac{R_B}{R_B + Z_i} = (140)(180)\left(\frac{2\,\text{M}\Omega}{2\,\text{M}\Omega + 974\,\text{k}\Omega}\right)$$
$$= \mathbf{16.95 \times 10^3}$$
$$Z_o \approx \frac{r_{i_1}}{\beta_1\beta_2} = \frac{3 \times 10^3}{(140)(180)} = \mathbf{0.12\,\Omega}$$

and

$$A_v = \frac{\beta_1\beta_2 R_C}{\beta_1\beta_2 R_C + r_{i_1}} = \frac{(140)(180)(75\,\Omega)}{(140)(180)(75\,\Omega) + 3000\,\Omega}$$
$$= \mathbf{0.9984 \approx 1}$$

Example 5.26 shows that the feedback pair connection provides operation with voltage gain very near 1 (just as with a Darlington emitter-follower), a very high current gain, a very low output impedance, and a high input impedance.

5.22 CURRENT MIRROR CIRCUITS

A current mirror circuit (see Fig. 5.99) provides a constant current and is used primarily in integrated circuits. The constant current is obtained from an output current, which is the reflection or mirror of a constant current developed on one side of the circuit. The circuit is particularly suited to IC manufacture since the circuit requires that the transistors used have identical base–emitter voltage drops and identical values of beta—results best achieved when transistors are formed at the same time in IC manufacture. In Fig. 5.99 the current I_X set by transistor Q_1 and resistor R_X is mirrored in the current I through transistor Q_2.

The current I_X and I can be obtained using the circuit currents listed in Fig. 5.100. We assume that the emitter current (I_E) for both transistors is the same (Q_1 and Q_2 being fabricated near each other on the same chip). The two transistor base currents are then approximately

$$I_B = \frac{I_E}{\beta + 1} \approx \frac{I_E}{\beta}$$

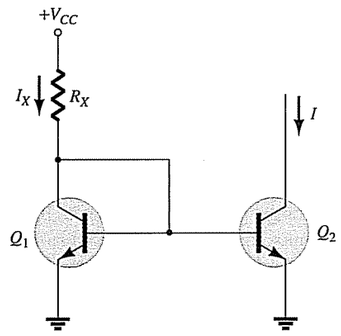


FIG. 5.99
Current mirror circuit.

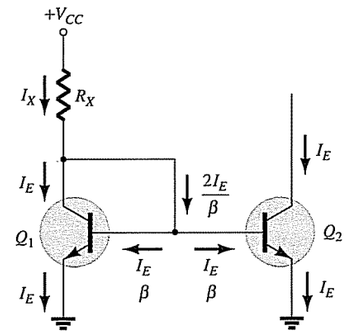


FIG. 5.100
Circuit currents for current mirror circuit.

The collector current of each transistor is then

$$I_C \approx I_E$$

Finally, the current I_X through resistor R_X is

$$I_X = I_E + \frac{2I_E}{\beta} = \frac{\beta I_E}{\beta} + \frac{2I_E}{\beta} = \frac{\beta + 2}{\beta} I_E \approx I_E$$

In summary, the constant current provided at the collector of Q_2 mirrors that of Q_1. Since

$$I_X = \frac{V_{CC} - V_{BE}}{R_X} \tag{5.133}$$

the current I_X set by V_{CC} and R_X is mirrored in the current into the collector of Q_2.

Transistor Q_1 is referred to as a diode-connected transistor because the base and the collector are shorted together.

EXAMPLE 5.27 Calculate the mirrored current I in the circuit of Fig. 5.101.


PSpice

Solution:

$$\text{Eq. (5.133): } I = I_X = \frac{V_{CC} - V_{BE}}{R_X} = \frac{12\,\text{V} - 0.7\,\text{V}}{1.1\,\text{k}\Omega} = \mathbf{10.27\,mA}$$

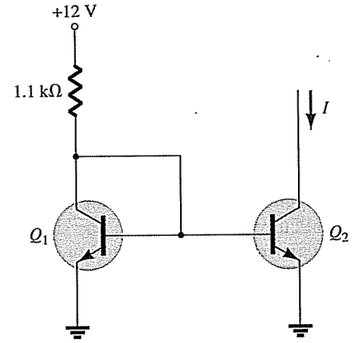


FIG. 5.101
Current mirror circuit for Example 5.27.

EXAMPLE 5.28 Calculate the current I through each of the transistor Q_2 and Q_3 in the circuit of Fig. 5.102.

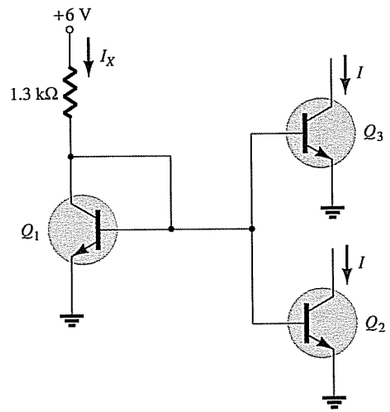


FIG. 5.102
Current mirror circuit for Example 5.28.

Solution: The current I_X is

$$I_X = I_E + \frac{3I_E}{\beta} = \frac{\beta + 3}{\beta} I_E \approx I_E$$

Therefore,

$$I \approx I_X = \frac{V_{CC} - V_{BE}}{R_X} = \frac{6\,\text{V} - 0.7\,\text{V}}{1.3\,\text{k}\Omega} = \mathbf{4.08\ mA}$$

Figure 5.103 shows another form of current mirror to provide higher output impedance than that of Fig. 5.99. The current through R_X is

$$I_X = \frac{V_{CC} - 2V_{BE}}{R_X} \approx I_E + \frac{I_E}{\beta} = \frac{\beta + 1}{\beta} I_E \approx I_E$$

Assuming that Q_1 and Q_2 are well matched, we find that the output current I is held constant at

$$I \approx I_E = I_X$$

Again we see that the output current I is a mirrored value of the current set by the fixed current through R_X.

Figure 5.104 shows still another form of current mirror. The junction field effect transistor (see next chapter) provides a constant current set at the value of I_{DSS}. This current is mirrored, resulting in a current through Q_2 of the same value:

$$I = I_{DSS}$$

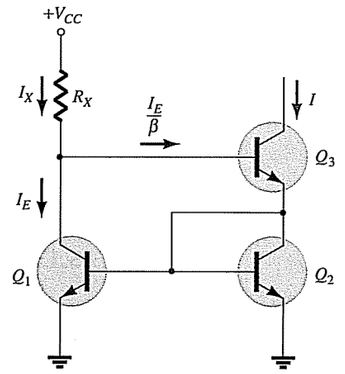


FIG. 5.103
Current mirror circuit with higher output impedance.

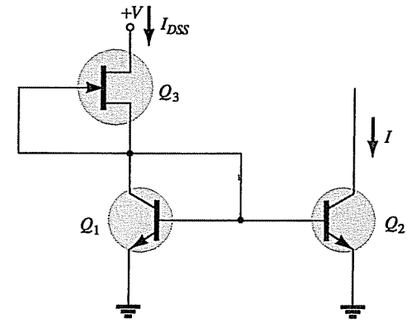


FIG. 5.104
Current mirror connection.

5.23 CURRENT SOURCE CIRCUITS

The concept of a power supply provides the starting point in our consideration of current source circuits. A practical voltage source (Fig. 5.105a) is a voltage supply in series with a resistance. An ideal voltage source has $R = 0$, whereas a practical source includes some small resistance. A practical current source (Fig. 5.105b) is a current supply in parallel with a resistance. An ideal current source has $R = \infty\Omega$, whereas a practical current source includes some very large resistance.

An ideal current source provides a constant current regardless of the load connected to it. There are many uses in electronics for a circuit providing a constant current at a very high

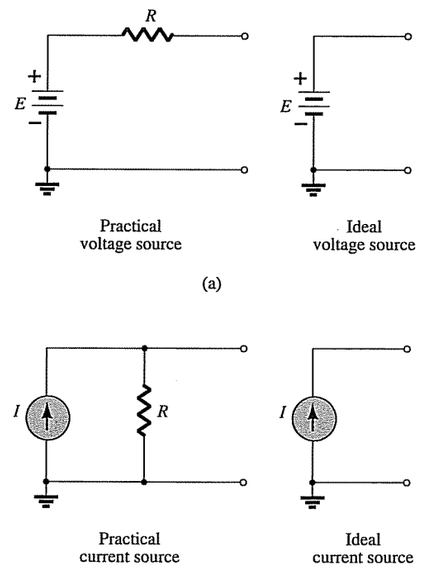


FIG. 5.105
Voltage and current sources.

impedance. Constant-current circuits can be built using bipolar devices, FET devices, and a combination of these components. There are circuits used in discrete form and others more suitable for operation in integrated circuits.

Bipolar Transistor Constant-Current Source

Bipolar transistors can be connected in a circuit that acts as a constant-current source in a number of ways. Figure 5.106 shows a circuit using a few resistors and an *npn* transistor for operation as a constant-current circuit. The current through I_E can be determined as follows. Assuming that the base input impedance is much larger than R_1 or R_2, we have

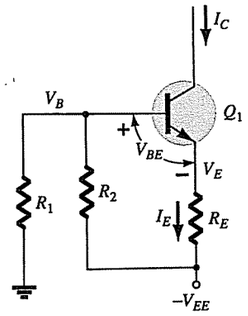


FIG. 5.106
Discrete constant-current source.

$$V_B = \frac{R_1}{R_1 + R_2}(-V_{EE})$$

and

$$V_E = V_B - 0.7\,\text{V}$$

with

$$I_E = \frac{V_E - (-V_{EE})}{R_E} \approx I_C \tag{5.134}$$

where I_C is the constant current provided by the circuit of Fig. 5.106.

EXAMPLE 5.29 Calculate the constant current I in the circuit of Fig. 5.107.

Solution:

$$V_B = \frac{R_1}{R_1 + R_2}(-V_{EE}) = \frac{5.1\,\text{k}\Omega}{5.1\,\text{k}\Omega + 5.1\,\text{k}\Omega}(-20\,\text{V}) = -10\,\text{V}$$

$$V_E = V_B - 0.7\,\text{V} = -10\,\text{V} - 0.7\,\text{V} = -10.7\,\text{V}$$

$$I = I_E = \frac{V_E - (-V_{EE})}{R_E} = \frac{-10.7\,\text{V} - (-20\,V)}{2\,\text{k}\Omega}$$

$$= \frac{9.3\,\text{V}}{2\,\text{k}\Omega} = \mathbf{4.65\ mA}$$

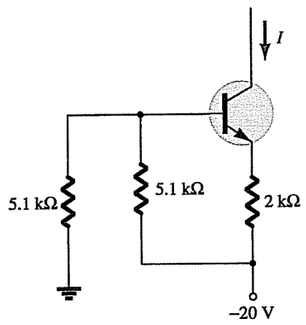


FIG. 5.107
Constant-current source for Example 5.29.

Transistor/Zener Constant-Current Source

Replacing resistor R_2 with a Zener diode, as shown in Fig. 5.108, provides an improved constant-current source over that of Fig. 5.106. The Zener diode results in a constant current calculated using the base-emitter KVL (Kirchhoff voltage loop) equation. The value of I can be calculated using

$$I \approx I_E = \frac{V_Z - V_{BE}}{R_E} \tag{5.135}$$

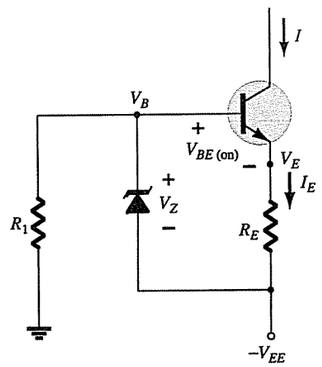


FIG. 5.108
Constant-current circuit using Zener diode.

A major point to consider is that the constant current depends on the Zener diode voltage, which remains quite constant, and the emitter resistor R_E. The voltage supply V_{EE} has no effect on the value of I.

EXAMPLE 5.30 Calculate the constant current I in the circuit of Fig. 5.109.

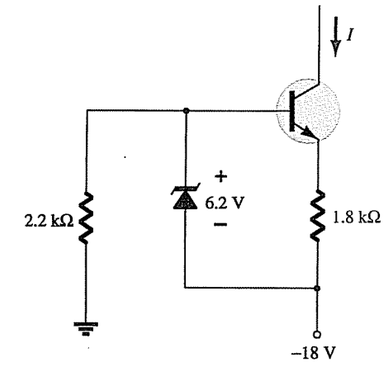


FIG. 5.109
Constant-current circuit for Example 5.30.

Solution:

$$\text{Eq. (5.135): } I = \frac{V_Z - V_{BE}}{R_E} = \frac{6.2\,\text{V} - 0.7\,\text{V}}{1.8\,\text{k}\Omega} = 3.06\,\text{mA} \approx \mathbf{3\ mA}$$

5.24 APPROXIMATE HYBRID EQUIVALENT CIRCUIT

The analysis using the approximate hybrid equivalent circuit of Fig. 5.110 for the common-emitter configuration and of Fig. 5.111 for the common-base configuration is very similar to that just performed using the r_e model. Although priorities do not permit a detailed analysis of all the configurations discussed thus far, a brief overview of some of the most important will be included in this section to demonstrate the similarities in approach and the resulting equations.

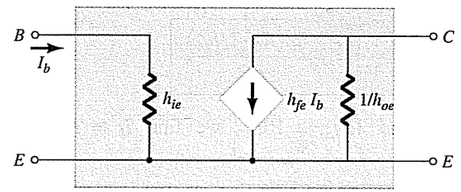


FIG. 5.110
Approximate common-emitter hybrid equivalent circuit.

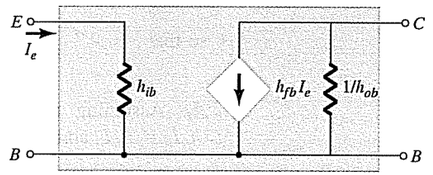


FIG. 5.111
Approximate common-base hybrid equivalent circuit.

Since the various parameters of the hybrid model are specified by a data sheet or experimental analysis, the dc analysis associated with use of the r_e model is not an integral part of the use of the hybrid parameters. In other words, when the problem is presented, the parameters such as h_{ie}, h_{fe}, h_{ib}, and so on, are specified. Keep in mind, however, that the hybrid parameters and components of the r_e model are related by the following equations, as discussed earlier in this chapter: $h_{ie} = \beta r_e$, $h_{fe} = \beta$, $h_{oe} = 1/r_o$, $h_{fb} = -\alpha$, and $h_{ib} = r_e$.

Fixed-Bias Configuration

For the fixed-bias configuration of Fig. 5.112, the small-signal ac equivalent network will appear as shown in Fig. 5.113 using the approximate common-emitter hybrid equivalent model. Compare the similarities in appearance with Fig. 5.36 and the r_e model analysis. The similarities suggest that the analyses will be quite similar, and the results of one can be directly related to the other.

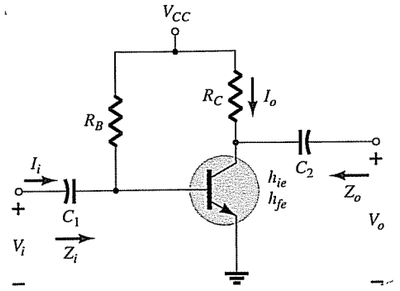


FIG. 5.112
Fixed-bias configuration.

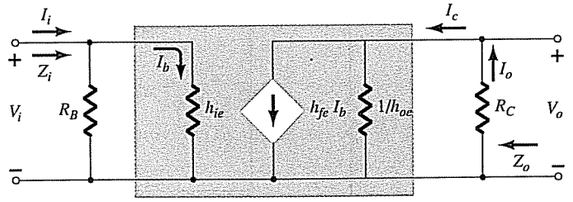


FIG. 5.113
Substituting the approximate hybrid equivalent circuit into the ac equivalent network of Fig. 5.112.

Z_i From Fig. 5.113,

$$\boxed{Z_i = R_B \| h_{ie}} \tag{5.136}$$

Z_o From Fig. 5.113,

$$\boxed{Z_o = R_C \| 1/h_{oe}} \tag{5.137}$$

A_v Using $R' = 1/h_{oe} \| R_C$, we obtain

$$V_o = -I_o R' = -I_C R'$$
$$= -h_{fe} I_b R'$$

and

$$I_b = \frac{V_i}{h_{ie}}$$

with

$$V_o = -h_{fe} \frac{V_i}{h_{ie}} R'$$

so that

$$\boxed{A_v = \frac{V_o}{V_i} = -\frac{h_{ie}(R_C \| 1/h_{oe})}{h_{ie}}} \tag{5.138}$$

A_i Assuming that $R_B \gg h_{ie}$ and $1/h_{oe} \geq 10R_C$, we find $I_b \cong I_i$ and $I_o = I_c = h_{fe} I_b = h_{fe} I_i$, and so

$$\boxed{A_i = \frac{I_o}{I_i} \cong h_{fe}} \tag{5.139}$$

EXAMPLE 5.31 For the network of Fig. 5.114, determine:

a. Z_i.
b. Z_o.
c. A_v.
d. A_i.

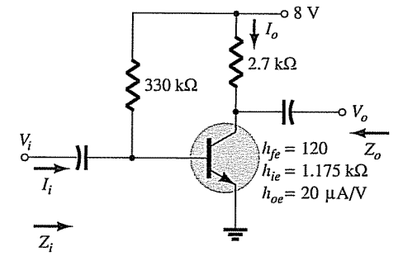


FIG. 5.114
Example 5.31.

Solution:

a. $Z_i = R_B \| h_{ie} = 330\,\text{k}\Omega \| 1.175\,\text{k}\Omega$
$\cong h_{ie} = \mathbf{1.171\,k\Omega}$

b. $r_o = \dfrac{1}{h_{oe}} = \dfrac{1}{20\,\mu\text{A/V}} = 50\,\text{k}\Omega$

$Z_o = \dfrac{1}{h_{oe}} \| R_C = 50\,\text{k}\Omega \| 2.7\,\text{k}\Omega = \mathbf{2.56\,k\Omega} \cong R_C$

c. $A_v = -\dfrac{h_{fe}(R_C \| 1/h_{oe})}{h_{ie}} = -\dfrac{(120)(2.7\,\text{k}\Omega \| 50\,\text{k}\Omega)}{1.171\,\text{k}\Omega} = \mathbf{-262.34}$

d. $A_i \cong h_{fe} = \mathbf{120}$

Voltage-Divider Configuration

For the voltage-divider bias configuration of Fig. 5.115, the resulting small-signal ac equivalent network will have the same appearance as Fig. 5.113, with R_B replaced by $R' = R_1 \| R_2$.

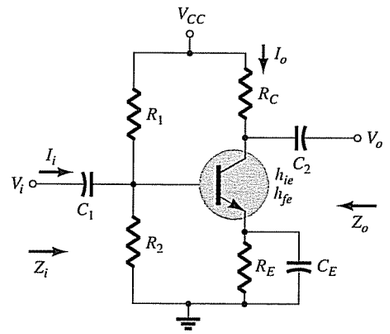


FIG. 5.115
Voltage-divider bias configuration.

Z_i From Fig. 5.113 with $R_B = R'$,

$$\boxed{Z_i = R_1 \| R_2 \| h_{ie}} \tag{5.140}$$

Z_o From Fig. 5.113,

$$\boxed{Z_o \cong R_C} \tag{5.141}$$

A_v

$$A_v = -\frac{h_{fe}(R_C \| 1/h_{oe})}{h_{ie}} \tag{5.142}$$

A_i

$$A_i = \frac{h_{fe}R'}{R' + h_{ie}} \tag{5.143}$$

Unbypassed Emitter-Bias Configuration

For the CE unbypassed emitter-bias configuration of Fig. 5.116, the small-signal ac model will be the same as Fig. 5.44, with βr_e replaced by h_{ie} and βI_b by $h_{fe}I_b$. The analysis will proceed in the same manner.

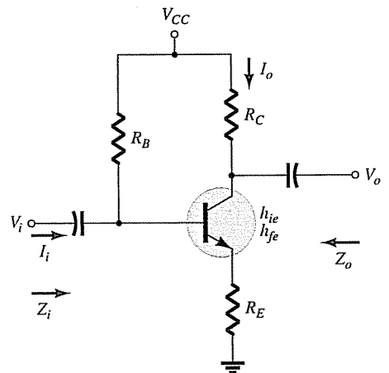


FIG. 5.116
CE unbypassed emitter-bias configuration.

Z_i

$$Z_b \cong h_{fe}R_E \tag{5.144}$$

and

$$Z_i = R_B \| Z_b \tag{5.145}$$

Z_o

$$Z_o = R_C \tag{5.146}$$

A_v

$$A_v = -\frac{h_{fe}R_C}{Z_b} \cong -\frac{h_{fe}R_C}{h_{fe}R_E}$$

and

$$A_v \cong -\frac{R_C}{R_E} \tag{5.147}$$

A_i

$$A_i = -\frac{h_{fe}R_B}{R_B + Z_b} \tag{5.148}$$

or

$$A_i = -A_v\frac{Z_i}{R_C} \tag{5.149}$$

Emitter-Follower Configuration

For the emitter-follower of Fig. 5.52, the small-signal ac model will match Fig. 5.117, with $\beta r_e = h_{ie}$ and $\beta = h_{fe}$. The resulting equations will therefore be quite similar.

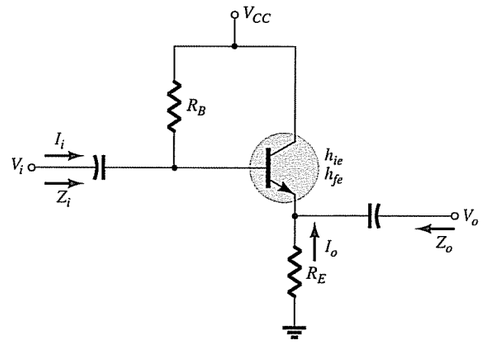


FIG. 5.117
Emitter-follower configuration.

Z_i

$$Z_b \cong h_{fe}R_E \tag{5.150}$$

$$Z_i = R_B \| Z_b \tag{5.151}$$

Z_o For Z_o, the output network defined by the resulting equations will appear as shown in Fig. 5.118. Review the development of the equations in Section 5.11 and

$$Z_o = R_E \| \frac{h_{ie}}{1 + h_{fe}}$$

or, since $1 + h_{fe} \cong h_{fe}$,

$$Z_o \cong R_E \| \frac{h_{ie}}{h_{fe}} \tag{5.152}$$

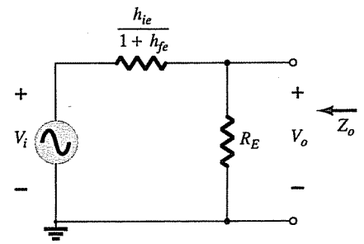


FIG. 5.118
Defining Z_o for the emitter-follower configuration.

A_v For the voltage gain, the voltage-divider rule can be applied to Fig. 5.118 as follows:

$$V_o = \frac{R_E(V_i)}{R_E + h_{ie}/(1 + h_{fe})}$$

but, since $1 + h_{fe} \cong h_{fe}$,

$$A_v = \frac{V_o}{V_i} \cong \frac{R_E}{R_E + h_{ie}/h_{fe}} \tag{5.153}$$

A_i

$$A_i = \frac{h_{fe} R_B}{R_B + Z_b} \tag{5.154}$$

or

$$A_i = -A_v \frac{Z_i}{R_E} \tag{5.155}$$

Common-Base Configuration

The last configuration to be examined with the approximate hybrid equivalent circuit will be the common-base amplifier of Fig. 5.119. Substituting the approximate common-base hybrid equivalent model results in the network of Fig. 5.120, which is very similar to Fig. 5.58.

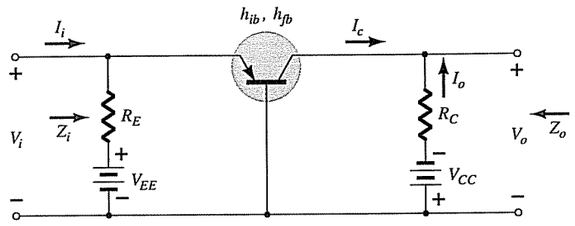


FIG. 5.119
Common-base configuration.

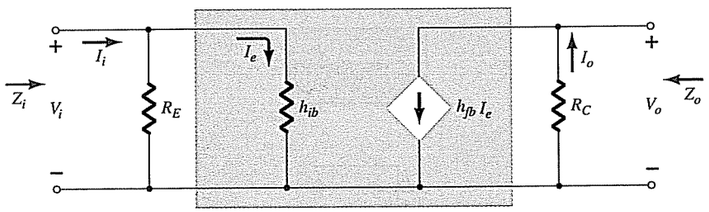


FIG. 5.120
Substituting the approximate hybrid equivalent circuit into the ac equivalent network of Fig. 5.119.

We have the following results from Fig. 5.120.

Z_i

$$Z_i = R_E \| h_{ib} \tag{5.156}$$

Z_o

$$Z_o = R_C \tag{5.157}$$

A_v

$$V_o = -I_o R_C = -(h_{fb} I_e) R_C$$

with $$I_e = \frac{V_i}{h_{ib}} \quad \text{and} \quad V_o = -h_{fb} \frac{V_i}{h_{ib}} R_C$$

so that

$$A_v = \frac{V_o}{V_i} = -\frac{h_{fb} R_C}{h_{ib}} \tag{5.158}$$

A_i

$$A_i = \frac{I_o}{I_i} = h_{fb} \cong -1 \tag{5.159}$$

EXAMPLE 5.32 For the network of Fig. 5.121, determine:

a. Z_i.
b. Z_o.
c. A_v.
d. A_i.

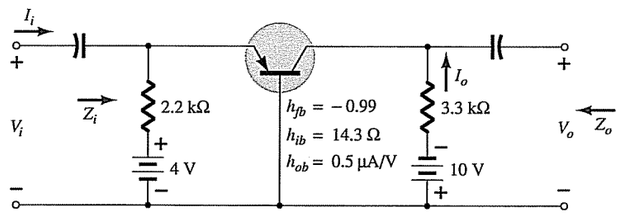


FIG. 5.121
Example 5.32.

Solution:

a. $Z_i = R_E \| h_{ib} = 2.2\,\text{k}\Omega \| 14.3\,\Omega = \mathbf{14.21\,\Omega} \cong h_{ib}$

b. $r_o = \frac{1}{h_{ob}} = \frac{1}{0.5\,\mu\text{A/V}} = 2\,\text{M}\Omega$

$Z_o = \frac{1}{h_{ob}} \| R_C \cong R_C = \mathbf{3.3\,k\Omega}$

c. $A_v = -\frac{h_{fb} R_C}{h_{ib}} = -\frac{(-0.99)(3.3\,\text{k}\Omega)}{14.21} = \mathbf{229.91}$

d. $A_i \cong h_{fb} = \mathbf{-1}$

The remaining configurations that were not analyzed in this section are left as an exercise in the problem section of this chapter. It is assumed that the analysis above clearly reveals the similarities in approach using the r_e or approximate hybrid equivalent models, thereby removing any real difficulty with analyzing the remaining networks of the earlier sections.

5.25 COMPLETE HYBRID EQUIVALENT MODEL

The analysis of Section 5.23 was limited to the approximate hybrid equivalent circuit with some discussion about the output impedance. In this section, we employ the complete equivalent circuit to show the effect of h_r and define in more specific terms the effect of h_o. It is important to realize that since the hybrid equivalent model has the same appearance for the common-base, common-emitter, and common-collector configurations, the equations developed in this section can be applied to each configuration. It is only necessary to insert

the parameters defined for each configuration. That is, for a common-base configuration, h_{fb}, h_{ib}, and so on, are employed, whereas for a common-emitter configuration, h_{fe}, h_{ie}, and so on, are used. Recall that Appendix B permits a conversion from one set to the other if one set is provided and the other is required.

Consider the general configuration of Fig. 5.122 with the two-port parameters of particular interest. The complete hybrid equivalent model is then substituted in Fig. 5.123 using parameters that do not specify the type of configuration. In other words, the solutions will be in terms of h_i, h_r, h_f, and h_o. Unlike the analysis of previous sections of this chapter, here the current gain A_i will be determined first since the equations developed will prove useful in the determination of the other parameters.

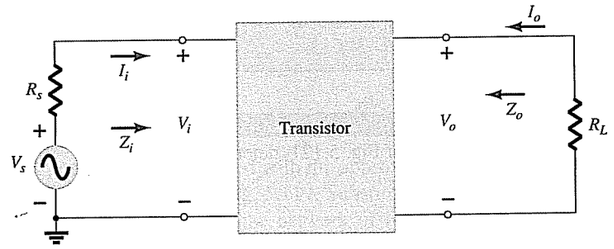


FIG. 5.122
Two-port system.

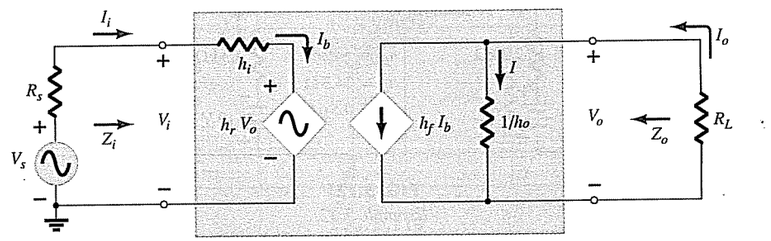


FIG. 5.123
Substituting the complete hybrid equivalent circuit into the two-port system of Fig. 5.122.

Current Gain, $A_i = I_o/I_i$

Applying Kirchhoff's current law to the output circuit yields

$$I_o = h_f I_b + I = h_f I_i + \frac{V_o}{1/h_o} = h_f I_i + h_o V_o$$

Substituting $V_o = -I_o R_L$ gives

$$I_o = h_f I_i - h_o R_L I_o$$

Rewriting the equation above, we have

$$I_o + h_o R_L I_o = h_f I_i$$

and

$$I_o(1 + h_o R_L) = h_f I_i$$

so that

$$\boxed{A_i = \frac{I_o}{I_i} = \frac{h_f}{1 + h_o R_L}} \qquad (5.160)$$

Note that the current gain reduces to the familiar result of $A_i = h_f$ if the factor $h_o R_L$ is sufficiently small compared to 1.

Voltage Gain, $A_v = V_o/V_i$

Applying Kirchhoff's voltage law to the input circuit results in

$$V_i = I_i h_i + h_r V_o$$

Substituting $I_i = (1 + h_o R_L) I_o / h_f$ from Eq. (5.160) and $I_o = -V_o/R_L$ from above results in

$$V_i = \frac{-(1 + h_o R_L) h_i}{h_f R_L} V_o + h_r V_o$$

Solving for the ratio V_o/V_i yields

$$\boxed{A_v = \frac{V_o}{V_i} = \frac{-h_f R_L}{h_i + (h_i h_o - h_f h_r) R_L}} \qquad (5.161)$$

In this case, the familiar form of $A_v = -h_f R_L / h_i$ returns if the factor $(h_i h_o - h_f h_r) R_L$ is sufficiently small compared to h_i.

Input Impedance, $Z_i = V_i/I_i$

For the input circuit,

$$V_i = h_i I_i + h_r V_o$$

Substituting

$$V_o = -I_o R_L$$

we have

$$V_i = h_i I_i - h_r R_L I_o$$

Since

$$A_i = \frac{I_o}{I_i}$$

$$I_o = A_i I_i$$

so that the equation above becomes

$$V_i = h_i I_i - h_r R_L A_i I_i$$

Solving for the ratio V_i/I_i, we obtain

$$Z_i = \frac{V_i}{I_i} = h_i - h_r R_L A_i$$

and substituting

$$A_i = \frac{h_f}{1 + h_o R_L}$$

yields

$$\boxed{Z_i = \frac{V_i}{I_i} = h_i - \frac{h_f h_r R_L}{1 + h_o R_L}} \qquad (5.162)$$

The familiar form of $Z_i = h_i$ is obtained if the second factor in the denominator $(h_o R_L)$ is sufficiently smaller than one.

Output Impedance, $Z_o = V_o/I_o$

The output impedance of an amplifier is defined to be the ratio of the output voltage to the output current with the signal V_s set to zero. For the input circuit with $V_s = 0$,

$$I_i = -\frac{h_r V_o}{R_s + h_i}$$

Substituting this relationship into the equation from the output circuit yields

$$I_o = h_f I_i + h_o V_o$$

$$= -\frac{h_f h_r V_o}{R_s + h_i} + h_o V_o$$

and

$$\boxed{Z_o = \frac{V_o}{I_o} = \frac{1}{h_o - [h_f h_r/(h_i + R_s)]}} \qquad (5.163)$$

In this case, the output impedance is reduced to the familiar form $Z_o = 1/h_o$ for the transistor when the second factor in the denominator is sufficiently smaller than the first.

EXAMPLE 5.33 For the network of Fig. 5.124, determine the following parameters using the complete hybrid equivalent model and compare to the results obtained using the approximate model.

a. Z_i and Z_i'.
b. A_v.
c. $A_i = I_o/I_i$.
d. Z_o (within R_C) and Z_o' (including R_C).

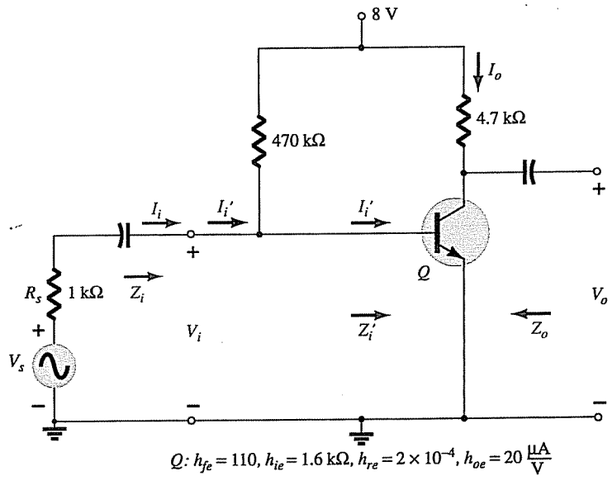


FIG. 5.124
Example 5.33.

Solution: Now that the basic equations for each quantity have been derived, the order in which they are calculated is arbitrary. However, the input impedance is often a useful quantity to know, and therefore will be calculated first. The complete common-emitter hybrid equivalent circuit has been substituted and the network redrawn as shown in Fig. 5.125. A Thévenin equivalent circuit for the input section of Fig. 5.125 results in the input equivalent of Fig. 5.126 since $E_{\text{Th}} \cong V_s$ and $R_{\text{Th}} \cong R_s = 1\ \text{k}\Omega$ (a result of $R_B = 470\ \text{k}\Omega$ being much greater than $R_s = 1\ \text{k}\Omega$). In this example, $R_L = R_C$, and I_o is defined as the current through R_C as in previous examples of this chapter. The output impedance Z_o as defined by Eq. (5.163) is for the output transistor terminals only. It does not include the effects of R_C. Z_o is simply the parallel combination of Z_o and R_L. The resulting configuration of Fig. 5.126

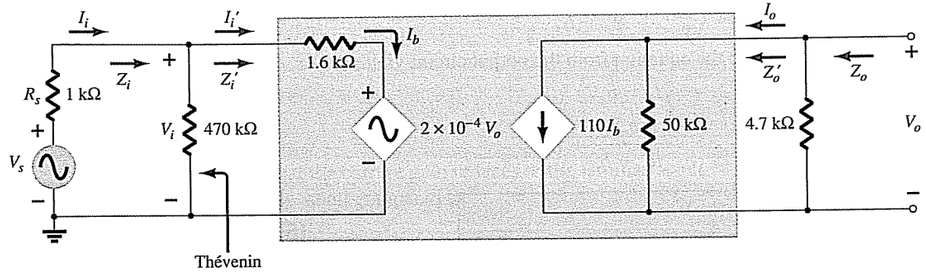


FIG. 5.125
Substituting the complete hybrid equivalent circuit into the ac equivalent network of Fig. 5.124.

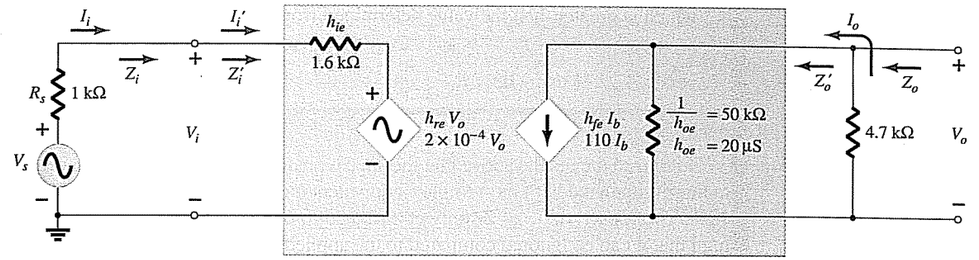


FIG. 5.126
Replacing the input section of Fig. 5.125 with a Thévenin equivalent circuit.

is then an exact duplicate of the defining network of Fig. 5.123, and the equations derived above can be applied.

a. Eq. (5.162):

$$Z_i = \frac{V_i}{I_i} = h_{ie} - \frac{h_{fe}h_{re}R_L}{1 + h_{oe}R_L}$$
$$= 1.6\,\text{k}\Omega - \frac{(110)(2 \times 10^{-4})(4.7\,\text{k}\Omega)}{1 + (20\,\mu\text{S})(4.7\,\text{k}\Omega)}$$
$$= 1.6\,\text{k}\Omega - 94.52\ \Omega$$
$$= \mathbf{1.51\,k\Omega}$$

versus 1.6 kΩ using simply h_{ie}; and

$$Z_i' = 470\,\text{k}\Omega \| Z_i \cong Z_i = \mathbf{1.51\,k\Omega}$$

b. Eq. (5.161):

$$A_v = \frac{V_o}{V_i} = \frac{-h_{fe}R_L}{h_{ie} + (h_{ie}h_{oe} - h_{fe}h_{re})R_L}$$
$$= \frac{-(110)(4.7\,\text{k}\Omega)}{1.6\,\text{k}\Omega + [(1.6\,\text{k}\Omega)(20\mu\text{S}) - (110)(2 \times 10^{-4})]4.7\,\text{k}\Omega}$$
$$= \frac{-517 \times 10^3\ \Omega}{1.6\,\text{k}\Omega + (0.032 - 0.022)4.7\,\text{k}\Omega}$$
$$= \frac{-517 \times 10^3\ \Omega}{1.6\,\text{k}\Omega + 47\ \Omega}$$
$$= \mathbf{-313.9}$$

versus −323.125 using $A_v \cong -h_{fe}R_L/h_{ie}$.

c. Eq. (5.160):

$$A_i' = \frac{I_o}{I_i'} = \frac{h_{fe}}{1 + h_{oe}R_L} = \frac{110}{1 + (20\,\mu\text{S})(4.7\,\text{k}\Omega)}$$
$$= \frac{110}{1 + 0.094} = \mathbf{100.55}$$

versus 110 using simply h_{fe}. Since $470\,\text{k}\Omega \gg Z_i', I_i \cong I_i'$ and $A_i \cong$ **100.55** also.

d. Eq. (5.163):

$$Z_o = \frac{V_o}{I_o} = \frac{1}{h_{oe} - [h_{fe}h_{re}/(h_{ie} + R_s)]}$$
$$= \frac{1}{20\,\mu\text{S} - [(110)(2 \times 10^{-4})/(1.6\,\text{k}\Omega + 1\,\text{k}\Omega)]}$$
$$= \frac{1}{20\,\mu\text{S} - 8.46\,\mu\text{S}}$$
$$= \frac{1}{11.54\,\mu\text{S}}$$
$$= \mathbf{86.66\,k\Omega}$$

which is greater than the value determined from $1/h_{oe}$, 50 kΩ; and

$$Z_o' = R_C \| Z_o = 4.7\,\text{k}\Omega \| 86.66\,\text{k}\Omega = \mathbf{4.46\,k\Omega}$$

versus 4.7 kΩ using only R_C.

Note from the results above that the approximate solutions for A_v and Z_i were very close to those calculated with the complete equivalent model. In fact, even A_i was off by less than 10%. The higher value of Z_o only contributed to our earlier conclusion that Z_o is often so high that it can be ignored compared to the applied load. However, keep in mind that when there is a need to determine the effect of h_{re} and h_{oe}, the complete hybrid equivalent model must be used, as described above.

The specification sheet for a particular transistor typically provides the common-emitter parameters as noted in Fig. 5.18. The next example will employ the same transistor parameters appearing in Fig. 5.124 in a *pnp* common-base configuration to introduce the parameter conversion procedure and emphasize the fact that the hybrid equivalent model maintains the same layout.

EXAMPLE 5.34 For the common-base amplifier of Fig. 5.127, determine the following parameters using the complete hybrid equivalent model and compare the results to those obtained using the approximate model.

a. Z_i
b. A_i
c. A_v.
d. Z_o

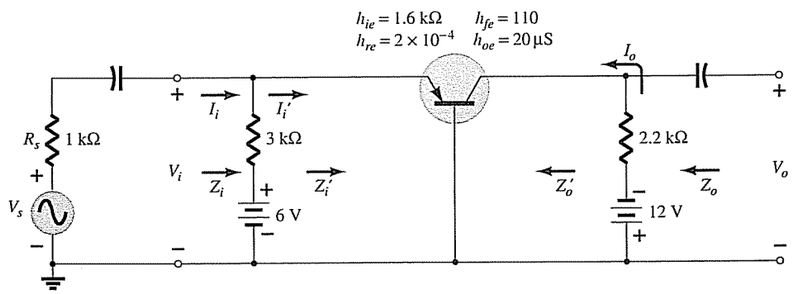


FIG. 5.127
Example 5.34.

Solution: The common-base hybrid parameters are derived from the common-emitter parameters using the approximate equations of Appendix B:

$$h_{ib} \cong \frac{h_{ie}}{1 + h_{fe}} = \frac{1.6\,\text{k}\Omega}{1 + 110} = \mathbf{14.41\ \Omega}$$

Note how closely the magnitude compares with the value determined from

$$h_{ib} = r_e = \frac{h_{ie}}{\beta} = \frac{1.6\,\text{k}\Omega}{110} = 14.55\ \Omega$$

Also,

$$h_{rb} \cong \frac{h_{ie}h_{oe}}{1 + h_{fe}} - h_{re} = \frac{(1.6\,\text{k}\Omega)(20\,\mu\text{S})}{1 + 110} - 2 \times 10^{-4}$$
$$= \mathbf{0.883 \times 10^{-4}}$$

$$h_{fb} \cong \frac{-h_{fe}}{1 + h_{fe}} = \frac{-110}{1 + 110} = \mathbf{-0.991}$$

$$h_{ob} \cong \frac{h_{oe}}{1 + h_{fe}} = \frac{20\,\mu\text{S}}{1 + 110} = \mathbf{0.18\ \mu S}$$

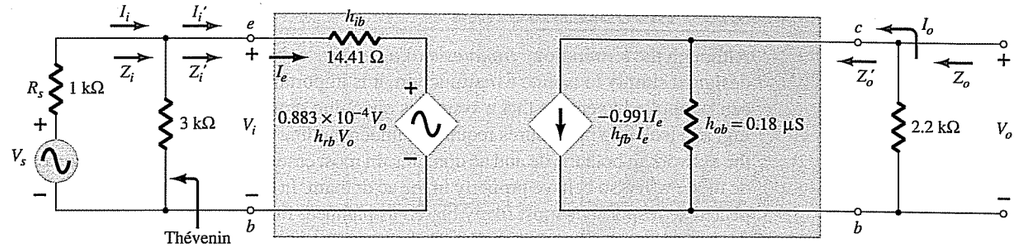


FIG. 5.128
Small-signal equivalent for the network of Fig. 5.127.

Substituting the common-base hybrid equivalent circuit into the network of Fig. 5.127 results in the small-signal equivalent network of Fig. 5.128. The Thévenin network for the input circuit results in $R_{\text{Th}} = 3\,\text{k}\Omega \| 1\,\text{k}\Omega = 0.75\,\text{k}\Omega$ for R_s in the equation for Z_o.

a. Eq. (5.162):

$$Z_i' = \frac{V_i}{I_i'} = h_{ib} - \frac{h_{fb}h_{rb}R_L}{1 + h_{ob}R_L}$$
$$= 14.41\ \Omega - \frac{(-1.991)(0.883 \times 10^{-4})(2.2\,\text{k}\Omega)}{1 + (0.18\,\mu\text{S})(2.2\,\text{k}\Omega)}$$
$$= 14.41\ \Omega + 0.19\ \Omega$$
$$= 14.60\ \Omega$$

versus 14.41 Ω using $Z_i \cong h_{ib}$; and

$$Z_i = 3\,\text{k}\Omega \| Z_i' \cong Z_i' = \mathbf{14.60\ \Omega}$$

b. Eq. (5.160):

$$A_i = \frac{I_o}{I_i'} = \frac{h_{fb}}{1 + h_{ob}R_L}$$
$$= \frac{-0.991}{1 + (0.18\,\mu\text{S})(2.2\,\text{k}\Omega)}$$
$$= -0.991 = h_{fb}$$

Since $3\,\text{k}\Omega \gg Z_i'$, $I_i \cong I_i'$ and $A_i = I_o/I_i \cong \mathbf{-1}$ also.

c. Eq. (5.161):

$$A_v = \frac{V_o}{V_i} = \frac{-h_{fb}R_L}{h_{ib} + (h_{ib}h_{ob} - h_{fb}h_{rb})R_L}$$
$$= \frac{-(-0.991)(2.2\,\text{k}\Omega)}{14.41\ \Omega + [(14.41\Omega)(0.18\,\mu\text{S}) - (-0.991)(0.883 \times 10^{-4})]2.2\,\text{k}\Omega}$$
$$= \mathbf{149.25}$$

versus 151.3 using $A_v \cong -h_{fb}R_L/h_{ib}$.

d. Eq. (5.163):

$$Z_o' = \frac{1}{h_{ob} - [h_{fb}h_{rb}/(h_{ib} + R_s)]}$$
$$= \frac{1}{0.18\,\mu\text{S} - [(-0.991)(0.883 \times 10^{-4})/(14.41\ \Omega + 0.75\,\text{k}\Omega)]}$$
$$= \frac{1}{0.295\,\mu\text{S}}$$
$$= \mathbf{3.39\,M\Omega}$$

versus 5.56 MΩ using $Z_o' \cong 1/h_{ob}$. For Z_o as defined by Fig. 5.138,

$$Z_o = R_C \| Z_o' = 2.2\,\text{k}\Omega \| 3.39\,\text{M}\Omega = \mathbf{2.199\,k\Omega}$$

versus 2.2 kΩ using $Z_o \cong R_C$.

5.26 TROUBLESHOOTING

Although the terminology *troubleshooting* suggests that the procedures to be described are designed simply to isolate a malfunction, it is important to realize that the same techniques can be applied to ensure that a system is operating properly. In any case, the testing, checking, and isolating procedures require an understanding of what to expect at various points in the network in both the dc and ac domains. In most cases, a network operating correctly in the dc mode will also behave properly in the ac domain. In addition, a network providing the expected ac response is most likely biased as planned. In a typical laboratory setting, both the dc and ac supplies are applied and the ac response at various points in the network is checked with an oscilloscope as shown in Fig. 5.129. Note that the black (gnd) lead of the oscilloscope is connected directly to ground and the red lead is moved from point to point in the network, providing the patterns appearing in Fig. 5.129. The vertical channels are set in the ac mode to remove any dc component associated with the voltage at a particular point. The small ac signal applied to the base is amplified to the level appearing from collector to ground. Note the difference in vertical scales for the two voltages. There is no ac response at the emitter terminal due to the short-circuit characteristics of the capacitor at the applied frequency. The fact that v_o is measured in volts and v_i in millivolts suggests a sizable gain for the amplifier. In general, the network appears to be operating properly. If desired, the dc mode of the multimeter could be used to check V_{BE} and the levels of V_B, V_{CE}, and V_E to review whether they lie in the expected range. Of course, the oscilloscope can also be used to compare dc levels simply by switching to the dc mode for each channel.

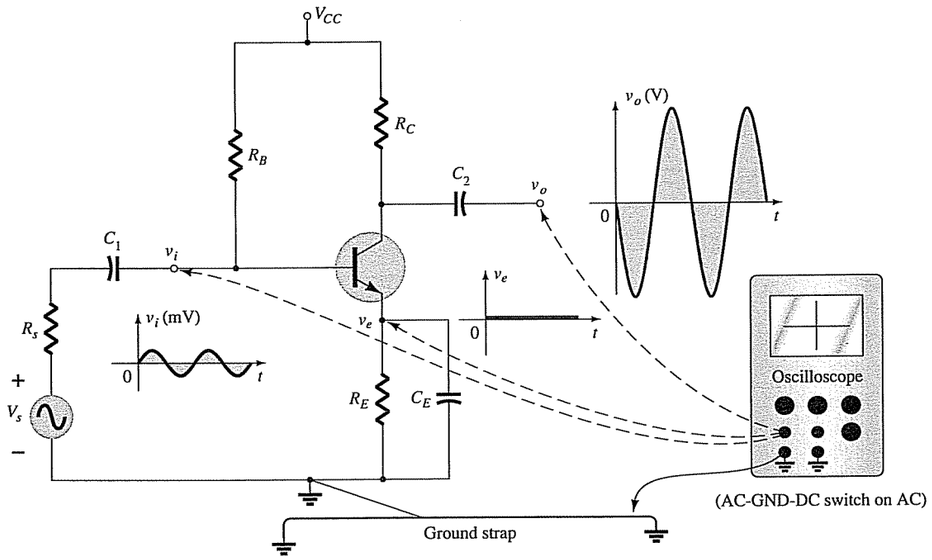


FIG. 5.129
Using the oscilloscope to measure and display various voltages of a BJT amplifier.

A poor ac response can be due to a variety of reasons. In fact, there may be more than one problem area in the same system. Fortunately, however, with time and experience, the probability of malfunctions in some areas can be predicted and an experienced person can isolate problem areas fairly quickly.

In general, there is nothing mysterious about the general troubleshooting process. If you decide to follow the ac response, it it good procedure to start with the applied signal and progress through the system toward the load, checking critical points along the way. An unexpected response at some point suggests that the network is fine up to that area, thereby defining the region that must be investigated further. The wave-form obtained on the oscilloscope will certainly help in defining the possible problems with the system.

If the response for the network of Fig. 5.129 is as appears in Fig. 5.130, the network has a malfunction that is probably in the emitter area. An ac response across the emitter is unexpected,

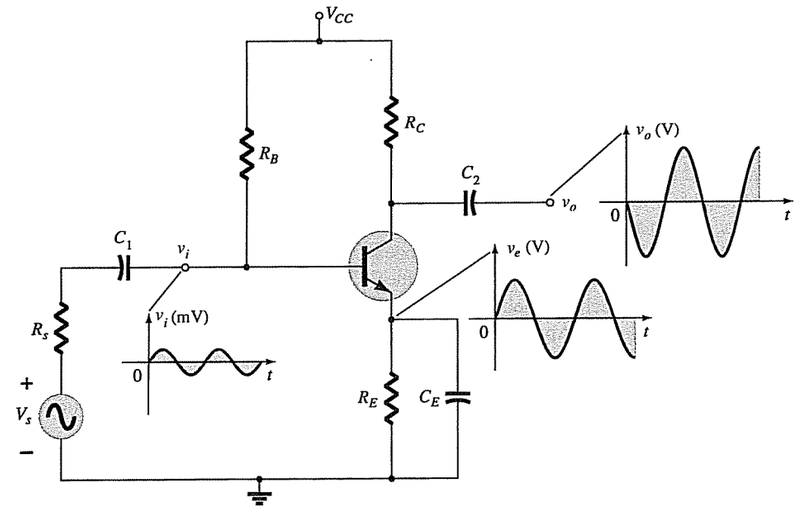


FIG. 5.130
The waveforms resulting from a malfunction in the emitter area.

and the gain of the system as revealed by v_o is much lower. Recall for this configuration that the gain is much greater if R_E is bypassed. The response obtained suggests that R_E is not bypassed by the capacitor, and the terminal connections of the capacitor and the capacitor itself should be checked. In this case, a checking of the dc levels will probably not isolate the problem area since the capacitor has an "open-circuit" equivalent for dc. In general, a prior knowledge of what to expect, a familiarity with the instrumentation, and, most important, experience are all factors that contribute to the development of an effective approach to the art of troubleshooting.

5.27 PRACTICAL APPLICATIONS

Audio Mixer

When two or more signals are to be combined into a single audio output, mixers such as shown in Fig. 5.131 are employed. The potentiometers at the input are the volume controls for each channel, with potentiometer R_3 included to provided additional balance between the two signals. Resistors R_4 and R_5 are there to ensure that one channel does not load down the other, that is, to ensure that one signal does not appear as a load to the other, draw power, and affect the desired balance on the mixed signal.

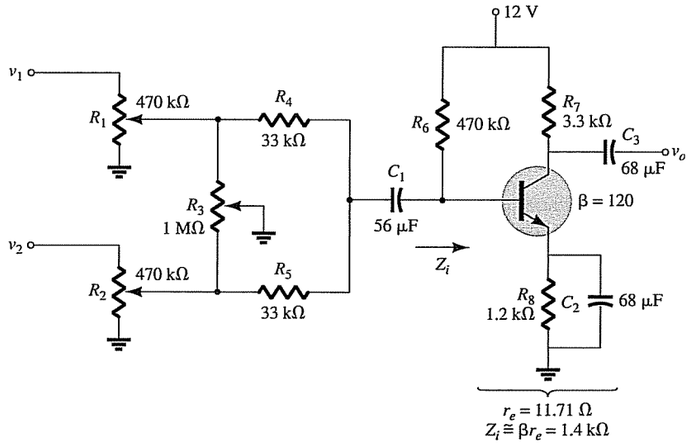


FIG. 5.131
Audio mixer.

The effect of resistors R_4 and R_5 is an important one that should be discussed in some detail. A dc analysis of the transistor configuration results in $r_e = 11.71\ \Omega$, which will establish an input impedance to the transistor of about 1.4 kΩ. The parallel combination of $R_6 \| Z_i$ is also approximately 1.4 kΩ. Setting both volume controls to their maximum value and the balance control R_3 to its midpoint result in the equivalent network of Fig. 5.132a. The signal at v_1 is assumed to be a low-impedance microphone with an internal resistance of 1 kΩ. The signal at v_2 is assumed to be a guitar amplifier with a higher internal impedance of 10 kΩ. Since the 470-kΩ and 500-kΩ resistors are in parallel for the above conditions, they can be combined and replaced with a single resistor of about 242 kΩ. Each source will then have an equivalent such as shown in Fig. 5.132b for the microphone. Applying Thévenin's theorem shows that it is an excellent approximation to simply drop the 242 kΩ and assume that the equivalent network is as shown for each channel. The result is the equivalent network of Fig. 5.132c for the input section of the mixer. Applying the superposition theorem results in the following equation for the ac voltage at the base of the transistor:

$$v_b = \frac{(1.4\,\text{k}\Omega \| 43\,\text{k}\Omega)v_{s_1}}{34\,\text{k}\Omega + (1.4\,\text{k}\Omega \| 43\,\text{k}\Omega)} + \frac{(1.4\,\text{k}\Omega \| 34\,\text{k}\Omega)v_{s_2}}{43\,\text{k}\Omega + (1.4\,\text{k}\Omega \| 34\,\text{k}\Omega)}$$
$$= 38 \times 10^{-3} v_{s_1} + 30 \times 10^{-3} v_{s_2}$$

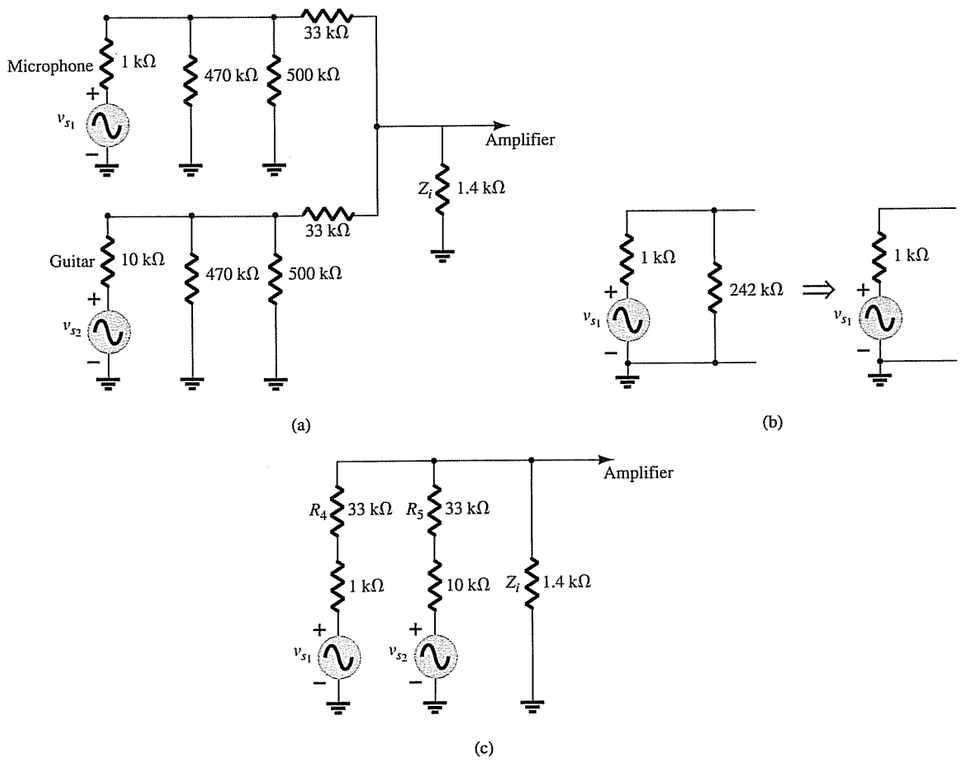


FIG. 5.132

(a) Equivalent network with R_3 set at the midpoint and the volume controls on their maximum settings; (b) finding the Thévenin equivalent for channel 1; (c) substituting the Thévenin equivalent networks into Fig. 5.132a.

With $r_e = 11.71\ \Omega$, the gain of the amplifier is $-R_C/r_e = 3.3\,\text{k}\Omega/11.71\ \Omega = -281.8$, and the output voltage is

$$v_o = -10.7v_{s_1} - 8.45v_{s_2}$$

which provides a pretty good balance between the two signals even though they have a 10:1 ratio in internal impedance. In general, the system will respond quite well. However, if we

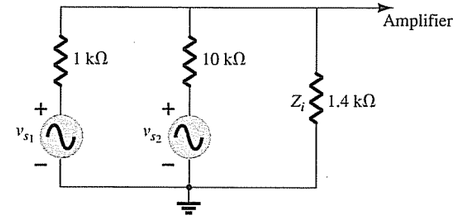


FIG. 5.133

Redrawing the network of Fig. 5.132c with the 33-kΩ resistors removed.

now remove the 33-kΩ resistors from the diagram of Fig. 5.132c, the equivalent network of Fig. 5.133 results and the following equation for v_b is obtained using the superposition theorem:

$$v_b = \frac{(1.4\,\text{k}\Omega \| 10\,\text{k}\Omega)v_{s_1}}{1\,\text{k}\Omega + 1.4\,\text{k}\Omega \| 10\,\text{k}\Omega} + \frac{(1.4\,\text{k}\Omega \| 1\,\text{k}\Omega)v_{s_2}}{10\,\text{k}\Omega + (1.4\,\text{k}\Omega \| 1\,\text{k}\Omega)}$$
$$= 0.55v_{s_1} + 0.055v_{s_2}$$

Using the same gain as before, we obtain the output voltage as

$$v_o = 155v_{s_1} + 15.5v_{s_2} \cong 155v_{s_1}$$

which indicates that the microphone will be quite loud and clear and the guitar input essentially lost.

The importance of the 33-kΩ resistors is therefore defined. It makes each applied signal appear to have a similar impedance level so that there is good balance at the output. One might suggest that the larger resistor improves the balance. However, even though the balance at the base of the transistor may be better, the strength of the signal at the base of the transistor will be less, and the output level reduced accordingly. In other words, the choice of resistors R_4 and R_5 is a give-and-take situation between the input level at the base of the transistor and the balance of the output signal.

To demonstrate that the capacitors are truly short-circuit equivalents in the audio range, substitute a very low audio frequency of 100 Hz into the reactance equation of a 56-μF capacitor:

$$X_C = \frac{1}{2\pi fC} = \frac{1}{2\pi(100\,\text{Hz})(56\,\mu\text{F})} = 28.42\ \Omega$$

A level of 28.42 Ω compared to any of the neighboring impedances is certainly small enough to be ignored. Higher frequencies will have even less effect.

A similar mixer will be discussed in connection with the junction field effect transistor (JFET) in the following chapter. The major difference will be the fact that the input impedance of the JFET can be approximated by an open circuit rather than the rather low-level input impedance of the BJT configuration. The result will be a higher signal level at the input to the JFET amplifier. However, the gain of the FET is much less than that of the BJT transistor, resulting in output levels that are actually quite similar.

Preamplifier

The primary function of a **preamplifier** is as its name implies: **an amplifier used to pick up the signal from its primary source and then operate on it in preparation for its passage into the amplifier section.** Typically, a preamplifier will amplify the signal, control its volume, perhaps change its input impedance characteristics, and if necessary determine its route through the stages to follow—in total, a stage of any system with a multitude of functions.

A preamplifier such as shown in Fig. 5.134 is often used with dynamic microphones to bring the signal level up to levels that are suitable for further amplification or power amplifiers. Typically, dynamic microphones are low-impedance microphones since their internal resistance is determined primarily by the winding of the voice coil. The basic construction consists of a voice coil attached to a small diaphragm that is free to move within a permanent magnet. When one speaks into the microphone, the diaphragm moves accordingly and causes

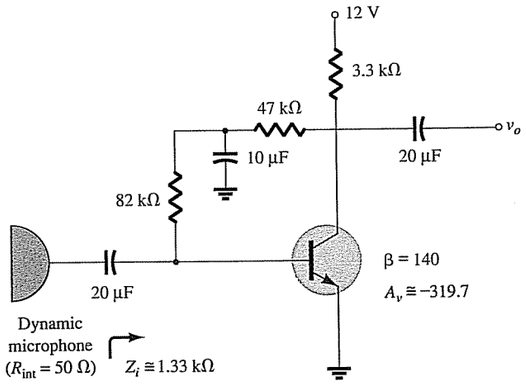


FIG. 5.134
Preamplifier for a dynamic microphone.

the voice coil to move in the same manner within the magnetic field. In accord with Faraday's law, a voltage will be induced across the coil that will carry the audio signal.

Since it is a low-impedance microphone, the input impedance of the transistor amplifier does not have to be that high to pick up most of the signal. Since the internal impedance of a dynamic microphone may be as low as 20 Ω to 100 Ω, most of the signal would be picked up with an amplifier having an input impedance as low as 1 to 2 kΩ. This, in fact, is the case for the preamplifier of Fig. 5.134. For dc biasing conditions, the collector dc feedback configuration was chosen because of its high stablity characteristics.

In the ac domain, the 10-μF capacitor will assume a short-circuit state (on an approximate basis), placing the 82-kΩ resistor across the input impedance of the transistor and the 47 kΩ across the output of the transistor. A dc analysis of the transistor configuration results in $r_e = 9.64\ \Omega$, giving an ac gain determined by

$$A_v = -\frac{(47\ k\Omega \| 3.3\ k\Omega)}{9.64\ \Omega} = \mathbf{-319.7}$$

which is excellent for this application. Of course, the gain will drop when this pickup stage of the design is connected to the input of the amplifier section. That is, the input resistance of the next stage will appear in parallel with the 47-kΩ and 3.3-kΩ resistors and will drop the gain below the unloaded level of 319.7.

The input impedance of the preamplifier is determined by

$$Z_i = 82\ k\Omega \| \beta r_e = 82\ k\Omega \| (140)(9.64\ \Omega) = 82\ k\Omega \| 1.34\ k\Omega = \mathbf{1.33\ k\Omega}$$

which is also fine for most low-impedance dynamic microphones. In fact, for a microphone with an internal impedance of 50 Ω, the signal at the base would be over 98% of that available. This discussion is important because if the impedance of the microphone is a great deal more, say, 1 kΩ, the preamplifier would have to be designed differently to ensure that the input impedance was at least 10 kΩ or more.

Random-Noise Generator

There is often a need for a random-noise generator to test the response of a speaker, microphone, filter, and, in fact, any system designed to work over a wide range of frequencies. A **random-noise generator** is just as its name implies: **a generator that generates signals of random amplitude and frequency.** The fact that these signals are usually totally unintelligible and unpredictable is the reason that they are simply referred to as *noise*. **Thermal noise** is noise generated due to thermal effects resulting from the interaction between free electrons and the vibrating ions of a material in conduction. The result is an uneven flow of electrons through the medium, which will result in a varying potential across the medium. In most cases, these randomly generated signals are in the microvolt range, but with sufficient amplification they can wreak havoc on a system's response. This thermal noise is also called **Johnson noise** (named after the original researcher in the area) or **white noise** (because in optics, white light contains all frequencies). This type of noise has a fairly flat

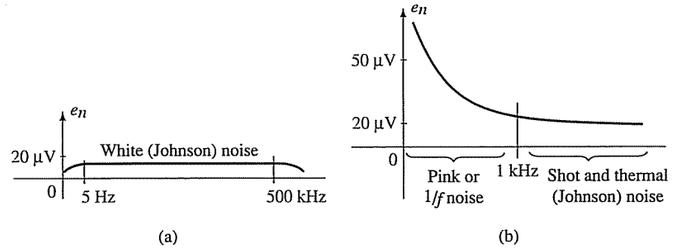


FIG. 5.135
Typical noise frequency spectra: (a) white or Johnson; (b) pink, thermal, and shot.

frequency response such as shown in Fig. 5.135a, that is, a plot of its power versus frequency from the very low to the very high end is fairly uniform. A second type of noise is called **shot noise**, a name derived from the fact that its noise sounds like a shower of lead shot hitting a solid surface or like heavy rain on a window. Its source is pockets of carriers passing through a medium at uneven rates. A third is **pink**, **flicker**, or **1/*f* noise**, which is due to the variation in transit times for carriers crossing various junctions of semiconductor devices. It is called 1/*f* noise because its magnitude drops off with increase in frequency. **Its effect is usually the most dramatic for frequencies below 1 kHz**, as shown in Fig. 5.135b.

The network of Fig. 5.136 is designed to generate both a white noise and a pink noise. Rather than a separate source for each, first white noise is developed (level across the entire frequency spectrum), and then a filter is applied to remove the mid- and high-frequency components, leaving only the low-frequency noise response. The filter is further designed to modify the flat response of the white noise in the low-frequency region (to create a 1/*f* drop-off) by having sections of the filter "drop in" as the frequency increases. The white noise is created by leaving the collector terminal of transistor Q_1 open and reverse-biasing the base-to-emitter junction. In essence, the transistor is being used as a diode biased in the Zener avalanche region. Biasing a transistor in this region creates a very unstable situation that is conductive to the generation of random white noise. The combination of the avalanche region with its rapidly changing charge levels, sensitivity of the current level to temperature, and quickly changing impedance levels contributes to the level of noise voltage and current generated by the transistor. Germanium transistors are often used because the avalanche region is less defined and less stable than in silicon transistors. In addition, there are diodes and transistors designed specifically for random-noise generation.

The source of the noise is not some specially designed generator. It is simply due to the fact that current flow is not an ideal phenomenon but actually varies with time at a level that

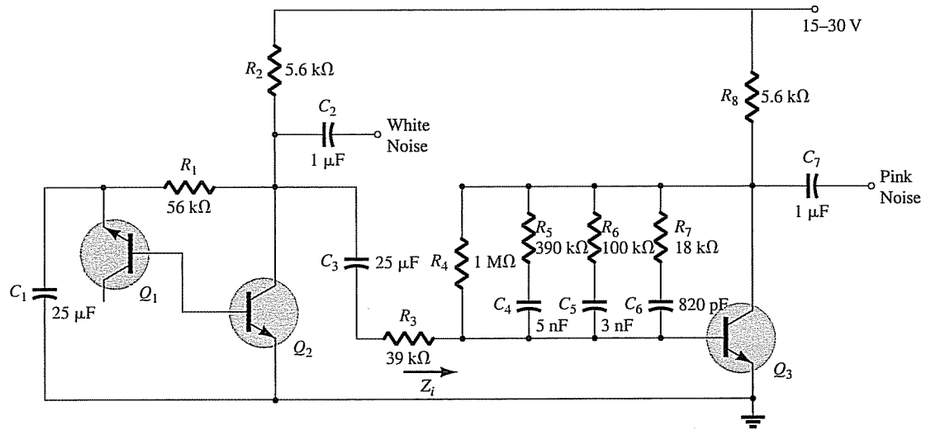


FIG. 5.136
White- and pink-noise generator.

generates unwanted variations in the terminal voltage across elements. In fact, that variation in flow is so broad that it can generate frequencies that extend across a wide spectrum—a very interesting phenomenon.

The generated noise current of Q_1 will then be the base current for Q_2, which will be amplified to generate a white noise of perhaps 100 mV, which for this design would suggest an input noise voltage of about 170 μV. Capacitor C_1 will have a low impedance throughout the frequency range of interest to provide a "shorting effect" on any spurious signals in the air from contributing to the signal at the base of Q_1. The capacitor C_2 is there to isolate the dc biasing of the white-noise generator from the dc levels of the filter network to follow. The 39 kΩ and the input impedance of the next stage create the simple voltage-divider network of Fig. 5.137. If the 39 kΩ were not present, the parallel combination of R_2 and Z_i would load down the first stage and reduce the gain of Q_1 considerably. In the gain equation, R_2 and Z_i would appear in parallel (discussed in Chapter 9).

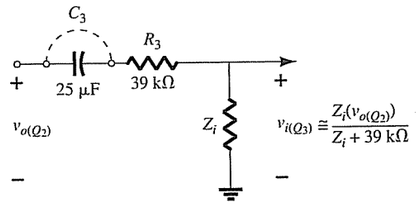


FIG. 5.137
Input circuit for the second stage.

The filter network is actually part of the feedback loop from collector to base appearing in the collector feedback network of Section 5.13. To describe its behavior, let us first consider the extremes of the frequency spectrum. For very low frequencies all the capacitors can be approximated by an open circuit, and the only resistance from collector to base is the 1-MΩ resistor. Using a beta of 100, we find that the gain of the section is about 280 and the input impedance about 1.28 kΩ. At a sufficiently high frequency all the capacitors could be replaced by short circuits, and the total resistance combination between collector and base would be reduced to about 14.5 kΩ, which would result in a very high unloaded gain of about 731, more than twice that just obtained with $R_F = 1$ MΩ. Since the $1/f$ filter is supposed to reduce the gain at high frequencies, it initially appears as though there is an error in design. However, the input impedance has dropped to about 19.33 Ω, which is a 66-fold drop from the level obtained with $R_F = 1$ MΩ. This would have a significant impact on the input voltage appearing at the second stage when we consider the voltage-divider action of Fig. 5.137. In fact, when compared to the series 39-kΩ resistor, the signal at the second stage can be assumed to be negligible or at a level where even a gain in excess of 700 cannot raise it to a level of any consequence. In total, therefore, the effect of doubling the gain is totally lost due to the tremendous drop in Z_i, and the output at very high frequencies can be ignored entirely.

For the range of frequencies between the very low and the very high, the three capacitors of the filter will cause the gain to drop off with increase in frequency. First, capacitor C_4 will be dropped in and cause a reduction in gain (around 100 Hz). Then capacitor C_5 will be included and will place the three branches in parallel (around 500 Hz). Finally, capacitor C_6 will result in four parallel branches and the minimum feedback resistance (around 6 kHz).

The result is a network with an excellent random-noise signal for the full frequency spectrum (white) and the low-frequency spectrum (pink).

Sound-Modulated Light Source

The light from the 12-V bulb of Fig. 5.138 will vary at a frequency and an intensity that are sensitive to the applied signal. The applied signal may be the output of an acoustical amplifier, a musical instrument, or even a microphone. Of particular interest is the fact that the applied voltage is 12 V ac rather than the typical dc biasing supply. The immediate question, in the absence of a dc supply, is how the dc biasing levels for the transistor will be

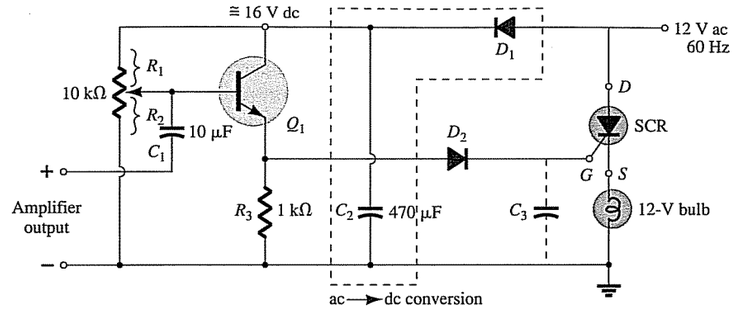


FIG. 5.138
Sound-modulated light source. SCR, Silicon-controlled rectifier.

established. In actuality, the dc level is obtained through the use of diode D_1, which rectifies the ac signal, and capacitor C_2, which acts as a power supply filter to generate a dc level across the output branch of the transistor. The peak value of a 12-V rms supply is about 17 V, resulting in a dc level after the capacitive filtering in the neighborhood of 16 V. If the potentiometer is set so that R_1 is about 320 Ω, the voltage from base to emitter of the transistor will be about 0.5 V, and the transistor will be in the "off" state. In this state the collector and emitter currents are essentially 0 mA, and the voltage across resistor R_3 is approximately 0 V. The voltage at the junction of the collector terminal and the diode is therefore 0 V, resulting in D_2 being in the "off" state and 0 V at the gate terminal of the silicon-controlled rectifier (SCR). The SCR (see Section 17.3) is fundamentally a diode whose state is controlled by an applied voltage at the gate terminal. The absence of a voltage at the gate means that the SCR and bulb are off.

If a signal is now applied to the gate terminal, the combination of the established biasing level and the applied signal can establish the required 0.7-V turn-on voltage, and the transistor will be turned on for periods of time dependent on the applied signal. When the transistor turns on, it will establish a collector current through resistor R_3 that will establish a voltage from collector to ground. If the voltage is more than the required 0.7 V for diode D_2, a voltage will appear at the gate of the SCR that may be sufficient to turn it on and establish conduction from the drain to the source of the SCR. However, we must now examine one of the most interesting aspects of this design. Since the applied voltage across the SCR is ac, which will vary in magnitude with time as shown in Fig. 5.139, the conduction strength of the SCR will vary with time also. As shown in the figure, if the SCR is turned on when the sinusoidal voltage is a maximum, the resulting current through the SCR will be a maximum also, and the bulb will be its brightest. If the SCR should turn on when the sinusoidal voltage is near its minimum, the bulb may turn on, but the lower current will result in considerably less illumination. The result is that the light bulb turns on in sync with when the input signal is peaking, but the strength of turn-on will be determined by where one is on the applied 12-V signal. One can imagine the interesting and varied responses of such a system. Each time one applies the same audio signal, the response will have a different character.

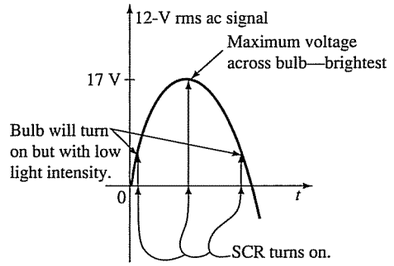


FIG. 5.139
Demonstrating the effect of an ac voltage on the operation of the SCR of Fig. 5.138.

In the above action, the potentiometer was set below the turn-on voltage of the transistor. The potentiometer can also be adjusted so that the transistor is "just on," resulting in a low-level base current. The result is a low-level collector current and insufficient voltage to forward-bias diode D_2 and turn on the SCR at the gate. However, the system is set up in this manner, the resultant light output will be more sensitive to lower amplitude components of the applied signal. In the first case, the system acts more like a peak detector, whereas in the latter case it is sensitive to more components of the signal.

Diode D_2 was included to be sure that there is sufficient voltage to turn on both the diode and the SCR, in other words, to eliminate the possibility of noise or some other low-level unexpected voltage on the line turning the SCR on. Capacitor C_3 can be inserted to slow down the response by ensuring the voltage charge across the capacitor before the gate will reach sufficient voltage to turn on the SCR.

5.28 SUMMARY

Important Conclusions and Concepts

1. Amplification in the ac domain cannot be obtained **without the application of dc biasing level**.
2. For most applications the BJT amplifier can be considered linear, permitting the use of the **superposition theorem** to separate the dc and ac analyses and designs.
3. When introducing the **ac model** for a BJT:
   a. All **dc sources are set to zero** and replaced by a short-circuit connection to ground.
   b. All **capacitors** are replaced by a **short-circuit equivalent**.
   c. All elements **in parallel with** an introduced short-circuit equivalent should be removed from the network.
   d. The network should be **redrawn** as often as possible.
4. The **input impedance** of an ac network **cannot be measured** with an ohmmeter.
5. The **output impedance** of an amplifier is measured with the **applied signal set to zero**. It cannot be measured with an ohmmeter.
6. The **output impedance** for the r_e model **can be included** only if obtained from a data sheet or from a graphical measurement from the characteristic curves.
7. Elements that were isolated by capacitors for the dc analysis **will appear in the ac analysis** due to the short-circuit equivalent for the capacitive elements.
8. The **amplification factor** (beta, β, or h_{fe}) is the least sensitive to changes **in collector current**, whereas the **output impedance** parameter is the most sensitive. The output impedance is also quite sensitive to changes in V_{CE}, whereas the **amplification** factor is the **least sensitive**. However, the **output impedance** is the **least sensitive** to changes in **temperature**, whereas the amplification factor is somewhat sensitive.
9. The r_e **model** for a BJT in the ac domain is sensitive to the **actual dc operating conditions of the network**. This parameter is normally not provided on a specification sheet, although h_{ie} of the normally provided hybrid parameters is equal to βr_e, but only under specific operating conditions.
10. Most **specification sheets** for BJTs include a **list of hybrid parameters** to establish an ac model for the transistor. One must be aware, however, that they are provided for a particular set of dc operating conditions.
11. The **CE fixed-bias configuration** can have a **significant voltage gain** characteristic, although its **input impedance can be relatively low**. The approximate **current gain** is given by simply **beta**, and the **output impedance** is normally assumed to be R_C.
12. The **voltage-divider bias configuration** has a **higher stability** than the fixed-bias configuration, but it has about the **same voltage gain, current gain, and output impedance**. Due to the biasing resistors, its input impedance may be lower than that of the fixed-bias configuration.
13. The **CE emitter-bias configuration** with an unbypassed emitter resistor has a **larger input resistance** than the bypassed configuration, but it will have a **much smaller voltage gain** than the bypassed configuration. For the unbypassed or bypassed situation, the **output impedance** is normally assumed to be simply R_C.
14. The **emitter-follower configuration** will always have an **output voltage slightly less than the input signal**. However, the **input impedance** can be **very large**, making it very useful for situations where a high-input first stage is needed to "pick up" as much of the applied signal as possible. Its **output impedance** is **extremely low**, making it an excellent signal source for the second stage of a multistage amplifier.
15. The **common-base configuration** has a **very low input impedance**, but it can have a **significant voltage gain**. The **current gain** is just **less than 1**, and the **output impedance** is simply R_C.
16. The **collector feedback configuration** has an **input impedance** that is **sensitive to beta** and that can be quite low depending on the parameters of the configuration. However, the **voltage gain** can be **significant** and the **current gain** of **some magnitude** if the parameters are chosen properly. The **output impedance** is most often simply the collector resistance R_C.
17. The **collector dc feedback configuration** uses the dc feedback to **increase its stability** and the changing state of a capacitor from dc to ac to establish a **higher voltage gain** than obtained with a straight feedback connection. The **output impedance** is usually close to R_C and the **input impedance** relatively close to that obtained with the **basic common-emitter configuration**.
18. The **approximate hybrid equivalent network** is very **similar** in composition to that used with the r_e **model**. In fact, the **same methods** of analysis can be applied to both models. For the hybrid model the results will be in terms of the network parameters and the hybrid parameters, whereas for the r_e model they will be in terms of the network parameters and β, r_e, and r_o.
19. The **hybrid model** for common-emitter, common-base, and common-collector configurations **is the same**. The only difference will be the magnitude of the parameters of the equivalent network.
20. The total gain of a cascaded system is determined by the **product of the gains of each stage**. The gain of each stage, however, must be determined **under loaded conditions**.
21. Since the total gain is the product of the individual gains of a cascaded system, the **weakest link** can have a major effect on the total gain.

Equations

$$r_e = \frac{26\text{ mV}}{I_E}$$

Hybrid parameters:

$$h_{ie} = \beta r_e, \qquad h_{fe} = \beta_{ac}, \qquad h_{ib} = r_e, \qquad h_{fb} = -\alpha \cong -1$$

CE fixed bias:

$$Z_i \cong \beta r_e, \qquad Z_o \cong R_C$$

$$A_v = -\frac{R_C}{r_e}, \qquad A_i = -A_v\frac{Z_i}{R_C} \cong \beta$$

Voltage-divider bias:

$$Z_i = R_1 \| R_2 \| \beta r_e, \qquad Z_o \cong R_C$$

$$A_v = -\frac{R_C}{r_e}, \qquad A_i = -A_v\frac{Z_i}{R_C} \cong \beta$$

CE emitter-bias:

$$Z_i \cong R_B \| \beta R_E, \qquad Z_o \cong R_C$$

$$A_v \cong -\frac{R_C}{R_E}, \qquad A_i \cong \frac{\beta R_B}{R_B + \beta R_E}$$

Emitter-follower:

$$Z_i \cong R_B \| \beta R_E, \qquad Z_o \cong r_e$$

$$A_v \cong 1, \qquad A_i = -A_v\frac{Z_i}{R_E}$$

Common-base:

$$Z_i \cong R_E \| r_e, \qquad Z_o \cong R_C$$

$$A_v \cong \frac{R_C}{r_e}, \qquad A_i \cong -1$$

Collector feedback:

$$Z_i \cong \frac{r_e}{\frac{1}{\beta} + \frac{R_C}{R_F}}, \qquad Z_o \cong R_C \| R_F$$

$$A_v = -\frac{R_C}{r_e}, \qquad A_i \cong \frac{R_F}{R_C}$$

Collector dc feedback:

$$Z_i \cong R_{F_1} \| \beta r_e, \qquad Z_o \cong R_C \| R_{F_2}$$

$$A_v = -\frac{R_{F_2} \| R_C}{r_e}, \qquad A_i = -A_v \frac{Z_i}{R_C}$$

Effect of load impedance:

$$A_v = \frac{V_o}{V_i} = \frac{R_L}{R_L + R_o} A_{v_{NL}}, \qquad A_i = \frac{I_o}{I_i} = -A_v \frac{Z_i}{R_L}$$

Effect of source impedance:

$$V_i = \frac{R_i V_s}{R_i + R_s}, \qquad A_{v_s} = \frac{V_o}{V_s} = \frac{R_i}{R_i + R_s} A_{v_{NL}}$$

$$I_s = \frac{V_s}{R_s + R_i}$$

Combined effect of load and source impedance:

$$A_v = \frac{V_o}{V_i} = \frac{R_L}{R_L + R_o} A_{v_{NL}}, \qquad A_{v_s} = \frac{V_o}{V_s} = \frac{R_i}{R_i + R_s} \cdot \frac{R_L}{R_L + R_o} A_{v_{NL}}$$

$$A_i = \frac{I_o}{I_i} = -A_v \frac{R_i}{R_L}, \qquad A_{i_s} = \frac{I_o}{I_s} = -A_{v_s} \frac{R_s + R_i}{R_L}$$

Cascode connection:

$$A_v = A_{v_1} A_{v_2}$$

Darlington connection:

$$\beta_D = \beta_1 \beta_2, \qquad \beta_D = \beta^2$$

$$Z_i = R_B \| (r_i + \beta_D R_E), \qquad A_i = \beta_D \frac{R_B}{(R_B + \beta_D R_E)}$$

$$Z_o = R_E \| r_i \| \frac{r_i}{\beta_D} \approx \frac{r_i}{\beta_D}, \qquad A_v = \frac{V_o}{V_i} = \frac{R_E + \beta_D R_E}{r_i + (R_E + \beta_D R_E)} \approx 1$$

Feedback pair:

$$Z_i = R_B \| (r_i + \beta_1 \beta_2 R_C), \qquad A_i = \beta_1 \beta_2 \frac{R_B}{R_B + Z_i}$$

$$Z_o \approx \frac{r_{i_1}}{\beta_1 \beta_2}, \qquad A_v = \frac{\beta_1 \beta_2 R_C}{(\beta_1 \beta_2 R_C + r_{i_1})}$$

5.29 COMPUTER ANALYSIS

PSpice Windows

BJT Voltage-Divider Configuration The last few chapters have been limited to the dc analysis of electronic networks using PSpice and Multisim. This section will consider the application of an ac source to a BJT network and describe how the results are obtained and interpreted.

Most of the construction of the network of Fig. 5.140 can be accomplished using the procedures introduced in earlier chapters. The ac source can be found in the **SOURCE** library as **VSIN**. You can scroll down the list of options or simply type in **VSIN** at the head of the listing. Once this is selected and placed, a number of labels will appear that define the parameters of the source. Double-clicking the source symbol or using the sequence **Edit-Properties** will result in the **Property Editor** dialog box, which lists all the parameters appearing on the screen and more. By scrolling all the way to the right, you will find a listing for **VAMPL**. Select the blank rectangle under the heading and enter the **1 mV** value. **It is**

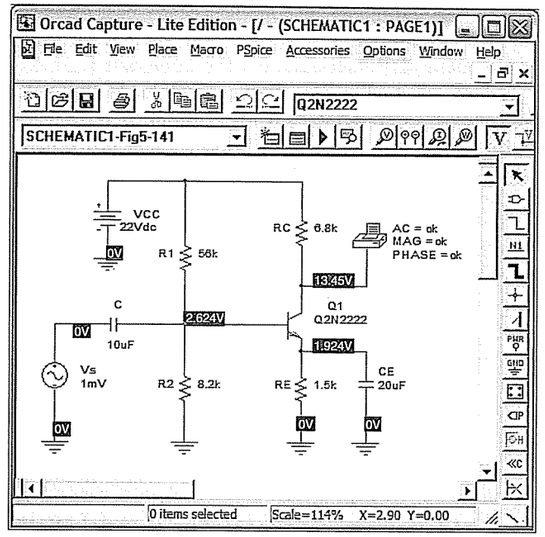


FIG. 5.140
Using PSpice Windows to analyze the network of Fig. 5.42 (Example 5.5).

important to realize that VAMPL defines the peak value of the waveform and not the rms value. In addition, be aware that the entries can use prefixes such as m (milli) and k (kilo). If you scroll to the far left, the heading **FREQ** will appear, in which you can enter **10 kHz**. Moving again to **PHASE**, you will find the default value is **0**, so it can be left alone. It represents the initial phase angle for the sinusoidal signal. At the far right you will find **VOFF**, the dc offset voltage for the sinusoidal signal, which is set at **0 V**. Finally, scroll all the way to the left to set **AC** at **1 mV** also. Now that each of the properties has been set we have to decide what to display on the screen to define the source. In Fig. 5.140 the only labels are Vs and 1 mV, so a number of items have to be deleted and the name of the source has to be modified. For each quantity simply return to the heading and select it for modification. If you choose **AC**, select **Display** to obtain the **Display Properties** dialog box. Select **Value Only** since we prefer not to have the label **AC** appear. Leave all the other choices blank. An **OK**, and you can move to the other parameters within the **Property Editor** dialog box. We do not want the **FREQ**, **VOFF**, **PHASE**, and **VAMPL** labels to appear with their values, so in each case select **Do Not Display**. To change **V1** to **Vs**, simply go to the **Part Reference**, and after selecting it, type in **Vs**. Then go to **Display** and select **Value Only**. Finally, to apply all the changes, select **Apply** and exit the dialog box; the source will appear as shown in Fig. 5.140.

The ac response for the voltage at a point in the network is obtained using the **VPRINT1** option found in the **SPECIAL** library. If the library does not appear, simply select **Add Library** followed by **special.olb**. When **VPRINT1** is chosen, it will appear on the screen as a printer with three labels: **AC**, **MAG**, and **PHASE**. Each has to be set to an OK status to reflect the fact that you desire this type of information about the voltage level. This is accomplished by simply clicking on the printer symbol to obtain the dialog box and setting each to **OK**. For each entry select **Display** and choose **Name and Label**. Finally, select **Apply** and exit the dialog box. The result appears in Fig. 5.140.

The transistor **Q2N2222** can be found under the **EVAL** library by typing it under the **Part** heading or simply scrolling through the possibilities. The levels of I_s and β can be set by applying the sequence **Edit-PSpice Model** to obtain the **PSpice Model Editor Lite** dialog box and changing **Is** to **2E-15A** and **Bf** to 90. The level of **Is** is the result of numerous runs of the network to find the value that would result in V_{BE} being closest to 0.7 V.

Now that all the components of the network have been set, it is time to ask the computer to analyze the network and provide some results. If improper entries were made, the computer will quickly respond with an error listing. First select the **New Simulation Profile** key to obtain the **New Simulation** dialog box. Then, after entering **Name** as **Fig. 5-141**, select

Create and the **Simulation Settings** dialog box will appear. Under **Analysis type**, select **AC Sweep/Noise** and then under **AC Sweep Type** choose **Linear**. The **Start Frequency** is **10 kHz**, the **End Frequency** is **10 kHz**, and the **Total Points** is **1**. An **OK**, and the simulation can be initiated by selecting the **Run PSpice** key (blue arrow). A schematic will result with a graph that extends from 5 kHz to 15 kHz with no vertical scale. Through the sequence **View-Output File** the listing of Fig. 5.141 can be obtained. It starts with a list of all

```
****     CIRCUIT DESCRIPTION
******************************************************************************

**** INCLUDING fig5-140-SCHEMATIC1.net ****
* source FIG5-140
C_C          N03236 N12252  10uF
Q_Q2         N07639 N12252 N02052 Q2N2222
V_VCC         N11445 0 22Vdc
.PRINT          AC
+ VM([N07639])
+ VP([N07639])
R_R2          0 N12252  8.2k
R_RC          N07639 N11445  6.8k
C_CE          0 N02052  20uF
R_RE          0 N02052  1.5k
R_R1          N12252 N11445  56k
V_Vs          N03236 0  AC 1mV
+SIN 0 1mV 10kHz 0 0 0
.END

****     BJT MODEL PARAMETERS
******************************************************************************

               Q2N2222
               NPN
          IS    2.000000E-15
          BF    90
          NF    1
          VAF   74.03
          IKF     .2847
          ISE   14.340000E-15
          NE    1.307
          BR    6.092
          NR    1
          RB    10
          RC    1
          CJE   22.010000E-12
          MJE     .377
          CJC   7.306000E-12
          MJC     .3416
          TF    411.100000E-12
          XTF   3
          VTF   1.7
          ITF     .6
          TR    46.910000E-09
          XTB   1.5
          CN    2.42
          D     .87

****     SMALL SIGNAL BIAS SOLUTION       TEMPERATURE =   27.000 DEG C
******************************************************************************

 NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

(N02052)    1.9244 (N03236)    0.0000 (N07639)   13.4530 (N11445)   22.0000

(N12252)    2.6239


    VOLTAGE SOURCE CURRENTS
    NAME         CURRENT

    V_VCC       -1.603E-03
    V_Vs         0.000E+00

    TOTAL POWER DISSIPATION   3.53E-02  WATTS


****     OPERATING POINT INFORMATION      TEMPERATURE =   27.000 DEG C
******************************************************************************

**** BIPOLAR JUNCTION TRANSISTORS

NAME          Q_Q2
MODEL         Q2N2222
IB            2.60E-05
IC            1.26E-03
VBE           6.99E-01
VBC          -1.08E+01
VCE           1.15E+01
BETADC        4.83E+01
GM            4.84E-02
RPI           1.14E+03
RX            1.00E+01
RO            6.75E+04
CBE           5.78E-11
CBC           2.87E-12
CJS           0.00E+00
BETAAC        5.50E+01
CBX/CBX2      0.00E+00
FT/FT2        1.27E+08

****     AC ANALYSIS                      TEMPERATURE =   27.000 DEG C
******************************************************************************

  FREQ         VM(N07639)   VP(N07639)
  1.000E+04    2.961E-01   -1.780E+02
```

FIG. 5.141
Output file for the network of Fig. 5.140.

the elements of the network and their settings followed by all the parameters of the transistor. In particular, note the level of **IS** and **BF**. Next the dc levels are provided under the **SMALL SIGNAL BIAS SOLUTION**, which match those appearing on the schematic of Fig. 5.140. The dc levels appear on Fig. 5.140 due to the selection of the **V** option. Also note that $V_{BE} = 2.624\,\text{V} - 1.924\,\text{V} = 0.7\,\text{V}$, as stated above, due to the choice of **Is**.

The next listing, **OPERATING POINT INFORMATION**, reveals that even though beta of the **BJT MODEL PARAMETERS** listing was set at 90, the operating conditions of the network resulted in a dc beta of 48.3 and an ac beta of 55. Fortunately, however, the voltage-divider configuration is less sensitive to changes in beta in the dc mode, and the dc results are excellent. However, the drop in ac beta had an effect on the resulting level of V_o: 296.1 mV versus the handwritten solution (with $r_o = 50\,\text{k}\Omega$) of 324.3 mV—a 9% difference. The results are certainly close, but probably not as close as one would like. A closer result (within 7%) could be obtained by setting all the parameters of the device except I_s and beta to zero. However, for the moment, the impact of the remaining parameters has been demonstrated, and the results will be accepted as sufficiently close to the handwritten levels. Later in this chapter, an ac model for the transistor will be introduced with results that will be an exact match with the handwritten solution. The phase angle is $-178°$ versus the ideal of $-180°$, a very close match.

A plot of the voltage at the collector of the transistor can be obtained by setting up a new simulation process to calculate the value of the desired voltage at a number of data points. The more points, the more accurate is the plot. The process is initiated by returning to the **Simulation Settings** dialog box and under **Analysis type** selecting **Time Domain(Transient)**. Time domain is chosen because the horizontal axis will be a time axis, requiring that the collector voltage be determined at a specified time interval to permit the plot. Since the period of the waveform is $1/10\,\text{kHz} = 0.1\,\text{ms} = 100\,\mu\text{s}$ and it would be convenient to display five cycles of the waveform, the **Run to time(TSTOP)** is set at 500 μs. The **Start saving data after** point is left at 0 s and under **Transient option**, the **Maximum step size** is set at 1 μs to ensure 100 data point for each cycle of the waveform. An **OK**, and a **SCHEMATIC** window will appear with a horizontal axis broken down in units of time but with no vertical axis defined. The desired waveform can then be added by first selecting **Trace** followed by **Add Trace** to obtain the **Add Trace** dialog box. In the provided listing **V(Q1:c)** is selected as the voltage at the collector of the transistor. The instant it is selected it will appear as the **Trace Expression** at the bottom of the dialog box. Referring to Fig. 5.140, we find that since the capacitor C_E will essentially be in the short-circuit state at 10 kHz, the voltage from collector to ground is the same as that across the output terminals of the transistor. An **OK**, and the simulation can be initiated by selecting the **Run PSpice** key.

The result will be the waveform of Fig. 5.142 having an average value of about 13.45 V, which corresponds exactly with the bias level of the collector voltage in Fig. 5.140. The range of the vertical axis was chosen automatically by the computer. Five full cycles of the out put voltage are displayed with 100 data points for each cycle. The data points appear in Fig. 5.140 because the sequence **Tools-Options-Mark Data Points** was applied. The data points appear as small dark circles on the plot curve. Using the scale of the graph, we see that the peak-to-peak value of the curve is approximately $13.76\,\text{V} - 13.16\,\text{V} = 0.6\,\text{V} = 600\,\text{mV}$, resulting in a peak value of 300 mV. Since a 1-mV signal was applied, the gain is 300, or very close to the calculator solution of 296.1.

If a comparison is to be made between the input and output voltages on the same screen, the **Add Y-Axis** option under **Plot** can be used. After you select it, choose the **Add Trace** icon and select **V(Vs: +)** from the provided list. The result is that both waveforms will appear on the same screen, each with its own vertical scale. Labels can be added to the waveforms as shown in Fig. 5.143 using **Tools-Label-Text**. A **Text Label** dialog box will appear, in which the desired text can be entered. Click **OK**, and it can be placed using the mouse at any point on the screen. The lines at the dc levels are added using the sequence **Plot-Label-Line**. A pencil will appear, which can be used to draw the line with a left-click at the starting point and another click when the line is in place.

If two separate graphs are preferred, we can start by selecting **Plot** followed by **Add Plot to Window** after the graph of Fig. 5.142 is in place. The result will be a second set of axes waiting for a decision about which curve to plot. Using **Trace-Add Trace-V(Vs: +)** will result in the graphs of Fig. 5.144. The labels were all added using the **Tools** option. The **SEL >>** (from **SELECT**) appearing next to one of the plots defines the "active" plot.

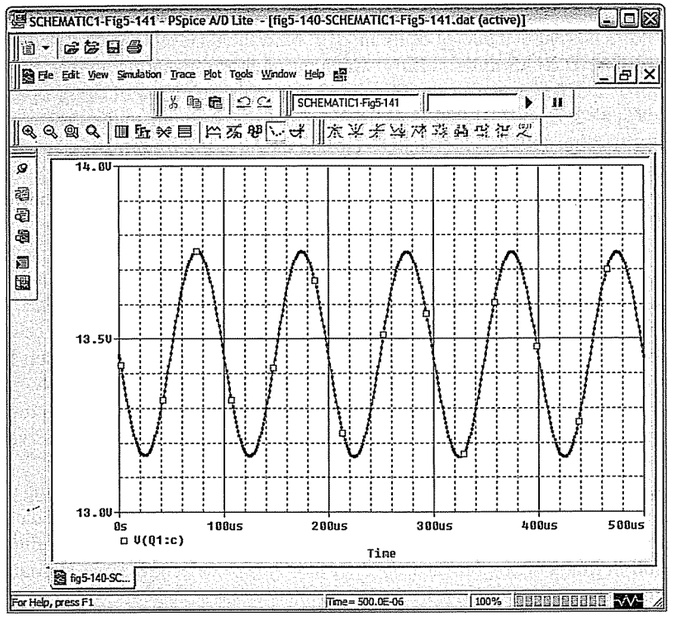


FIG. 5.142

Voltage v_C for the network of Fig. 5.140.

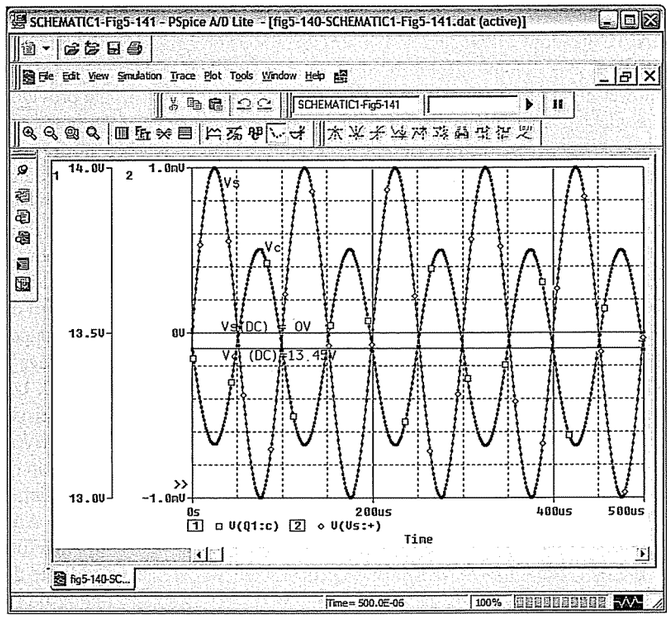


FIG. 5.143

The voltages v_C and v_s for the network of Fig. 5.140.

The last operation to be introduced in this coverage of graph displays is the use of the cursor option. The result of the sequence **Trace-Cursor-Display** is a line at the dc level of the graph of Fig. 5.142 intersecting with a vertical line. The level and time both appear in the small dialog box in the bottom right corner of the screen. The first number for **A1** is the time intersection and the second is the voltage level at that instant. A left-click of the mouse

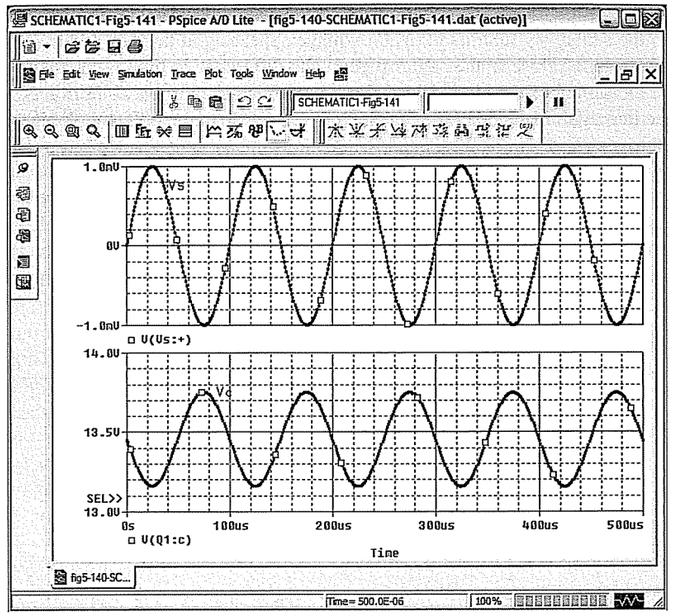


FIG. 5.144

Two separate plots of v_C and v_s in Fig. 5.140.

will provide control of the intersecting vertical and horizontal lines at this level. Clicking on the vertical line and holding down on the clicker will allow you to move the intersection horizontally along the curve, simultaneously displaying the time and voltage level in the data box at the bottom right of the screen. If it is moved to the first peak of the waveform, the time appears as 73.913 μs with a voltage level of 13.754 V as shown in Fig. 5.145. On

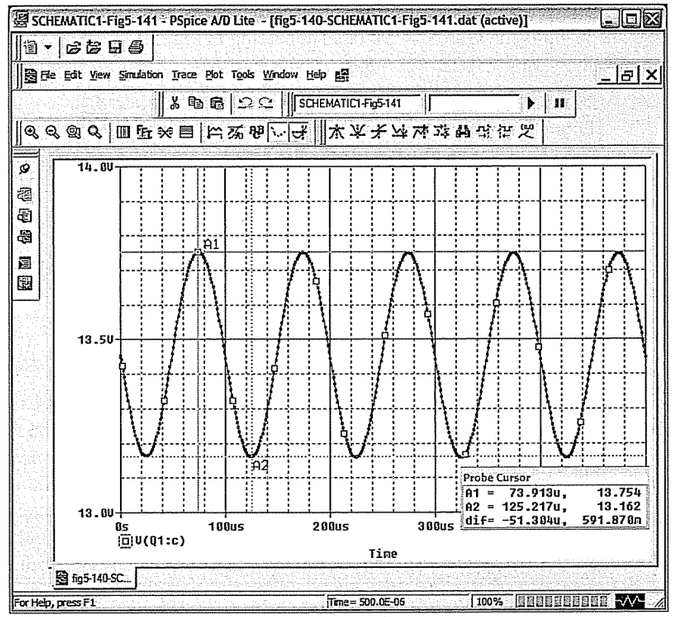


FIG. 5.145

Demonstrating the use of cursors to read specific points on a plot.

right-clicking of the mouse, a second intersection, defined by **A2**, will appear, which can moved in the same way with its time and voltage appearing in the same dialog box. Note that if **A2** is placed close to the negative peak, the difference in time is 51.304 μs (as displayed in the same box), which is very close to one-half the period of the waveform. The difference in magnitude is 591.87 mV, which is very close to the 600 mV obtained earlier.

Voltage-Divider Configuration–Controlled Source Substitution The results obtained for any analysis using the transistors provided in the PSpice listing will always be somewhat different from those obtained with an equivalent model that only includes the effect of beta and r_e. This was clearly demonstrated for the network of Fig. 5.140. If a solution is desired that is limited to the approximate model used in the hand calculations, then the transistor must be represented by a model such as appearing in Fig. 5.146.

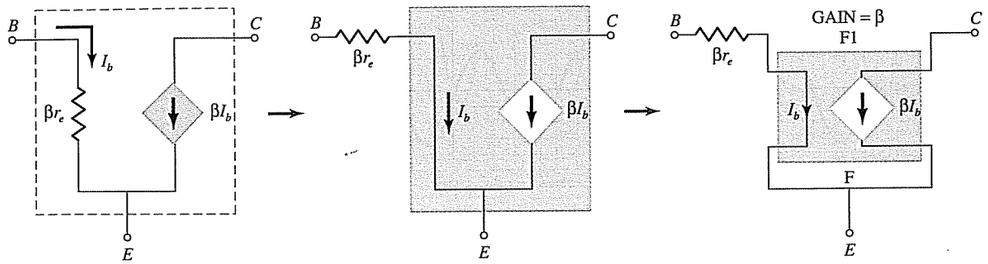


FIG. 5.146
Using a controlled source to represent the transistor of Fig. 5.140.

For Example 5.5, β is 90, with $\beta r_e = 1.66\,\text{k}\Omega$. The current-controlled current source (CCCS) is found in the **ANALOG** library as part **F**. After selection, an **OK**, and the graphical symbol for the CCCS will appear on the screen as shown in Fig. 5.147. Since it does not appear within the basic structure of the CCCS, it must be added in series with the controlling current that appears as an arrow in the symbol. Note the added 1.66-kΩ resistor, labeled **beta-re** in Fig. 5.147. Double-clicking on the CCCS symbol will result in the **Property Editor** dialog box, in which the **GAIN** can be set to 90. It is the only change to be made in the listing. Then select **Display** followed by **Name and Value** and exit (**x**) the dialog box. The result is the **GAIN = 90** label appearing in Fig. 5.147.

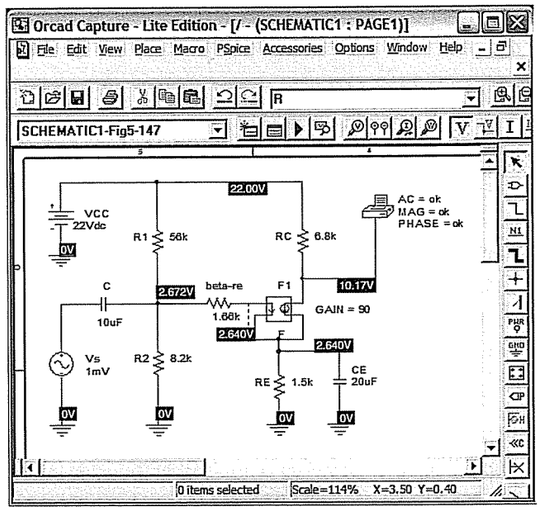
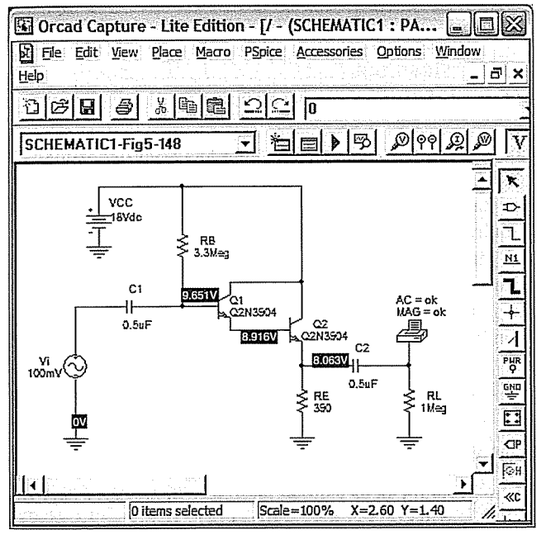


FIG. 5.147
Substituting the controlled source of Fig. 5.146 for the transistor of Fig. 5.140.

A simulation and the dc levels of Fig. 5.147 will appear. The dc levels do not match the earlier results because the network is a mix of dc and ac parameters. The equivalent model substituted in Fig. 5.147 is a representation of the transistor under ac conditions, not dc biasing conditions. When the software package analyzes the network from an ac viewpoint it will work with an ac equivalent of Fig. 5.147, which will not include the dc parameters. The **Output File** will reveal that the output collector voltage is 368.3 mV, or a gain of 368.3, essentially an exact match with the handwritten solution of 368.76. The effects of r_o could be included by simply placing a resistor in parallel with the controlled source.

Darlington Configuration Although PSpice does have two Darlington pairs in the library, individual transistors are employed in Fig. 5.148 to test the solution to Example 5.20. The details of setting up the network have been covered in the preceding sections and chapters. For each transistor I_s is set to 100E-18 and β to 89.4. The applied frequency is 10 kHz. A simulation of the network results in the dc levels appearing in Fig. 5.148a and the **Output File** in Fig. 5.148b. In particular, note that the voltage drop between base and emitter for both transistors is $9.651\,\text{V} - 8.063\,\text{V} = 1.588\,\text{V}$ compared to the 1.6 V assumed in the example—a very close match. Recall that the drop across Darlington pairs is typically about 1.6 V and not simply twice that of a single transistor, or $2(0.7\,\text{V}) = 1.4\,\text{V}$. The output voltage of 99.36 mV is very close to the 99.80 mV obtained in Example 5.24.



(a)

```
****     BJT MODEL PARAMETERS

         Q2N3904
         NPN
IS    100.000000E-18
BF    89.4
NF    1
BR    1
NR    1
CN    2.42
D     .87

****     SMALL SIGNAL BIAS SOLUTION       TEMPERATURE =   27.000 DEG C

NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE
(N00623)  18.0000 (N00659)  8.9155 (N00737)  9.6513 (N00769)  0.0000
(N00902)   0.0000 (N01429)  8.0632

****     AC ANALYSIS

 FREQ        VM(N00902)

 1.000E+04  9.936E-02
```

(b)

FIG. 5.148
(a) Design Center schematic of Darlington network; (b) output listing for circuit of part (a) (edited).

Multisim

Collector Feedback Configuration Since the collector feedback configuration generated the most complex equations for the various parameters of a BJT network, it seems appropriate that Multisim be used to verify the conclusions of Example 5.12. The network appears as shown in Fig. 5.149 using the "virtual" transistor from the **Transistor family** toolbar. Recall from the previous chapter that transistors are obtained by first selecting the **Transistor** keypad appearing as the fourth option down on the first vertical toolbar. Once chosen, the **Select a Component** dialog box will appear; under the **Family** heading, select **TRANSISTORS**. Under the **Component** heading, choose **BJT_NPN_VIRTUAL**, followed by **OK** to place it on the screen. The result is the symbol and labels appearing in Fig. 5.149. We must now check that the beta value is 200 to match the example under investigation. This can be accomplished using one of two paths. In Chapter 4 we used the

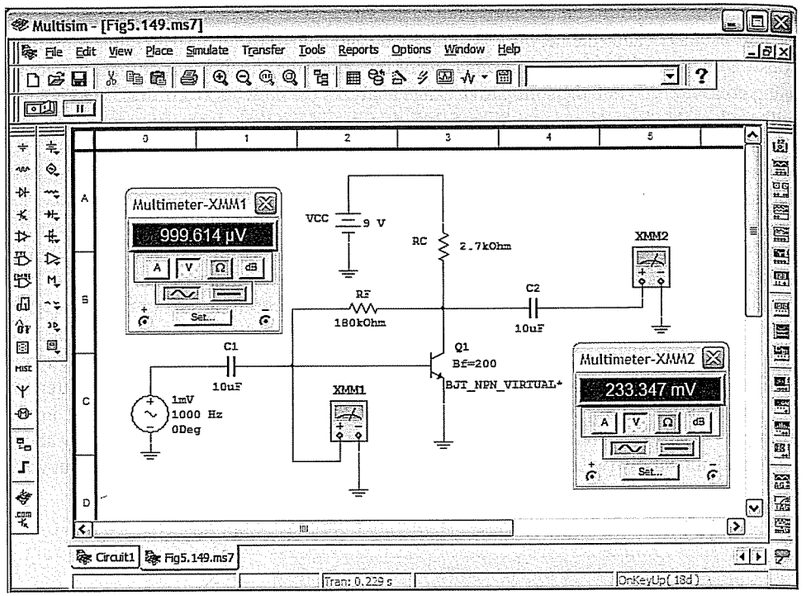


FIG. 5.149

Network of Example 5.12 redrawn using Multisim.

EDIT-PROPERTIES sequence, but here we will simply double-click on the symbol to obtain the **TRANSISTORS_VIRTUAL** dialog box. Under **Value**, select **Edit Model** to obtain the **Edit Model** dialog box (the dialog box has a different appearance from that obtained with the other route and requires a different sequence to change its parameters). The value of **BF** appears as **100**, which must be changed to 200. First select the **BF** line to make it blue all the way across. Then place the cursor directly over the 100 value and select it to isolate it as the quantity to be changed. After deleting the 100, type in the desired 200 value. Then click the **BF** line directly under the **Name** heading and the entire line will be blue again, but now with the 200 value. Then choose **Change Part Model** at the bottom left of the dialog box and the **TRANSISTORS-VIRTUAL** dialog box will appear again. Select **OK** and $\beta = 200$ will be set for the virtual transistor. Note again the asterisk next to the BJT label to indicate the parameters of the device have been changed from the default values.

This will be the first opportunity to set up an ac source. First, it is important to realize that there are two types of ac sources available, one whose value is in rms units, the other with its peak value displayed. **The option under Power Sources uses rms values, whereas the ac source under Signal Sources uses peak values.** Since meters display rms values, the **Power Sources** option will be used here. Once **Source** (the first option at the top of the first vertical toolbar) is selected, the **Select a Component** dialog box will appear. Under the **Family** listing select **POWER_SOURCES** and then select **AC POWER** under the **Component** listing. An **OK**, and the source will appear on the screen with four pieces of information. The label **V1** can be deleted by first double-clicking on the source symbol to obtain the **POWER_SOURCES** dialog box. Select **Display** and disengage **Use Schematic Global Settings**. To remove the label **V1**, disengage the **reference ID** option. An **OK**, and the **V1** will disappear from the screen. Next the value has to be set at 1 mV, a process initiated by selecting **Value** in the dialog box and then changing the **Voltage (RMS)** to 1 mV. Take particular note of the **RMS** in the parentheses as mentioned above. The units of mV can be set using the scroll keys to the right of the magnitude of the source. After you change the **Voltage** to **1 mV**, an **OK** will place this new value on the screen. The frequency of **1000 Hz** can be set in the same way. The **0**-degree phase shift happens to be the default value.

The label **Bf = 200** is set in the same way as described in Chapter 4. The two multimeters are obtained using the first option at the top of the right vertical toolbar. The meter faces appearing in Fig. 5.149 were obtained by simply double-clicking on the multimeter symbols on the schematic. Both were set to read voltages, the magnitudes of which will be in rms units.

After simulation the results of Fig. 5.149 appear. Note that the meter **XMM1** is not reading the 1 mV expected. This is due to the small drop in voltage across the input capacitor at 1 kHz. Certainly, however, it is very close to 1 mV. The output of 233.347 mV quickly reveals that the gain of the transistor configuration is about 233.3, which is a very close match with the 240 obtained in Example 5.12.

Darlington Configuration Applying Multisim to the network of Fig. 5.148 results in the printout of Fig. 5.150. For each transistor the parameters were changed to **Is = 100E-18 A** and **Bf = 89.4** using the technique described above. For practice purposes the ac signal source was employed rather than the power source. The peak value of the applied signal is set at 100 mV, but note that the multimeter reads the effective or rms value at 70.708 mV. The indicators provide a confirmation of the PSpice analysis, with the base voltage of Q_1 at 9.637 V, compared to 9.651 V, and the emitter voltage of Q_2 at 8.059 V, compared to 8.063 V. The rms value of the output voltage is 70.256 mV, resulting in a peak value of $(1.414)(70.256\,\text{mV}) = 99.342\,\text{mV}$, which compares very well with the 99.36 mV obtained using PSpice. Although it was not employed here, Multisim provides a number of Darlington configurations in its library.

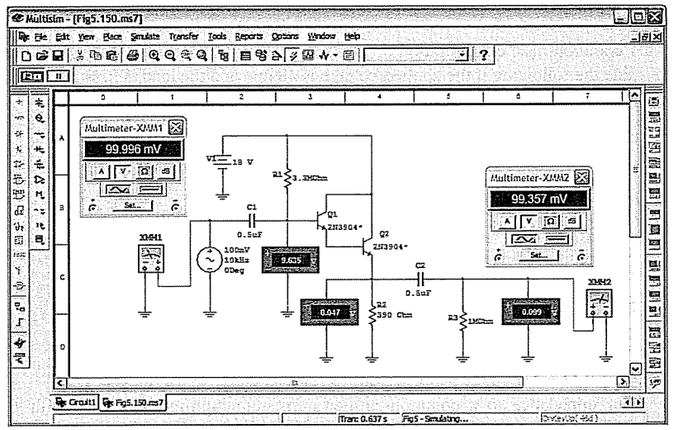


FIG. 5.150

Network of Fig. 5.148 analyzed using Multisim.

PROBLEMS

**Note:* Asterisks indicate more difficult problems.

5.2 Amplification in the AC Domain

1. **a.** What is the expected amplification of a BJT transistor amplifier if the dc supply is set to zero volts?
   b. What will happen to the output ac signal if the dc level is insufficient? Sketch the effect on the waveform.
   c. What is the conversion efficiency of an amplifier in which the effective value of the current through a 2.2-kΩ load is 5 mA and the drain on the 18-V dc supply is 3.8 mA?
2. Can you think of an analogy that would explain the importance of the dc level on the resulting ac gain?

5.3 BJT Transistor Modeling

3. What is the reactance of a 10-μF capacitor at a frequency of 1 kHz? For networks in which the resistor levels are typically in the kilohm range, is it a good assumption to use the short-circuit equivalence for the conditions just described? How about at 100 kHz?
4. Given the common-base configuration of Fig. 5.151, sketch the ac equivalent using the notation for the transistor model appearing in Fig. 5.5.

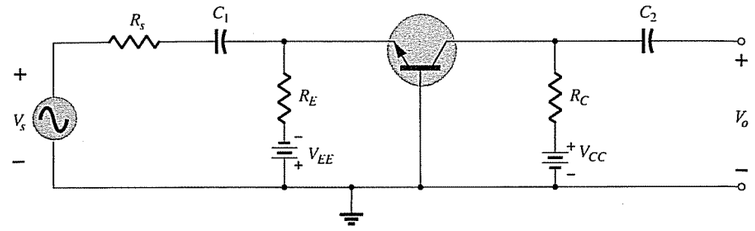


FIG. 5.151
Problem 4.

5.4 The r_e Transistor Model

5. For the common-base configuration of Fig. 5.7, an ac signal of 10 mV is applied, resulting in an emitter current of 0.5 mA. If $\alpha = 0.980$, determine:
   a. Z_i.
   b. V_o if $R_L = 1.2\,\text{k}\Omega$.
   c. $A_v = V_o/V_i$.
   d. Z_o with $r_o = \infty\,\Omega$.
   e. $A_i = I_o/I_i$.
   f. I_b.
6. For the common-base configuration of Fig. 5.7, the emitter current is 3.2 mA and α is 0.99. Determine the following if the applied voltage is 48 mV and the load is 2.2 kΩ.
   a. r_e.
   b. Z_i.
   c. I_c.
   d. V_o.
   e. A_v.
   f. I_b.
7. Using the model of Fig. 5.17, determine the following for a common-emitter amplifier if $\beta = 80$, $I_E(\text{dc}) = 2\,\text{mA}$, and $r_o = 40\,\text{k}\Omega$.
   a. Z_i.
   b. I_b.
   c. $A_i = I_o/I_i = I_L/I_b$ if $R_L = 1.2\,\text{k}\Omega$.
   d. A_v if $R_L = 1.2\,\text{k}\Omega$.
8. The input impedance to a common-emitter transistor amplifier is $1.2\,\text{k}\Omega$ with $\beta = 140$, $r_o = 50\,\text{k}\Omega$, and $R_L = 2.7\,\text{k}\Omega$. Determine:
   a. r_e.
   b. I_b if $V_i = 30\,\text{mV}$.
   c. I_c.
   d. $A_i = I_o/I_i = I_L/I_b$.
   e. $A_v = V_o/V_i$.

5.5 The Hybrid Equivalent Model

9. Given $I_E(\text{dc}) = 1.2\,\text{mA}$, $\beta = 120$, and $r_o = 40\,\text{k}\Omega$, sketch the following:
   a. Common-emitter hybrid equivalent model.
   b. Common-emitter r_e equivalent model.
   c. Common-base hybrid equivalent model.
   d. Common-base r_e equivalent model.
10. Given $h_{ie} = 2.4\,\text{k}\Omega$, $h_{fe} = 100$, $h_{re} = 4 \times 10^{-4}$, and $h_{oe} = 25\,\mu\text{S}$, sketch the following:
    a. Common-emitter hybrid equivalent model.
    b. Common-emitter r_e equivalent model.
    c. Common-base hybrid equivalent model.
    d. Common-base r_e equivalent model.
11. Redraw the common-emitter network of Fig. 5.3 for the ac response with the approximate hybrid equivalent model substituted between the appropriate terminals.
12. Redraw the network of Fig. 5.152 for the ac response with the r_e model inserted between the appropriate terminals. Include r_o.
13. Redraw the network of Fig. 5.153 for the ac response with the r_e model inserted between the appropriate terminals. Include r_o.

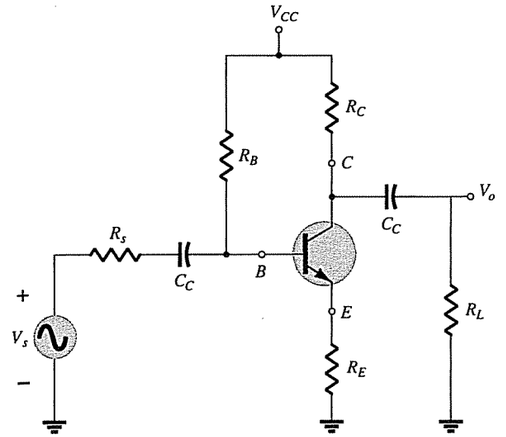


FIG. 5.152
Problem 12.

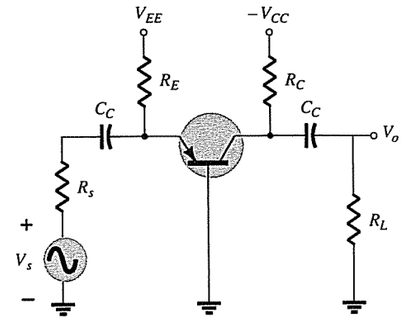


FIG. 5.153
Problem 13.

14. Given the typical values of $h_{ie} = 1\,\text{k}\Omega$, $h_{re} = 2 \times 10^{-4}$, and $A_v = -160$ for the input configuration of Fig. 5.154:
    a. Determine V_o in terms of V_i.
    b. Calculate I_b in terms of V_i.
    c. Calculate I_b if $h_{re}V_o$ is ignored.
    d. Determine the percentage difference in I_b using the following equation:

$$\%\ \text{difference in } I_b = \frac{I_b(\text{without } h_{re}) - I_b(\text{with } h_{re})}{I_b(\text{without } h_{re})} \times 100\%$$

    e. Is it a valid approach to ignore the effects of $h_{re}V_o$ for the typical values employed in this example?

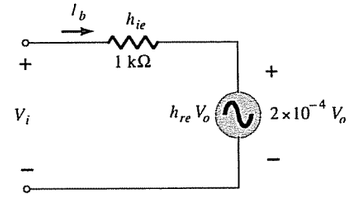


FIG. 5.154
Problems 14 and 16.

15. Given the typical values of $R_L = 2.2\,\text{k}\Omega$ and $h_{oe} = 20\,\mu\text{S}$, is it a good approximation to ignore the effects of $1/h_{oe}$ on the total load impedance? What is the percentage difference in total loading on the transistor using the following equation?

$$\%\ \text{difference in total load} = \frac{R_L - R_L\|(1/h_{oe})}{R_L} \times 100\%$$

16. Repeat Problem 14 using the average values of the parameters of Fig. 5.18 with $A_v = -180$.
17. Repeat Problem 15 for $R_L = 3.3\,\text{k}\Omega$ and the average value of h_{oe} in Fig. 5.18.

5.6 Hybrid π Model

18. a. Sketch the Giacoletto (hybrid π) model for a common-emitter transistor if $r_b = 4\,\Omega$, $C_\pi = 5\,\text{pF}$, $C_u = 1.5\,\text{pF}$, $h_{oe} = 18\,\mu\text{S}$, $\beta = 120$, and $r_e = 14$.
    b. If the applied load is $1.2\,\text{k}\Omega$ and the source resistance is $250\,\Omega$, draw the approximate hybrid π model for the low- and mid-frequency range.

5.7 Variations of Transistor Parameters

For Problems 19 through 25, use Figs. 5.31 through 5.33.

19. **a.** Using Fig. 5.31, determine the magnitude of the percentage change in h_{fe} for an I_C change from 0.2 mA to 1 mA using the equation

$$\%\ \text{change} = \left| \frac{h_{fe}(0.2\ \text{mA}) - h_{fe}(1\ \text{mA})}{h_{fe}(0.2\ \text{mA})} \right| \times 100\%$$

b. Repeat part (a) for an I_C change from 1 mA to 5 mA.

20. Repeat Problem 19 for h_{ie} (same changes in I_C).

21. **a.** If $h_{oe} = 20\ \mu\text{S}$ at $I_C = 1\ \text{mA}$ on Fig. 5.31, what is the approximate value of h_{oe} at $I_C = 0.2\ \text{mA}$?

b. Determine its resistive value at 0.2 mA and compare to a resistive load of 6.8 kΩ. Is it a good approximation to ignore the effects of $1/h_{oe}$ in this case?

22. **a.** If $h_{oe} = 20\ \mu\text{S}$ at $I_C = 1\ \text{mA}$ of Fig. 5.31, what is the approximate value of h_{oe} at $I_C = 10\ \text{mA}$?

b. Determine its resistive value at 10 mA and compare to a resistive load of 6.8 kΩ. Is it a good approximation to ignore the effects of $1/h_{oe}$ in this case?

23. **a.** If $h_{re} = 2 \times 10^{-4}$ at $I_C = 1\ \text{mA}$ on Fig. 5.31, determine the approximate value of h_{re} at 0.1 mA.

b. For the value of h_{re} determined in part (a), can h_{re} be ignored as a good approximation if $A_v = 210$?

24. **a.** Based on a review of the characteristics of Fig. 5.31, which parameter changed the least for the full range of collector current?

b. Which parameter changed the most?

c. What are the maximum and minimum values of $1/h_{oe}$? Is the approximation $1/h_{oe} \| R_L \cong R_L$ more appropriate at high or low levels of collector current?

d. In which region of current spectrum is the approximation $h_{re}V_{ce} \cong 0$ the most appropriate?

25. **a.** Based on a review of the characteristics of Fig. 5.33, which parameter changed the most with increase in temperature?

b. Which changed the least?

c. What are the maximum and minimum values of h_{fe}? Is the change in magnitude significant? Was it expected?

d. How does r_e vary with increase in temperature? Simply calculate its level at three or four points and compare their magnitudes.

e. In which temperature range do the parameters change the least?

5.8 Common-Emitter Fixed-Bias Configuration

26. For the network of Fig. 5.155:

a. Determine Z_i and Z_o.

b. Find A_v.

c. Repeat part (a) with $r_o = 20\ \text{k}\Omega$.

d. Repeat part (b) with $r_o = 20\ \text{k}\Omega$.

27. For the network of Fig. 5.156, determine V_{CC} for a voltage gain of $A_v = -200$.

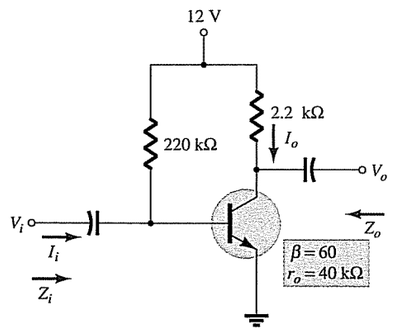


FIG. 5.155
Problem 26.

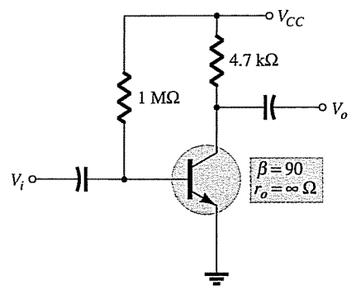


FIG. 5.156
Problem 27.

***28.** For the network of Fig. 5.157:

a. Calculate I_B, I_C, and r_e.

b. Determine Z_i and Z_o.

c. Calculate A_v.

d. Determine the effect of $r_o = 30\ \text{k}\Omega$ on A_v.

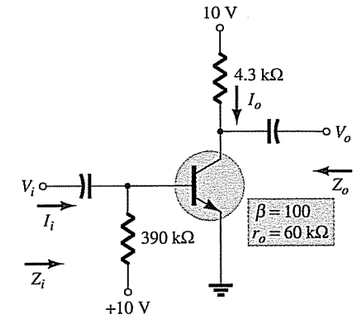


FIG. 5.157
Problem 28.

5.9 Voltage-Divider Bias

29. For the network of Fig. 5.158:

a. Determine r_e.

b. Calculate Z_i and Z_o.

c. Find A_v.

d. Repeat parts (b) and (c) with $r_o = 25\ \text{k}\Omega$.

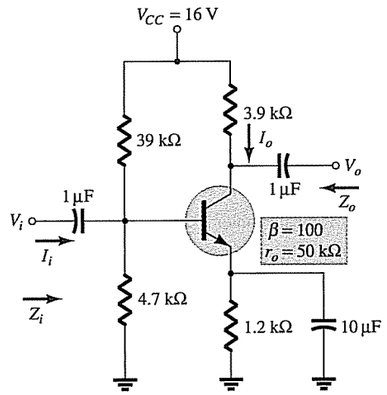


FIG. 5.158
Problem 29.

30. Determine V_{CC} for the network of Fig. 5.159 if $A_v = -160$ and $r_o = 100\ \text{k}\Omega$.

31. For the network of Fig. 5.160:

a. Determine r_e.

b. Calculate V_B and V_C.

c. Determine Z_i and $A_v = V_o/V_i$.

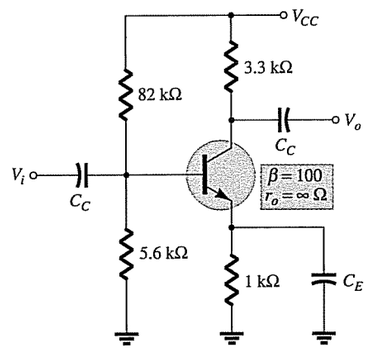


FIG. 5.159
Problem 30.

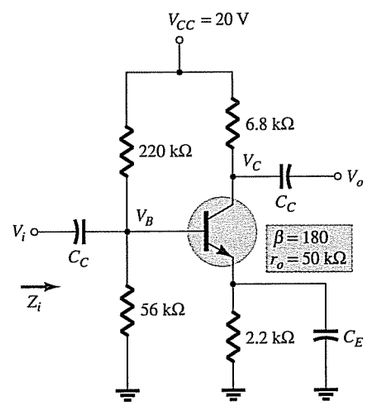


FIG. 5.160
Problem 31.

5.10 CE Emitter-Bias Configuration

32. For the network of Fig. 5.161:
- **a.** Determine r_e.
- **b.** Find Z_i and Z_o.
- **c.** Calculate A_v.
- **d.** Repeat parts (b) and (c) with $r_o = 20\,\text{k}\Omega$.

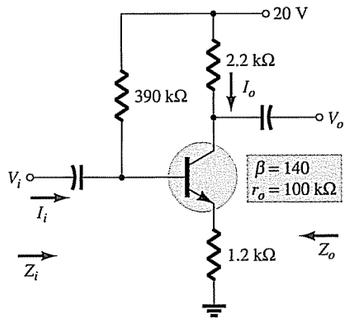


FIG. 5.161
Problems 32 and 34.

33. For the network of Fig. 5.162, determine R_E and R_B if $A_v = -10$ and $r_e = 3.8\,\Omega$. Assume that $Z_b = \beta R_E$.

34. Repeat Problem 32 with R_E bypassed. Compare results.

***35.** For the network of Fig. 5.163:
- **a.** Determine r_e.
- **b.** Find Z_i and A_v.

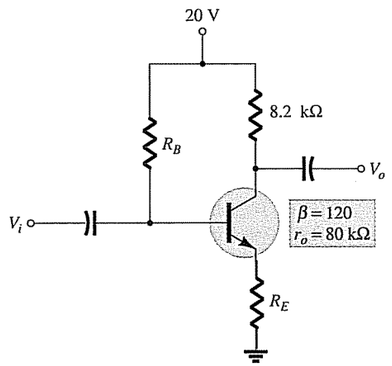


FIG. 5.162
Problem 33.

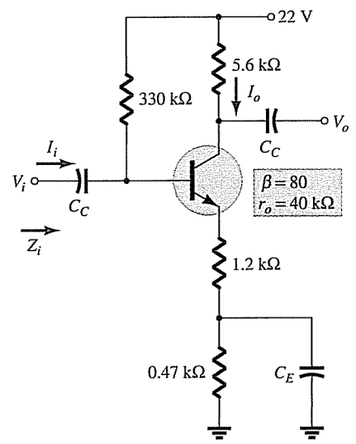


FIG. 5.163
Problem 35.

5.11 Emitter-Follower Configuration

36. For the network of Fig. 5.164:
- **a.** Determine r_e and βr_e.
- **b.** Find Z_i and Z_o.
- **c.** Calculate A_v.

***37.** For the network of Fig. 5.165:
- **a.** Determine Z_i and Z_o.
- **b.** Find A_v.
- **c.** Calculate V_o if $V_i = 1\,\text{mV}$.

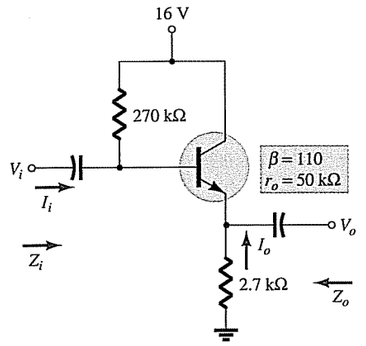


FIG. 5.164
Problem 36.

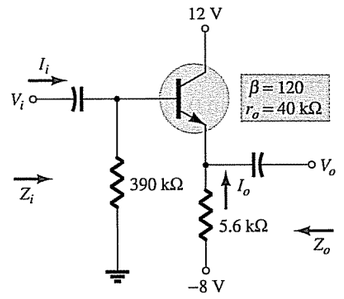


FIG. 5.165
Problem 37.

***38.** For the network of Fig. 5.166:
- **a.** Calculate I_B and I_C.
- **b.** Determine r_e.
- **c.** Determine Z_i and Z_o.
- **d.** Find A_v.

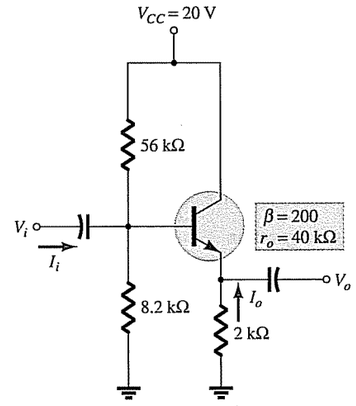


FIG. 5.166
Problem 38.

5.12 Common-Base Configuration

39. For the common-base configuration of Fig. 5.167:
- **a.** Determine r_e.
- **b.** Find Z_i and Z_o.
- **c.** Calculate A_v.

***40.** For the network of Fig. 5.168, determine A_v.

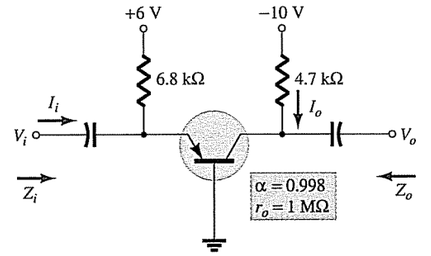


FIG. 5.167
Problem 39.

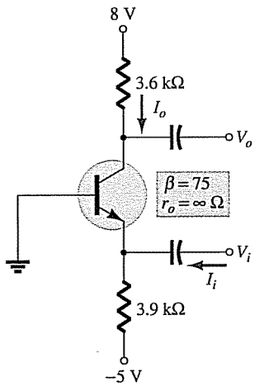


FIG. 5.168
Problem 40.

5.13 Collector Feedback Configuration

41. For the collector feedback configuration of Fig. 5.169:
- **a.** Determine r_e.
- **b.** Find Z_i and Z_o.
- **c.** Calculate A_v.

***42.** Given $r_e = 10\ \Omega$, $\beta = 200$, $A_v = -160$, and $A_i = 19$ for the network of Fig. 5.170, determine R_C, R_F, and V_{CC}.

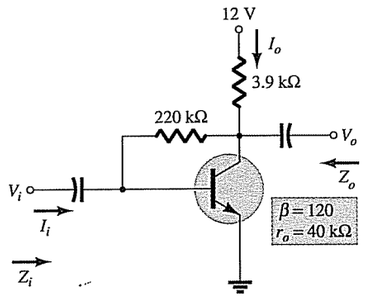


FIG. 5.169
Problem 41.

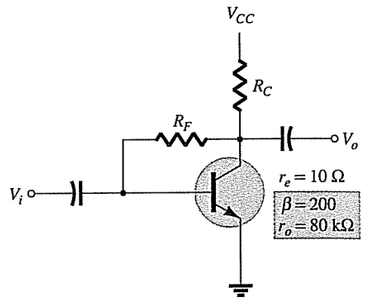


FIG. 5.170
Problem 42.

***43.** For the network of Fig. 5.64:
- **a.** Derive the approximate equation for A_v.
- **b.** Derive the approximate equations for Z_i and Z_o.
- **c.** Given $R_C = 2.2\ \text{k}\Omega$, $R_F = 120\ \text{k}\Omega$, $R_E = 1.2\ \text{k}\Omega$, $\beta = 90$, and $V_{CC} = 10$ V, calculate the magnitudes of A_v, Z_i, and Z_o using the equations of parts (a) and (b).

5.14 Collector DC Feedback Configuration

44. For the network of Fig. 5.171:
- **a.** Determine Z_i and Z_o.
- **b.** Find A_v.

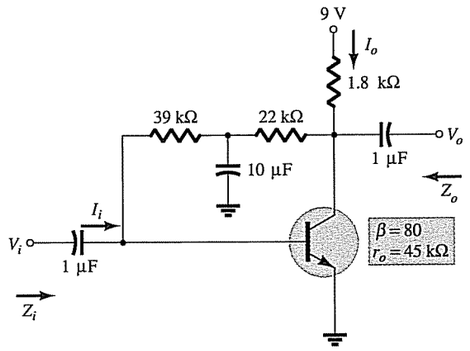


FIG. 5.171
Problem 44.

5.15 Determining the Current Gain

45. Determine the current gain for the common-emitter configuration of Fig. 5.155.

46. Determine the current gain for the common-emitter configuration of Fig. 5.157.

47. Determine the current gain for the voltage-divider network of Fig. 5.158.

48. Determine the current gain for the CE emitter-bias network of Fig. 5.161.

49. Determine the current gain for the emitter-follower configuration of Fig. 5.166.

50. Determine the current gain for the common-base configuration of Fig. 5.168.

51. Determine the current gain for the collector feedback configuration of Fig. 5.169.

52. Determine the current gain for the collector dc feedback configuration of Fig. 5.171.

5.16–5.17 Effect of R_L and R_s and Two-Port Systems Approach

***53.** For the fixed-bias configuration of Fig. 5.172:
- **a.** Determine $A_{v_{NL}}$, Z_i, and Z_o.
- **b.** Sketch the two-port model of Fig. 5.77 with the parameters determined in part (a) in place.
- **c.** Calculate the gain A_v.
- **d.** Determine the current gain A_i.
- **e.** Determine A_v, A_i, Z_i, and Z_o using the r_e model and compare with the solutions above.

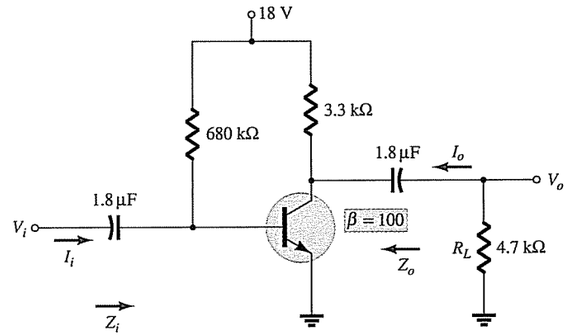


FIG. 5.172
Problems 53 and 54.

54. **a.** Determine the voltage gain A_v for the network of Fig. 5.172 for $R_L = 4.7$, 2.2, and 0.5 kΩ. What is the effect of decreasing levels of R_L on the voltage gain?
- **b.** How will Z_i, Z_o, and $A_{v_{NL}}$ change with decreasing values of R_L?

***55.** For the network of Fig. 5.173:
- **a.** Determine $A_{v_{NL}}$, Z_i, and Z_o.
- **b.** Sketch the two-port model of Fig. 5.77 with the parameters determined in part (a) in place.
- **c.** Determine A_v.
- **d.** Determine A_{v_s}.
- **e.** Determine A_{v_s} using the r_e model and compare the results to that obtained in part (d).
- **f.** Change R_s to 1 kΩ and determine A_v. How does A_v change with the level of R_s?
- **g.** Change R_s to 1 kΩ and determine A_{v_s}. How does A_{v_s} change with the level of R_s?
- **h.** Change R_s to 1 kΩ and determine $A_{v_{NL}}$, Z_i, and Z_o. How do they change with change in R_s?

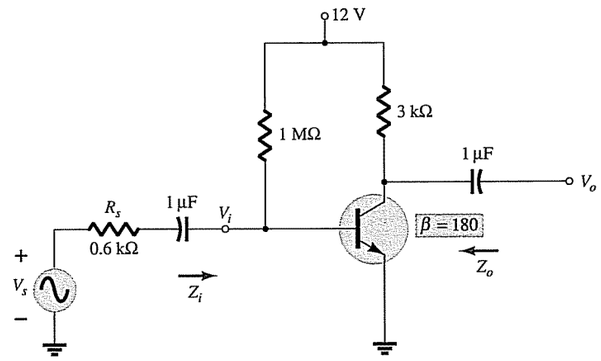


FIG. 5.173
Problem 55.

*56. For the network of Fig. 5.174:
- a. Determine $A_{v_{NL}}$, Z_i, and Z_o.
- b. Sketch the two-port model of Fig. 5.77 with the parameters determined in part (a) in place.
- c. Determine A_v and A_{v_s}.
- d. Calculate A_i.
- e. Change R_L to 5.6 kΩ and calculate A_{v_s}. What is the effect of increasing levels of R_L on the gain?
- f. Change R_s to 0.5 kΩ (with R_L at 2.7 kΩ) and comment on the effect of reducing R_s on A_{v_s}.
- g. Change R_L to 5.6 kΩ and R_s to 0.5 kΩ and determine the new levels of Z_i and Z_o. How are the impedance parameters affected by changing levels of R_L and R_s?

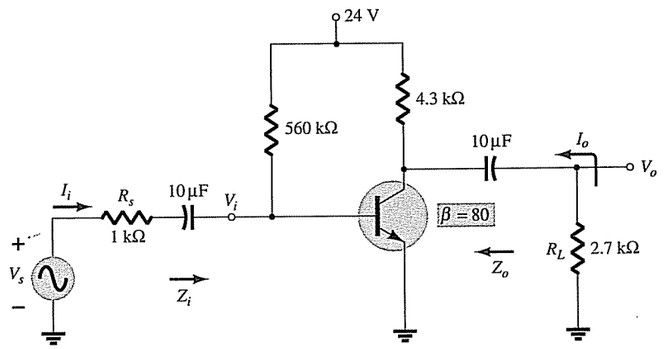


FIG. 5.174
Problem 56.

57. For the voltage-divider configuration of Fig. 5.175:
- a. Determine $A_{v_{NL}}$, Z_i, and Z_o.
- b. Sketch the two-port model of Fig. 5.77 with the parameters determined in part (a) in place.
- c. Calculate the gain A_v.
- d. Determine the current gain A_i.
- e. Determine A_v, A_i, and Z_o using the r_e model and compare solutions.

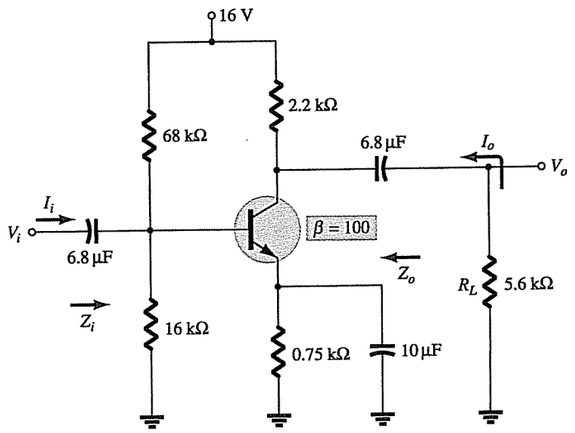


FIG. 5.175
Problem 57.

58. a. Determine the voltage gain A_v for the network of Fig. 5.175 with $R_L = 4.7$, 2.2, and 0.5 kΩ. What is the effect of decreasing levels of R_L on the voltage gain?
- b. How will Z_i, Z_o, and $A_{v_{NL}}$ change with decreasing levels of R_L?

59. For the emitter-stabilized network of Fig. 5.176:
- a. Determine $A_{v_{NL}}$, Z_i, and Z_o.
- b. Sketch the two-port model of Fig. 5.77 with the values determined in part (a).

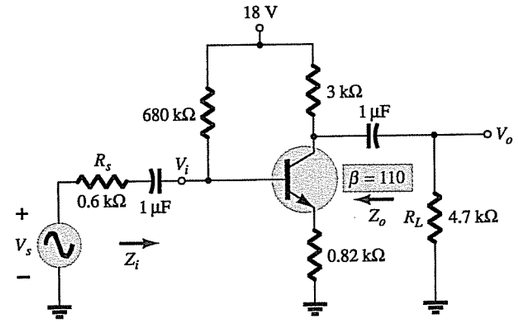


FIG. 5.176
Problem 59.

- c. Determine A_v and A_{v_s}.
- d. Change R_s to 1 kΩ. What is the effect on $A_{v_{NL}}$, Z_i, and Z_o?
- e. Change R_s to 1 kΩ and determine A_v and A_{v_s}. What is the effect of increasing levels of R_s on A_v and A_{v_s}?

*60. For the network of Fig. 5.177:
- a. Determine $A_{v_{NL}}$, Z_i, and Z_o.
- b. Sketch the two-port model of Fig. 5.77 with the values determined in part (a).
- c. Determine A_v and A_{v_s}.
- d. Change R_s to 1 kΩ and determine A_v and A_{v_s}. What is the effect of increasing levels of R_s on the voltage gains?
- e. Change R_s to 1 kΩ and determine $A_{v_{NL}}$, Z_i, and Z_o. What is the effect of increasing levels of R_s on the parameters?
- f. Change R_L to 5.6 kΩ and determine A_v and A_{v_s}. What is the effect of increasing levels of R_L on the voltage gains? Maintain R_s at its original level of 0.6 kΩ.

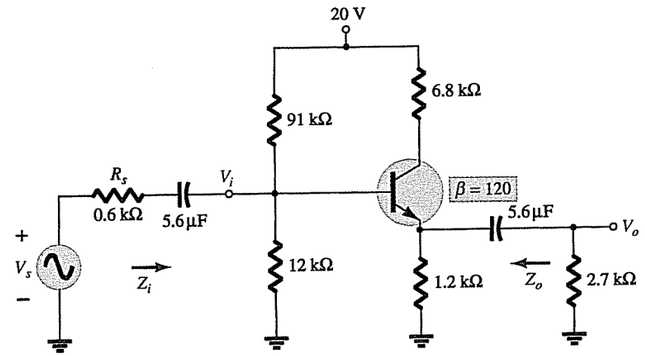


FIG. 5.177
Problem 60.

*61. For the common-base network of Fig. 5.178:
- a. Determine Z_i, Z_o, and $A_{v_{NL}}$.
- b. Sketch the two-port model of Fig. 5.77 with the parameters of part (a) in place.
- c. Determine A_v and A_{v_s}.
- d. Determine A_v and A_{v_s} using the r_e model and compare with the results of part (c).
- e. Change R_s to 0.5 kΩ and R_L to 2.2 kΩ and calculate A_v and A_{v_s}. What is the effect of changing levels of R_s and R_L on the voltage gains?
- f. Determine Z_o if R_s changed to 0.5 kΩ with all other parameters as appearing in Fig. 5.178. How is Z_o affected by changing levels of R_s?
- g. Determine Z_i if R_L is reduced to 2.2 kΩ. What is the effect of changing levels of R_L on the input impedance?

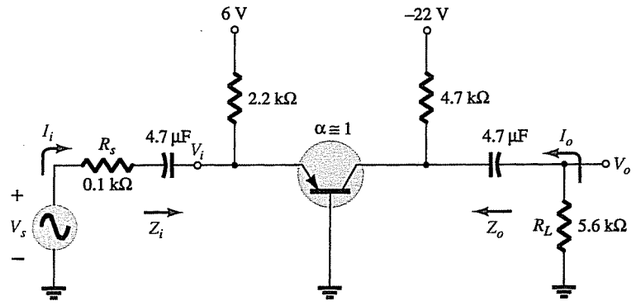


FIG. 5.178
Problem 61.

5.19 Cascaded Systems

*62. For the cascaded system of Fig. 5.179 with two identical stages, determine:
- **a.** The loaded voltage gain of each stage.
- **b.** The total gain of the system, A_v and A_{v_s}.
- **c.** The loaded current gain of each stage.
- **d.** The total current gain of the system.
- **e.** How Z_i is affected by the second stage and R_L.
- **f.** How Z_o is affected by the first stage and R_s.
- **g.** The phase relationship between V_o and V_i.

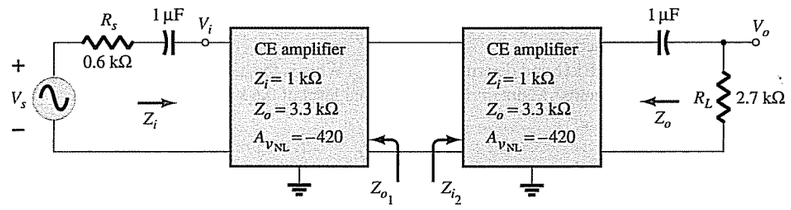


FIG. 5.179
Problem 62.

*63. For the cascaded system of Fig. 5.180, determine:
- **a.** The loaded voltage gain of each stage.
- **b.** The total gain of the system, A_v and A_{v_s}.
- **c.** The loaded current gain of each stage.
- **d.** The total current gain of the system.
- **e.** How Z_i is affected by the second stage and R_L.
- **f.** How Z_o is affected by the first stage and R_s.
- **g.** The phase relationship between V_o and V_i.

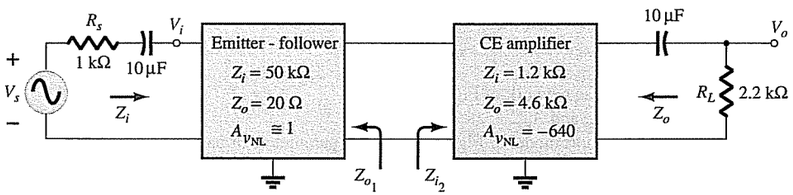


FIG. 5.180
Problem 63.

64. For the BJT cascade amplifier of Fig. 5.181, calculate the dc bias voltages and collector current for each stage.

65. Calculate the voltage gain of each stage and the overall ac voltage gain for the BJT cascade amplifier circuit of Fig. 5.181.

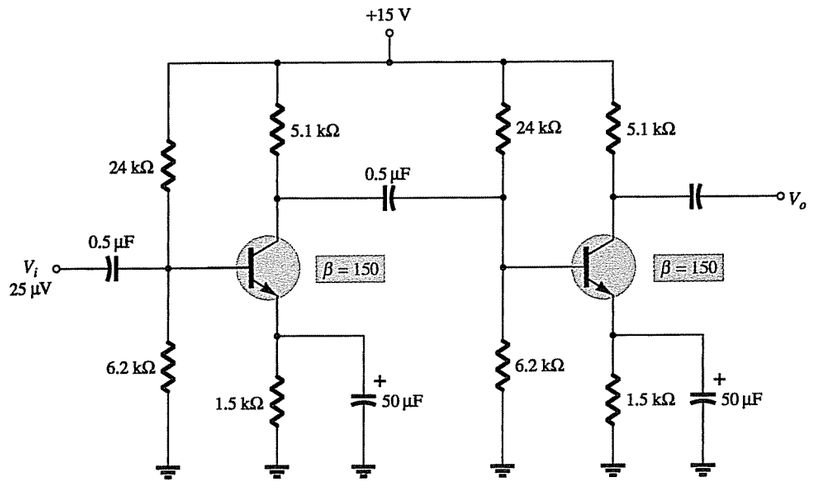


FIG. 5.181
Problems 64 and 65.

66. In the cascode amplifier circuit of Fig. 5.182, calculate the dc bias voltages V_{B_1}, V_{B_2}, and V_{C_2}.

*67. For the cascode amplifier circuit of Fig. 5.182, calculate the voltage gain A_v and output voltage V_o.

68. Calculate the ac voltage across a 10-kΩ load connected at the output of the circuit in Fig. 5.182.

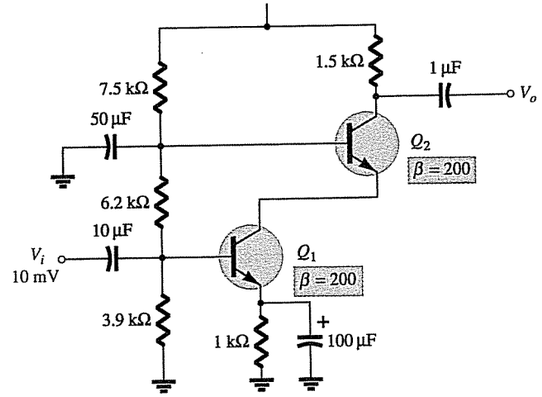


FIG. 5.182
Problems 66 through 68.

5.20 Darlington Connection

69. For the circuit of Fig. 5.183, calculate the dc bias voltage V_{E_2} and emitter current I_{E_2}.

*70. For the circuit of Fig. 5.183, calculate the amplifier voltage gain.

5.21 Feedback Pair

71. For the feedback pair circuit of Fig. 5.184, calculate the dc bias values of V_{B_1}, V_{C_2}, and I_C.

*72. Calculate the output ac voltage for the circuit of Fig. 5.184.

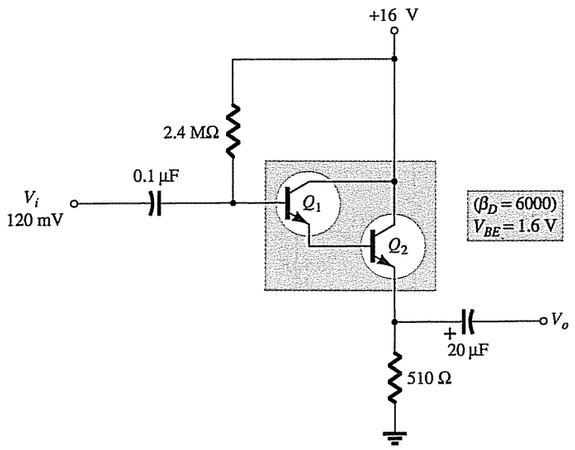


FIG. 5.183
Problems 69 and 70.

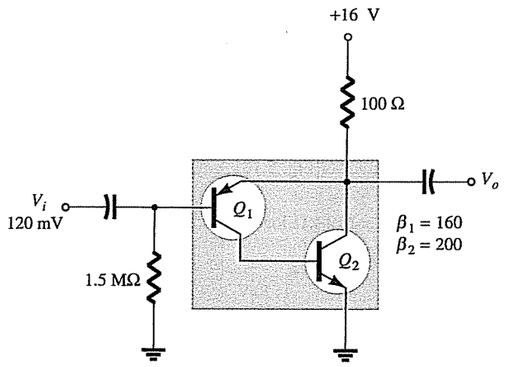


FIG. 5.184
Problems 71 and 72.

5.22 Current Mirror Circuits

73. Calculate the mirrored current I in the circuit of Fig. 5.185.

***74.** Calculate collector currents for Q_1 and Q_2 in Fig. 5.186.

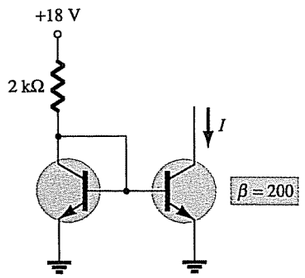


FIG. 5.185
Problem 73.

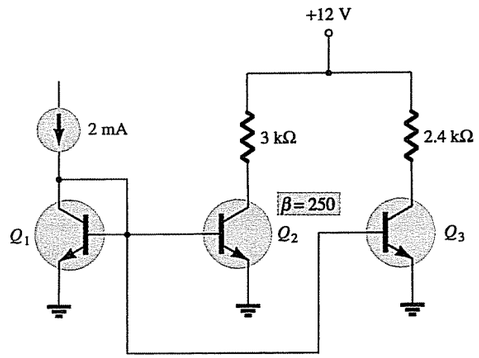


FIG. 5.186
Problem 74.

5.23 Current Source Circuits

75. Calculate the current through the 2-kΩ load in the circuit of Fig. 5.187.

76. For the circuit of Fig. 5.188, calculate the current I.

***77.** Calculate the current I in the circuit of Fig. 5.189.

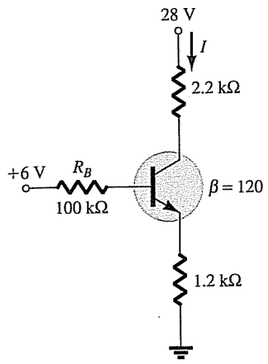


FIG. 5.187
Problem 75.

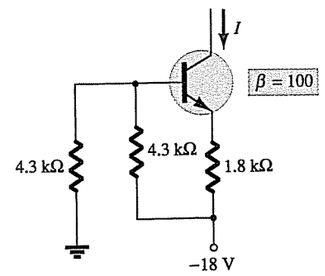


FIG. 5.188
Problem 76.

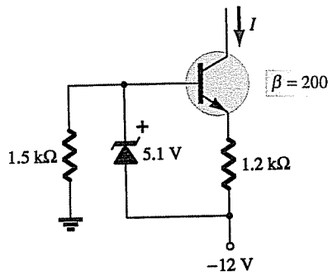


FIG. 5.189
Problem 77.

5.24 Approximate Hybrid Equivalent Circuit

78. **a.** Given $\beta = 120$, $r_e = 4.5\ \Omega$, and $r_o = 40\ \text{k}\Omega$, sketch the approximate hybrid equivalent circuit.

b. Given $h_{ie} = 1\ \text{k}\Omega$, $h_{re} = 2 \times 10^{-4}$, $h_{fe} = 90$, and $h_{oe} = 20\ \mu\text{S}$, sketch the r_e model.

79. For the network of Problem 26:

a. Determine r_e.
b. Find h_{fe} and h_{ie}.
c. Find Z_i and Z_o using the hybrid parameters.
d. Calculate A_v and A_i using the hybrid parameters.
e. Determine Z_i and Z_o if $h_{oe} = 50\ \mu\text{S}$.
f. Determine A_v and A_i if $h_{oe} = 50\ \mu\text{S}$.
g. Compare the solutions above with those of Problem 26. (Note: The solutions are available in Appendix E if Problem 26 was not performed.)

80. For the network of Fig. 5.190.

a. Determine Z_i and Z_o.
b. Calculate A_v and A_i.
c. Determine r_e and compare βr_e to h_{ie}.

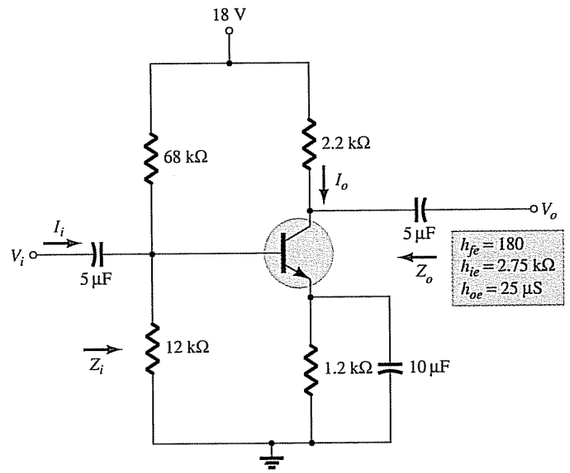


FIG. 5.190
Problem 80.

*81. For the common-base network of Fig. 5.191:
   a. Determine Z_i and Z_o.
   b. Calculate A_v and A_i.
   c. Determine α, β, r_e, and r_o.

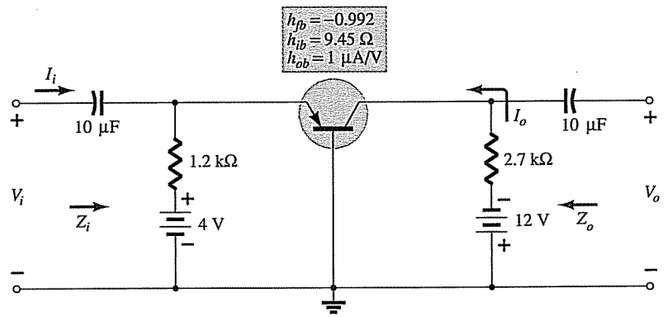


FIG. 5.191
Problem 81.

5.25 Complete Hybrid Equivalent Model

*82. Repeat parts (a) and (b) of Problem 80 with $h_{re} = 2 \times 10^{-4}$ and compare results.

*83. For the network of Fig. 5.192, determine:
   a. Z_i.
   b. A_v.
   c. $A_i = I_o/I_i$.
   d. Z_o.

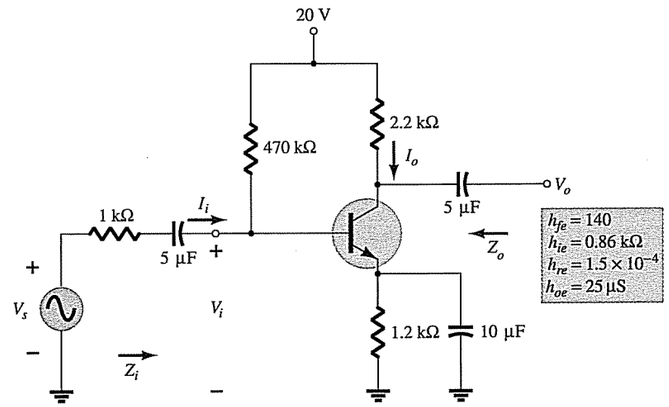


FIG. 5.192
Problem 83.

*84. For the common-base amplifier of Fig. 5.193, determine:
   a. Z_i.
   b. A_i.
   c. A_v.
   d. Z_o.

5.26 Troubleshooting

*85. Given the network of Fig. 5.194:
   a. Is the network of Fig. 5.194a properly biased?
   b. What problem in the network construction could cause V_B to be 6.22 V and obtain the output waveform of Fig. 5.194b?

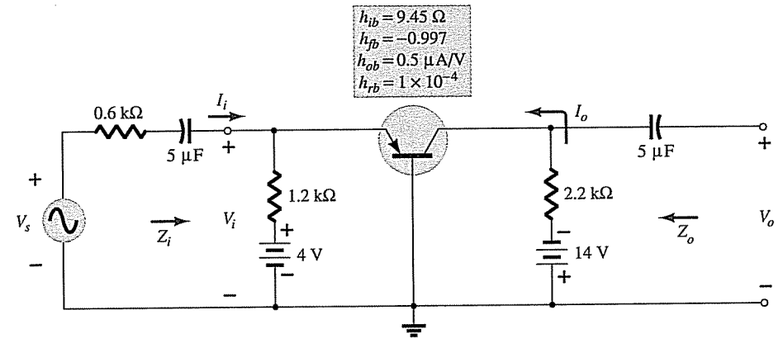


FIG. 5.193
Problem 84.

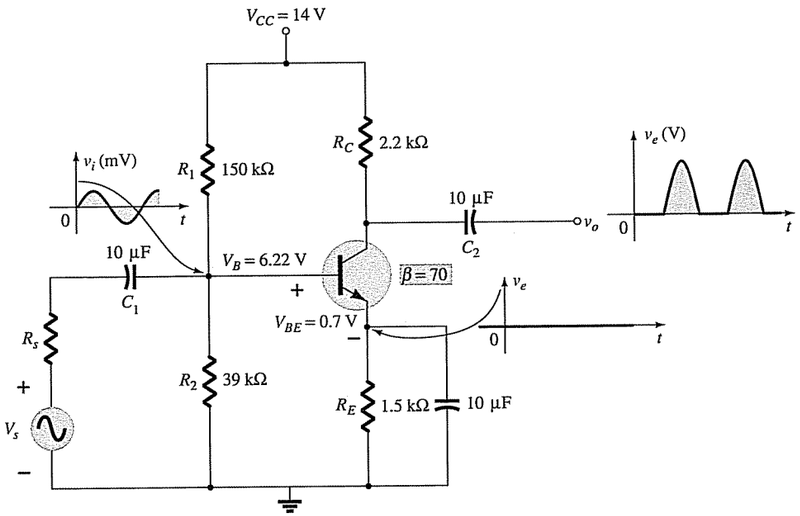


FIG. 5.194
Problem 85.

5.27 Computer Analysis

86. Using PSpice Windows, determine the voltage gain for the network of Fig. 5.39. Use Probe to display the input and output waveforms.

87. Using PSpice Windows, determine the voltage gain for the network of Fig. 5.46. Use Probe to display the input and output waveforms.

88. Using PSpice Windows, determine the voltage gain for the network of Fig. 5.59. Use Probe to display the input and output waveforms.

89. Using Multisim, determine the voltage gain for the network of Fig. 5.42.

90. Using Multisim, determine the voltage gain for the network of Fig. 5.54.

91. Using PSpice Windows, determine the level of V_o for $V_i = 1$ mV for the network of Fig. 5.85. For the capacitive elements assume a frequency of 1 kHz.

92. Repeat Problem 91 for the network of Fig. 5.86.

93. Repeat Problem 91 for the network of Fig. 5.92.

94. Repeat Problem 91 using Multisim.

95. Repeat Problem 93 using Multisim.

6 Field-Effect Transistors

CHAPTER OUTLINE

6.1 Introduction
6.2 Construction and Characteristics of JFETs
6.3 Transfer Characteristics
6.4 Specification Sheets (JFETs)
6.5 Instrumentation
6.6 Important Relationships
6.7 Depletion-Type MOSFET
6.8 Enhancement-Type MOSFET
6.9 MOSFET Handling
6.10 VMOS
6.11 CMOS
6.12 MESFETs
6.13 Summary Table
6.14 Summary
6.15 Computer Analysis

6.1 INTRODUCTION

The field-effect transistor (FET) is a three-terminal device used for a variety of applications that match, to a large extent, those of the BJT transistor described in Chapters 3 through 5. Although there are important differences between the two types of devices, there are also many similarities, which will be pointed out in the sections to follow.

The primary difference between the two types of transistors is the fact that:

The BJT transistor is a current-controlled device as depicted in Fig. 6.1a, whereas the JFET transistor is a voltage-controlled device as shown in Fig. 6.1b.

In other words, the current I_C in Fig. 6.1a is a direct function of the level of I_B. For the FET the current I_D will be a function of the voltage V_{GS} applied to the input circuit as shown in Fig. 6.1b. In each case the current of the output circuit is controlled by a parameter of the input circuit—in one case a current level and in the other an applied voltage.

Just as there are *npn* and *pnp* bipolar transistors, there are *n-channel* and *p-channel* field-effect transistors. However, it is important to keep in mind that the BJT transistor is a *bipolar* device—the prefix *bi* indicates that the conduction level is a function of two charge carriers, electrons and holes. The FET is a *unipolar* device depending solely on either electron (*n*-channel) or hole (*p*-channel) conduction.

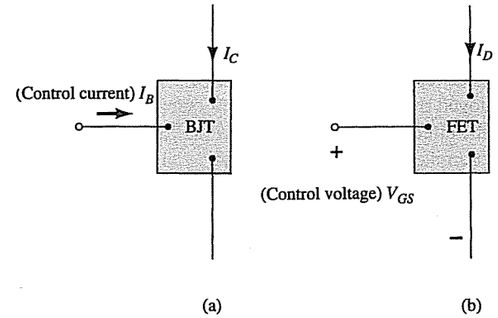


FIG. 6.1
(a) Current-controlled and (b) voltage-controlled amplifiers.

The term *field effect* in the name deserves some explanation. We are all familiar with the ability of a permanent magnet to draw metal filings to itself without the need for actual contact. The magnetic field of the permanent magnet envelopes the filings and attracts them to the magnet because the magnetic flux lines act so as to be as short as possible. For the FET an *electric field* is established by the charges present, which controls the conduction path of the output circuit without the need for direct contact between the controlling and controlled quantities.

There is a natural tendency when introducing a device with a range of applications similar to one already introduced to compare some of the general characteristics of one to those of the other:

One of the most important characteristics of the FET is its high input impedance.

At a level of 1 MΩ to several hundred megohms it far exceeds the typical input resistance levels of the BJT transistor configurations—a very important characteristic in the design of linear ac amplifier systems. On the other hand, the BJT transistor has a much higher sensitivity to changes in the applied signal. In other words, the variation in output current is typically a great deal more for BJTs than for FETs for the same change in the applied voltage.

For this reason:

Typical ac voltage gains for BJT amplifiers are a great deal more than for FETs.

In general:

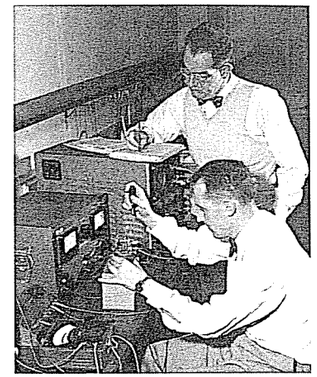
FETs are more temperature stable than BJTs, and FETs are usually smaller than BJTs, making them particularly useful in integrated-circuit (IC) chips.

The construction characteristics of some FETs, however, can make them more sensitive to handling than BJTs.

Three types of FETs are introduced in this chapter: the *junction field-effect transistor* (JFET), *the metal–oxide–semiconductor field-effect transistor* (MOSFET), and the *metal–semiconductor field-effect transistor* (MESFET). The MOSFET category is further broken down into *depletion* and *enhancement* types, which are both described. The MOSFET transistor has become one of the most important devices used in the design and construction of integrated circuits for digital computers. Its thermal stability and other general characteristics make it extremely popular in computer circuit design. However, as a discrete element in a typical top-hat container, it must be handled with care (to be discussed in a later section). The MESFET is a more recent development and takes full advantage of the high-speed characteristics of GaAs as the base semiconductor material. Although currently the more expensive option, the cost issue is often outweighed by the need for higher speeds in RF and computer designs.

Once the FET construction and characteristics have been introduced, the biasing arrangements will be covered in Chapter 7. The analysis performed in Chapter 4 using BJT transistors will prove helpful in the derivation of the important equations and understanding the results obtained for FET circuits.

Ian Munro Ross and G. C. Dacey (Fig. 6.2) were instrumental in the early stages of development of the field-effect transistor. Take particular note of the equipment used in 1955 for their research.



Drs. Ian Munro Ross (front) and G. C. Dacey jointly developed an experimental procedure for measuring the characteristics of a field-effect transistor in 1955.

Dr. Ross Born: Southport, England; PhD, Gonville and Caius College, Cambridge University; President Emeritus, AT&T Bell Labs; Fellow, IEEE; Member, the National Science Board; Chairman, National Advisory Committee on Semiconductors

Dr. Dacey Born: Chicago, Illinois; PhD, California Institute of Technology; Director of Solid-State Electronics Research, Bell Labs; Vice President, Research, Sandia Corporation; Member IRE, Tau Beta Pi, Eta Kappa Nu

FIG. 6.2
Early development of the field-effect transistor.
(Photo courtesy of AT&T Archives.)

6.2 CONSTRUCTION AND CHARACTERISTICS OF JFETs

As indicated earlier, the JFET is a three-terminal device with one terminal capable of controlling the current between the other two. In our discussion of the BJT transistor the *npn* transistor was employed through the major part of the analysis and design sections, with a section devoted to the effect of using a *pnp* transistor. For the JFET transistor the *n*-channel device will be the prominent device, with paragraphs and sections devoted to the effect of using a *p*-channel JFET.

The basic construction of the *n*-channel JFET is shown in Fig. 6.3. Note that the major part of the structure is the *n*-type material, which forms the channel between the embedded layers of *p*-type material. The top of the *n*-type channel is connected through an ohmic contact to a terminal referred to as the *drain (D)*, whereas the lower end of the same material is connected through an ohmic contact to a terminal referred to as the *source (S)*. The two *p*-type materials are connected together and to the *gate (G)* terminal. In essence, therefore, the drain and the source are connected to the ends of the *n*-type channel and the gate to the two layers of *p*-type material. In the absence of any applied potentials the JFET has two *p–n* junctions under no-bias conditions. The result is a depletion region at each junction, as shown in Fig. 6.3, that resembles the same region of a diode under no-bias conditions. Recall also that a depletion region is void of free carriers and is therefore unable to support conduction.

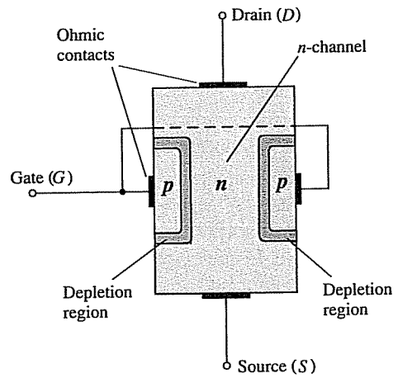


FIG. 6.3
Junction field-effect transistor (JFET).

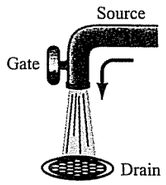


FIG. 6.4
Water analogy for the JFET control mechanism.

Analogies are seldom perfect and at times can be misleading, but the water analogy of Fig. 6.4 does provide a sense for the JFET control at the gate terminal and the appropriateness of the terminology applied to the terminals of the device. The source of water pressure can be likened to the applied voltage from drain to source, which establishes a flow of water (electrons) from the spigot (source). The "gate," through an applied signal (potential), controls the flow of water (charge) to the "drain." The drain and source terminals are at opposite ends of the *n*-channel as introduced in Fig. 6.3 because the terminology is defined for electron flow.

V_{GS} = 0 V, V_{DS} Some Positive Value

In Fig. 6.5, a positive voltage V_{DS} is applied across the channel and the gate is connected directly to the source to establish the condition $V_{GS} = 0$ V. The result is a gate and a source terminal at the same potential and a depletion region in the low end of each *p*-material similar to the distribution of the no-bias conditions of Fig. 6.3. The instant the voltage V_{DD} (=V_{DS}) is applied, the electrons are drawn to the drain terminal, establishing the conventional current I_D with the defined direction of Fig. 6.5. The path of charge flow clearly reveals that the drain and source currents are equivalent ($I_D = I_S$). Under the conditions in Fig. 6.5, the flow of charge is relatively uninhibited and is limited solely by the resistance of the *n*-channel between drain and source.

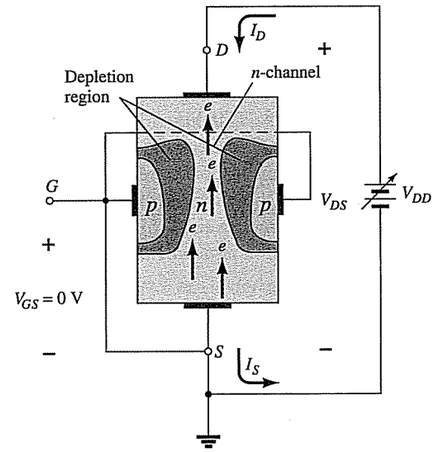


FIG. 6.5
JFET at $V_{GS} = 0$ V and $V_{DS} > 0$ V.

It is important to note that the depletion region is wider near the top of both *p*-type materials. The reason for the change in width of the region is best described through the help of Fig. 6.6. Assuming a uniform resistance in the *n*-channel, we can break down the resistance of the channel into the divisions appearing in Fig. 6.6. The current I_D will establish the voltage levels through the channel as indicated on the same figure. The result is that the upper region of the *p*-type material will be reverse-biased by about 1.5 V, with the lower region only reverse-biased by 0.5 V. Recall from the discussion of the diode operation that the greater the applied reverse bias, the wider is the depletion region—hence the distribution of the depletion region as shown in Fig. 6.6. The fact that the *p–n* junction is reverse-biased for the length of the channel results in a gate current of zero amperes, as shown in the same figure. The fact that $I_G = 0$ A is an important characteristic of the JFET.

As the voltage V_{DS} is increased from 0 V to a few volts, the current will increase as determined by Ohm's law and the plot of I_D versus V_{DS} will appear as shown in Fig. 6.7. The relative straightness of the plot reveals that for the region of low values of V_{DS}, the resistance is essentially constant. As V_{DS} increases and approaches a level referred to as V_P in Fig. 6.7, the depletion regions of Fig. 6.5 will widen, causing a noticeable reduction in the channel width. The reduced path of conduction causes the resistance to increase and the curve in the graph of Fig. 6.7 to occur. The more horizontal the curve, the higher the resistance, suggesting that the resistance is approaching "infinite" ohms in the horizontal region. If V_{DS} is increased to a level where it appears that the two depletion regions would "touch" as

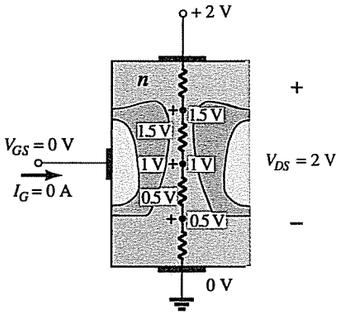


FIG. 6.6
Varying reverse-bias potentials across the p–n junction of an n-channel JFET.

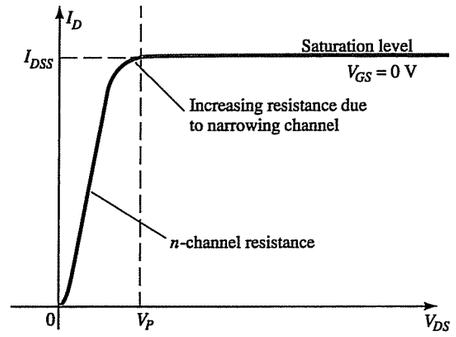


FIG. 6.7
I_D versus V_{DS} for $V_{GS} = 0$ V.

shown in Fig. 6.8, a condition referred to as *pinch-off* will result. The level of V_{DS} that establishes this condition is referred to as the *pinch-off voltage* and is denoted by V_P, as shown in Fig. 6.7. In actuality, the term *pinch-off* is a misnomer in that it suggests the current I_D is pinched off and drops to 0 A. As shown in Fig. 6.7, however, this is hardly the case—I_D maintains a saturation level defined as I_{DSS} in Fig. 6.7. In reality a very small channel still exists, with a current of very high density. The fact that I_D does not drop off at pinch-off and maintains the saturation level indicated in Fig. 6.7 is verified by the following fact: The absence of a drain current would remove the possibility of different potential levels through the *n*-channel material to establish the varying levels of reverse bias along the *p*–*n* junction. The result would be a loss of the depletion region distribution that caused pinch-off in the first place.

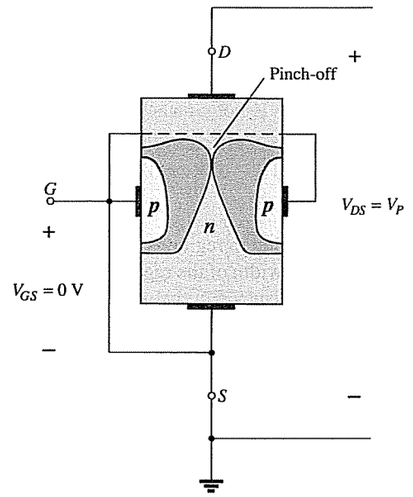


FIG. 6.8
Pinch-off ($V_{GS} = 0$ V, $V_{DS} = V_P$).

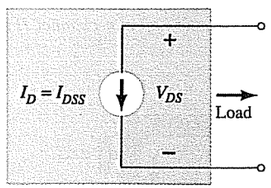


FIG. 6.9
Current source equivalent for $V_{GS} = 0$ V, $V_{DS} > V_P$.

As V_{DS} is increased beyond V_P, the region of close encounter between the two depletion regions increases in length along the channel, but the level of I_D remains essentially the same. In essence, therefore, once $V_{DS} > V_P$ the JFET has the characteristics of a current source. As shown in Fig. 6.9, the current is fixed at $I_D = I_{DSS}$, but the voltage V_{DS} (for levels $> V_P$) is determined by the applied load.

The choice of notation I_{DSS} is derived from the fact that it is the *d*rain-to-*s*ource current with a *s*hort-circuit connection from gate to source. As we continue to investigate the characteristics of the device we will find that:

I_{DSS} is the maximum drain current for a JFET and is defined by the conditions $V_{GS} = 0$ V and $V_{DS} > \lvert V_P \rvert$.

Note in Fig. 6.7 that $V_{GS} = 0$ V for the entire length of the curve. The next few paragraphs will describe how the characteristics of Fig. 6.7 are affected by changes in the level of V_{GS}.

$V_{GS} < 0$ V

The voltage from gate to source, denoted V_{GS}, is the controlling voltage of the JFET. Just as various curves for I_C versus V_{CE} were established for different levels of I_B for the BJT transistor, curves of I_D versus V_{DS} for various levels of V_{GS} can be developed for the JFET. For the *n*-channel device the controlling voltage V_{GS} is made more and more negative from its $V_{GS} = 0$ V level. In other words, the gate terminal will be set at lower and lower potential levels as compared to the source.

In Fig. 6.10 a negative voltage of -1 V is applied between the gate and source terminals for a low level of V_{DS}. The effect of the applied negative-bias V_{GS} is to establish depletion regions similar to those obtained with $V_{GS} = 0$ V, but at lower levels of V_{DS}. Therefore, the result of applying a negative bias to the gate is to reach the saturation level at a lower level of V_{DS}, as shown in Fig. 6.11 for $V_{GS} = -1$ V. The resulting saturation level for I_D has been reduced and in fact will continue to decrease as V_{GS} is made more and more negative. Note also in Fig. 6.11 how the pinch-off voltage continues to drop in a parabolic manner as V_{GS} becomes more and more negative. Eventually, V_{GS} when $V_{GS} = -V_P$ will be sufficiently negative to establish a saturation level that is essentially 0 mA, and for all practical purposes the device has been "turned off." In summary:

The level of V_{GS} that results in $I_D = 0$ mA is defined by $V_{GS} = V_P$, with V_P being a negative voltage for n-channel devices and a positive voltage for p-channel JFETs.

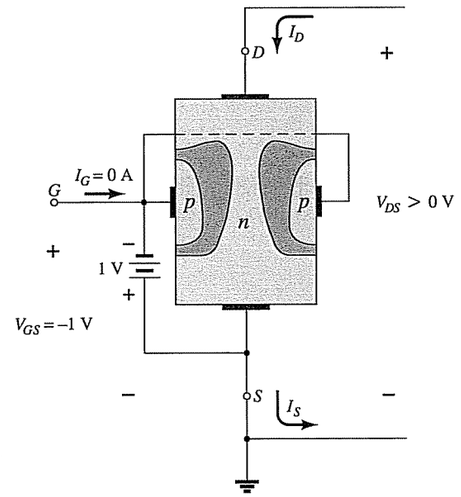


FIG. 6.10
Application of a negative voltage to the gate of a JFET.

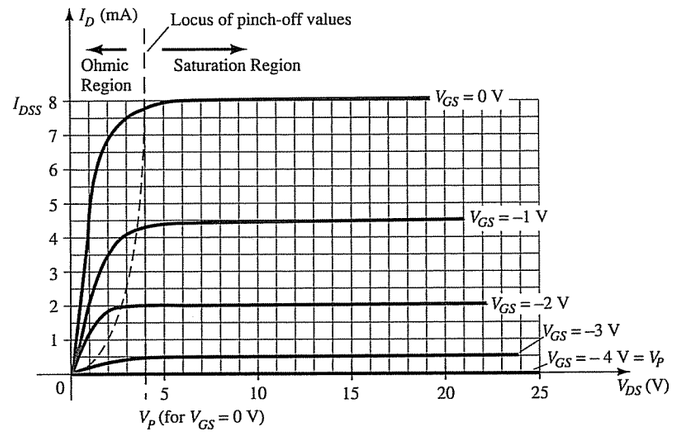


FIG. 6.11
n-Channel JFET characteristics with $I_{DSS} = 8$ mA and $V_P = -4$ V.

On most specification sheets the pinch-off voltage is specified as $V_{GS(off)}$ rather than V_P. A specification sheet will be reviewed later in the chapter when the primary elements of concern have been introduced. The region to the right of the pinch-off locus of Fig. 6.11 is the region typically employed in linear amplifiers (amplifiers with minimum distortion of the applied signal) and is commonly referred to as the *constant-current, saturation,* or *linear amplification region.*

Voltage-Controlled Resistor

The region to the left of the pinch-off locus of Fig. 6.11 is referred to as the *ohmic* or *voltage-controlled resistance region.* In this region the JFET can actually be employed as a variable resistor (possibly for an automatic gain control system) whose resistance is controlled by the applied gate-to-source voltage. Note in Fig. 6.11 that the slope of each curve and therefore the resistance of the device between drain and source for $V_{DS} < V_P$ are a function of the applied voltage V_{GS}. As V_{GS} becomes more and more negative, the slope of each curve becomes more and more horizontal, corresponding to an increasing resistance level. The following equation provides a good first approximation to the resistance level in terms of the applied voltage V_{GS}:

$$r_d = \frac{r_o}{(1 - V_{GS}/V_P)^2} \tag{6.1}$$

where r_o is the resistance with $V_{GS} = 0$ V and r_d is the resistance at a particular level of V_{GS}.

For an n-channel JFET with $r_o = 10\,\text{k}\Omega$ ($V_{GS} = 0\,\text{V}, V_P = -6\,\text{V}$), Eq. (6.1) results in $40\,\text{k}\Omega$ at $V_{GS} = -3$ V.

p-Channel Devices

The p-channel JFET is constructed in exactly the same manner as the n-channel device of Fig. 6.3 but with a reversal of the p- and n-type materials as shown in Fig. 6.12. The defined current directions are reversed, as are the actual polarities for the voltages V_{GS} and V_{DS}. For the p-channel device, the channel will be constricted by increasing positive voltages from gate to source and the double-subscript notation for V_{DS} will result in negative voltages for V_{DS} on the characteristics of Fig. 6.13, which has an I_{DSS} of 6 mA and a pinch-off voltage of $V_{GS} = +6$ V. Do not let the minus signs for V_{DS} confuse you. They simply indicate that the source is at a higher potential than the drain.

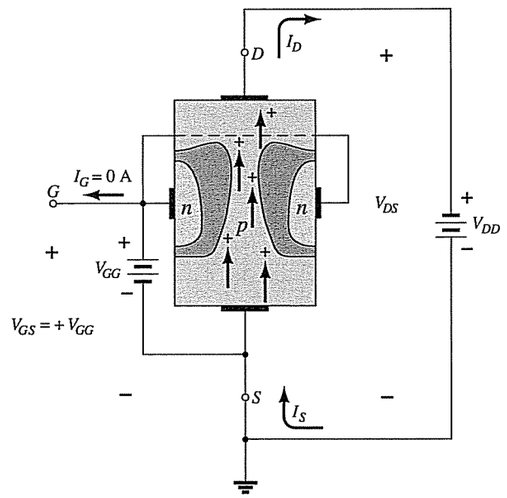


FIG. 6.12
p-Channel JFET.

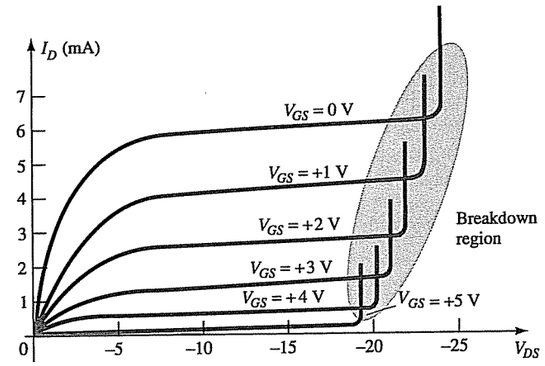


FIG. 6.13
p-Channel JFET characteristics with $I_{DSS} = 6$ mA and $V_P = +6$ V.

Note at high levels of V_{DS} that the curves suddenly rise to levels that seem unbounded. The vertical rise is an indication that breakdown has occurred and the current through the channel (in the same direction as normally encountered) is now limited solely by the external circuit. Although not appearing in Fig. 6.11 for the n-channel device, they do occur for the n-channel device if sufficient voltage is applied. This region can be avoided if the level of $V_{DS_{max}}$ is noted on the specification sheet and the design is such that the actual level of V_{DS} is less than this value for *all* values of V_{GS}.

Symbols

The graphic symbols for the n-channel and p-channel JFETs are provided in Fig. 6.14. Note that the arrow is pointing in for the n-channel device of Fig. 6.14a to represent the direction in which I_G would flow if the p–n junction were forward-biased. For the p-channel device (Fig. 6.14b) the only difference in the symbol is the direction of the arrow.

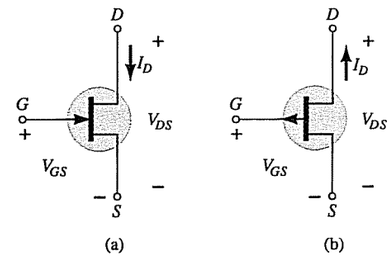


FIG. 6.14
JFET symbols: (a) n-channel; (b) p-channel.

Summary

A number of important parameters and relationships were introduced in this section. A few that will surface frequently in the analysis to follow in this chapter and the next for n-channel JFETs include the following:

The maximum current is defined as I_{DSS} and occurs when $V_{GS} = 0$ V and $V_{DS} \geq |V_P|$, as shown in Fig. 6.15a.

For gate-to-source voltages V_{GS} less than (more negative than) the pinch-off level, the drain current is 0 A ($I_D = 0$ A), as in Fig. 6.15b.

For all levels of V_{GS} between 0 V and the pinch-off level, the current I_D will range between I_{DSS} and 0 A, respectively, as in Fig. 6.15c.

A similar list can be developed for p-channel JFETs.

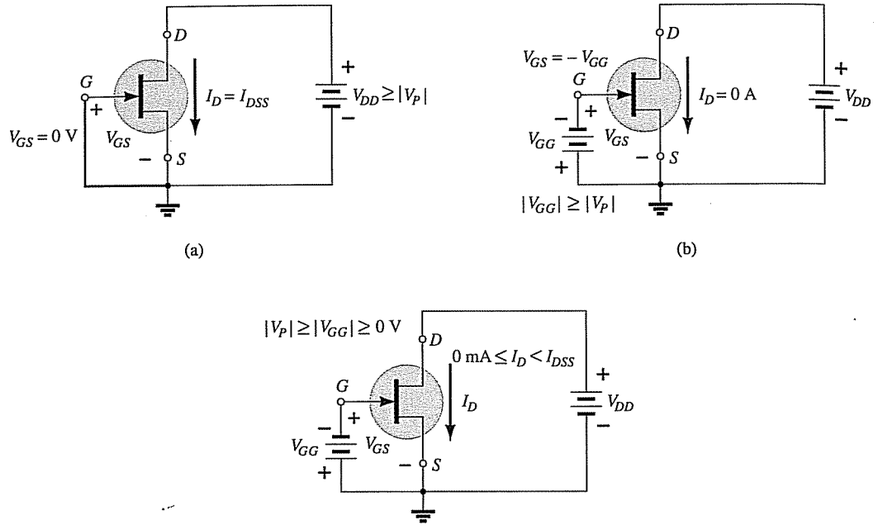


FIG. 6.15

(a) $V_{GS} = 0$ V, $I_D = I_{DSS}$; (b) cutoff ($I_D = 0$ A) V_{GS} less than the pinch-off level; (c) I_D is between 0 A and I_{DSS} for $V_{GS} \leq 0$ V and greater than the pinch-off level.

6.3 TRANSFER CHARACTERISTICS

Derivation

For the BJT transistor the output current I_C and the input controlling current I_B are related by beta, which was considered constant for the analysis to be performed. In equation form,

$$I_C = f(I_B) = \beta I_B \qquad \text{(6.2)}$$

(β: control variable; constant)

In Eq. (6.2) a linear relationship exists between I_C and I_B. Double the level of I_B and I_C will increase by a factor of two also.

Unfortunately, this linear relationship does not exist between the output and input quantities of a JFET. The relationship between I_D and V_{GS} is defined by *Shockley's equation* (see Fig. 6.16):

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \qquad \text{(6.3)}$$

(V_{GS}: control variable; I_{DSS}, V_P: constants)

The squared term in the equation results in a nonlinear relationship between I_D and V_{GS}, producing a curve that grows exponentially with decreasing magnitude of V_{GS}.

For the dc analysis to be performed in Chapter 7, a graphical rather than a mathematical approach will in general be more direct and easier to apply. The graphical approach, however, will require a plot of Eq. (6.3) to represent the device and a plot of the network equation relating the same variables. The solution is defined by the point of intersection of the two curves. It is important to keep in mind when applying the graphical approach that the device characteristics will be *unaffected* by the network in which the device is employed.



William Bradford Shockley (1910–1989), co-inventor of the first transistor and formulator of the "field-effect" theory employed in the development of the transistor and the FET.

Born: London, England;
PhD, Harvard, 1936;
Head, Transistor Physics Department, Bell Laboratories;
President, Shockley Transistor Corp.;
Poniatoff Professor of Engineering Science, Stanford University;
Nobel Prize in physics in 1956 with Walter Brattain and John Bardeen

FIG. 6.16

Dr. William Bradford Shockley. (Photo courtesy of AT&T Archives.)

The network equation may change along with the intersection between the two curves, but the transfer curve defined by Eq. (6.3) is unaffected. In general, therefore:

The transfer characteristics defined by Shockley's equation are unaffected by the network in which the device is employed.

The transfer curve can be obtained using Shockley's equation or from the output characteristics of Fig. 6.11. In Fig. 6.17 two graphs are provided, with the vertical scaling in milliamperes for each graph. One is a plot of I_D versus V_{DS}, whereas the other is I_D versus V_{GS}. Using the drain characteristics on the right of the "y" axis, we can draw a horizontal line from the saturation region of the curve denoted $V_{GS} = 0$ V to the I_D axis. The resulting current level for both graphs is I_{DSS}. The point of intersection on the I_D versus V_{GS} curve will be as shown since the vertical axis is defined as $V_{GS} = 0$ V.

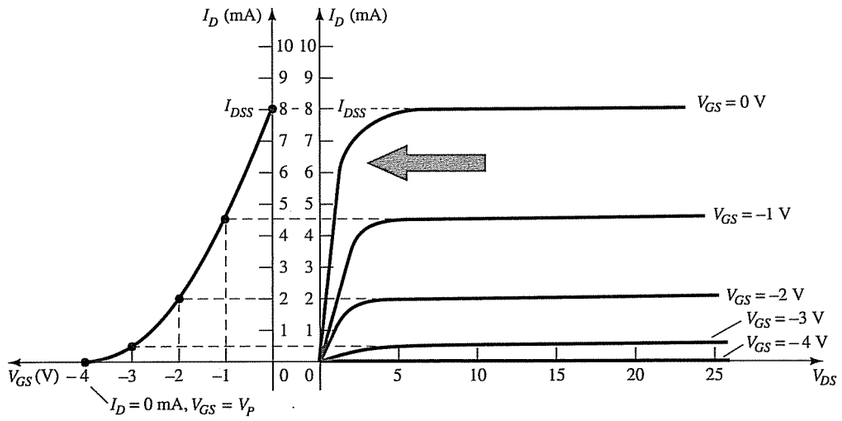


FIG. 6.17

Obtaining the transfer curve from the drain characteristics.

In review:

$$\boxed{\text{When } V_{GS} = 0\text{ V}, \quad I_D = I_{DSS}} \qquad \text{(6.4)}$$

When $V_{GS} = V_P = -4$ V, the drain current is 0 mA, defining another point on the transfer curve. That is:

$$\boxed{\text{When } V_{GS} = V_P, \quad I_D = 0\text{ mA}} \qquad \text{(6.5)}$$

Before continuing, it is important to realize that the drain characteristics relate one output (or drain) quantity to another output (or drain) quantity—both axes are defined by variables in the same region of the device characteristics. The transfer characteristics are a plot of an output (or drain) current versus an input-controlling quantity. There is therefore a direct "transfer" from input to output variables when employing the curve to the left of Fig. 6.17. If the relationship were linear, the plot of I_D versus V_{GS} would result in a straight line between I_{DSS} and V_P. However, a parabolic curve will result because the vertical spacing between steps of V_{GS} on the drain characteristics of Fig. 6.17 decreases noticeably as V_{GS} becomes more and more negative. Compare the spacing between $V_{GS} = 0$ V and $V_{GS} = -1$ V to that between $V_{GS} = -3$ V and pinch-off. The change in V_{GS} is the same, but the resulting change in I_D is quite different.

If a horizontal line is drawn from the $V_{GS} = -1$ V curve to the I_D axis and then extended to the other axis, another point on the transfer curve can be located. Note that $V_{GS} = -1$ V on the bottom axis of the transfer curve with $I_D = 4.5$ mA. Note in the definition of I_D at $V_{GS} = 0$ V and -1 V that the saturation levels of I_D are employed and the ohmic region ignored. Continuing with $V_{GS} = -2$ V and -3 V, we can complete the transfer curve. It is

the transfer curve of I_D versus V_{GS} that will receive extended use in the analysis of Chapter 7 and not the drain characteristics of Fig. 6.17. The next few paragraphs will introduce a quick, efficient method of plotting I_D versus V_{GS} given only the levels of I_{DSS} and V_P and Shockley's equation.

Applying Shockley's Equation

The transfer curve of Fig. 6.17 can also be obtained directly from Shockley's equation (6.3) given simply the values of I_{DSS} and V_P. The levels of I_{DSS} and V_P define the limits of the curve on both axes and leave only the necessity of finding a few intermediate plot points. The validity of Eq. (6.3) as a source of the transfer curve of Fig. 6.17 is best demonstrated by examining a few specific levels of one variable and finding the resulting level of the other as follows:

Substituting $V_{GS} = 0\,\text{V}$ gives

$$\text{Eq. (6.3):} \quad I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$
$$= I_{DSS}\left(1 - \frac{0}{V_P}\right)^2 = I_{DSS}(1 - 0)^2$$

and

$$\boxed{I_D = I_{DSS}|_{V_{GS}=0\,\text{V}}} \tag{6.6}$$

Substituting $V_{GS} = V_P$ yields

$$I_D = I_{DSS}\left(1 - \frac{V_P}{V_P}\right)^2$$
$$= I_{DSS}(1 - 1)^2 = I_{DSS}(0)$$

$$\boxed{I_D = 0\,\text{A}|_{V_{GS}=V_P}} \tag{6.7}$$

For the drain characteristics of Fig. 6.17, if we substitute $V_{GS} = -1\,\text{V}$,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$
$$= 8\,\text{mA}\left(1 - \frac{-1\,\text{V}}{-4\,\text{V}}\right)^2 = 8\,\text{mA}\left(1 - \frac{1}{4}\right)^2 = 8\,\text{mA}(0.75)^2$$
$$= 8\,\text{mA}(0.5625)$$
$$= \mathbf{4.5\,mA}$$

as shown in Fig. 6.17. Note the care taken with the negative signs for V_{GS} and V_P in the calculations above. The loss of one sign would result in a totally erroneous result.

It should be obvious from the above that given I_{DSS} and V_P (as is normally provided on specification sheets), the level of I_D can be found for any level of V_{GS}. Conversely, by using basic algebra we can obtain [from Eq. (6.3)] an equation for the resulting level of V_{GS} for a given level of I_D. The derivation is quite straightforward and results in

$$\boxed{V_{GS} = V_P\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)} \tag{6.8}$$

Let us test Eq. (6.8) by finding the level of V_{GS} that will result in a drain current of 4.5 mA for the device with the characteristics of Fig. 6.17. We find

$$V_{GS} = -4\,\text{V}\left(1 - \sqrt{\frac{4.5\,\text{mA}}{8\,\text{mA}}}\right)$$
$$= -4\,\text{V}(1 - \sqrt{0.5625}) = -4\,\text{V}(1 - 0.75)$$
$$= -4\,\text{V}(0.25)$$
$$= \mathbf{-1\,V}$$

as substituted in the above calculation and verified by Fig. 6.17.

Shorthand Method

Since the transfer curve must be plotted so frequently, it would be quite advantageous to have a shorthand method for plotting the curve in the quickest, most efficient manner while maintaining an acceptable degree of accuracy. The format of Eq. (6.3) is such that specific levels of V_{GS} will result in levels of I_D that can be memorized to provide the plot points needed to sketch the transfer curve. If we specify V_{GS} to be one-half the pinch-off value V_P, the resulting level of I_D will be the following, as determined by Shockley's equation:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$
$$= I_{DSS}\left(\frac{1 - V_P/2}{V_P}\right)^2 = I_{DSS}\left(1 - \frac{1}{2}\right)^2 = I_{DSS}(0.5)^2$$
$$= I_{DSS}(0.25)$$

and

$$\boxed{I_D = \frac{I_{DSS}}{4}\bigg|_{V_{GS}=V_P/2}} \tag{6.9}$$

Now it is important to realize that Eq. (6.9) is not for a particular level of V_P. It is a general equation for any level of V_P as long as $V_{GS} = V_P/2$. The result specifies that the drain current will always be one-fourth the saturation level I_{DSS} as long as the gate-to-source voltage is one-half the pinch-off value. Note the level of I_D for $V_{GS} = V_P/2 = -4\,\text{V}/2 = -2\,\text{V}$ in Fig. 6.17.

If we choose $I_D = I_{DSS}/2$ and substitute into Eq. (6.8), we find that

$$V_{GS} = V_P\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)$$
$$= V_P\left(1 - \sqrt{\frac{I_{DSS}/2}{I_{DSS}}}\right) = V_P(1 - \sqrt{0.5}) = V_P(0.293)$$

and

$$\boxed{V_{GS} \cong 0.3V_P|_{I_D=I_{DSS}/2}} \tag{6.10}$$

Additional points can be determined, but the transfer curve can be sketched to a satisfactory level of accuracy simply using the four plot points defined above and reviewed in Table 6.1. In fact, in the analysis of Chapter 7, a maximum of four plot points are used to sketch the transfer curves. On most occasions using just the plot point defined by $V_{GS} = V_P/2$ and the axis intersections at I_{DSS} and V_P will provide a curve accurate enough for most calculations.

TABLE 6.1
V_{GS} Versus I_D Using Shockley's Equation

V_{GS}	I_D
0	I_{DSS}
$0.3V_P$	$I_{DSS}/2$
$0.5V_P$	$I_{DSS}/4$
V_P	0 mA

EXAMPLE 6.1 Sketch the transfer curve defined by $I_{DSS} = 12\,\text{mA}$ and $V_P = -6\,\text{V}$.

Solution: Two plot points are defined by

$$I_{DSS} = \mathbf{12\,mA} \quad \text{and} \quad V_{GS} = \mathbf{0\,V}$$

and

$$I_D = \mathbf{0\,mA} \quad \text{and} \quad V_{GS} = V_P$$

At $V_{GS} = V_P/2 = -6\,\text{V}/2 = \mathbf{-3\,V}$ the drain current is determined by $I_D = I_{DSS}/4 = 12\,\text{mA}/4 = \mathbf{3\,mA}$. At $I_D = I_{DSS}/2 = 12\,\text{mA}/2 = \mathbf{6\,mA}$ the gate-to-source voltage is determined by $V_{GS} \cong 0.3V_P = 0.3(-6\,\text{V}) = \mathbf{-1.8\,V}$. All four plot points are well defined on Fig. 6.18 with the complete transfer curve.

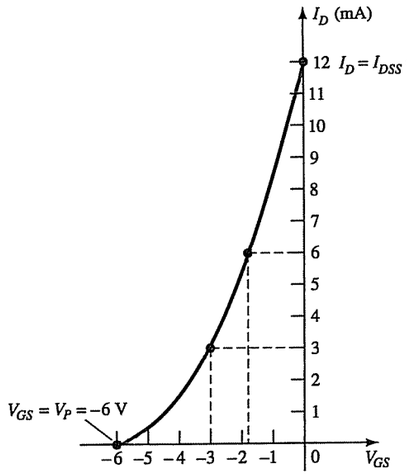


FIG. 6.18
Transfer curve for Example 6.1.

For *p*-channel devices Shockley's equation (6.3) can still be applied exactly as it appears. In this case, both V_P and V_{GS} will be positive and the curve will be the mirror image of the transfer curve obtained with an *n*-channel and the same limiting values.

EXAMPLE 6.2 Sketch the transfer curve for a *p*-channel device with $I_{DSS} = 4$ mA and $V_P = 3$ V.

Solution: At $V_{GS} = V_P/2 = 3\text{ V}/2 = \mathbf{1.5\ V}$, $I_D = I_{DSS}/4 = 4\text{ mA}/4 = \mathbf{1\ mA}$. At $I_D = I_{DSS}/2 = 4\text{ mA}/2 = \mathbf{2\ mA}$, $V_{GS} = 0.3V_P = 0.3(3\text{ V}) = \mathbf{0.9\ V}$. Both plot points appear in Fig. 6.19 along with the points defined by I_{DSS} and V_P.

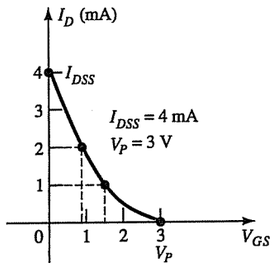


FIG. 6.19
Transfer curve for the p-channel device of Example 6.2.

Mathcad

Using Mathcad, we will now plot Shockley's equation using the **X-Y plot operator**. The plot operator can be selected using the **Graph = X-Y Plot** under the **Insert** option on the menu bar.

Once the plot is chosen, Mathcad will create a graph with placeholders on each axis as shown in Fig. 6.20. To plot Shockley's equation, first select the placeholder in the middle of the horizontal axis and enter the horizontal variable **VGS**. Then establish a range for **VGS** by first typing **VGS** followed by a colon and the range of values. The range of values is

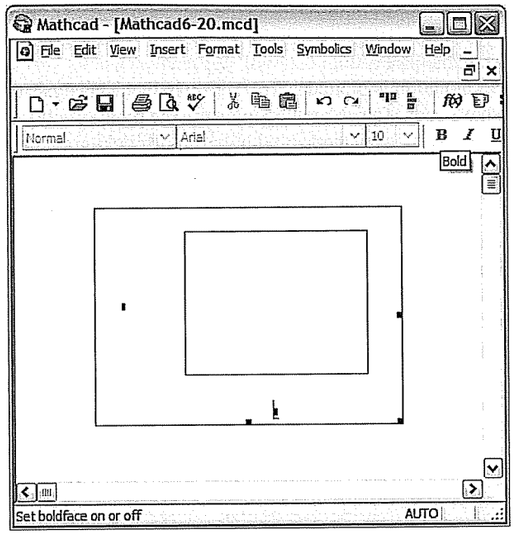


FIG. 6.20
The resulting graph when the plotting routing using Mathcad is initiated.

entered by first typing **0** (to represent **VGS = 0 V**) followed by a comma and the next value to be substituted in the equation for **ID**. This range also defines the interval between data points for the plot. If the **−0.1** were omitted, Mathcad would have used −1 as the interval, and the plot would have appeared with straight-line segments between data points rather than the smooth curve normally associated with Shockley's equation. For this example the chosen interval is **−0.1 V**; take careful note of the negative sign since **VGS** is getting more and more negative. Next the semicolon (**;**) key is chosen to tell the computer that a range is being defined. The computer response, however, is a double period, as shown in Fig. 6.21, followed by the last value of the range, the pinch-off voltage of **−4 V**.

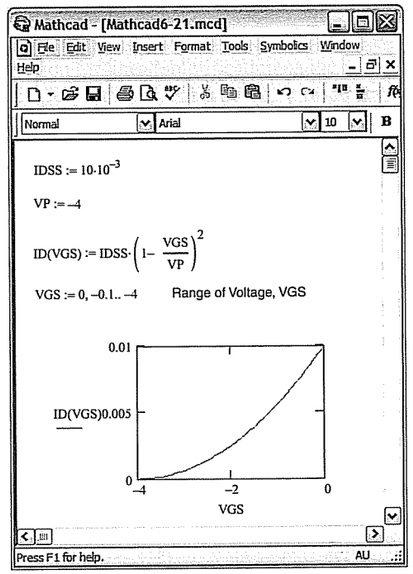


FIG. 6.21
Plotting Shockley's equation using Mathcad.

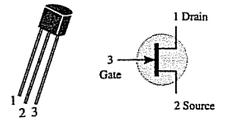
To define the quantity to be graphed, select the placeholder at the middle of the vertical axis and type **ID(VGS)**. The range is also defined as shown in Fig. 6.21. Click anywhere outside the graph, and the plot of Fig. 6.21 will appear.

Since Shockley's equation is plotted so frequently in the dc analysis of JFET networks, it is very useful to have such a quick method to obtain the plot. Simply change the value of **IDSS** or **VP**, and the new plot will appear with the single click of the mouse.

6.4 SPECIFICATION SHEETS (JFETs)

Although the general content of specification sheets may vary from the absolute minimum to an extensive display of graphs and charts, there are a few fundamental parameters that will be provided by all manufacturers. A few of the most important are discussed in the following paragraphs. The specification sheet for the 2N5457 *n*-channel JFET as provided by Motorola is provided as Fig. 6.22.

2N5457
CASE 29-04, STYLE 5
TO-92 (TO-226AA)



JFETs
GENERAL PURPOSE
N-CHANNEL—DEPLETION

Refer to 2N4220 for graphs.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	25	Vdc
Drain-Gate Voltage	V_{DG}	25	Vdc
Reverse Gate-Source Voltage	V_{GSR}	–25	Vdc
Gate Current	I_G	10	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	310 2.82	mW mW/°C
Junction Temperature Range	T_J	125	°C
Storage Channel Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Gate-Source Breakdown Voltage (I_G = –10 μAdc, V_{DS} = 0)		$V_{(BR)GSS}$	–25	–	–	Vdc
Gate Reverse Current (V_{GS} = –15 Vdc, V_{DS} = 0) (V_{GS} = –15 Vdc, V_{DS} = 0, T_A = 100°C)		I_{GSS}	– –	– –	–1.0 –200	nAdc
Gate Source Cutoff Voltage (V_{DS} = 15 Vdc, I_D = 10 nAdc)	2N5457	$V_{GS(off)}$	–0.5	–	–6.0	Vdc
Gate Source Voltage (V_{DS} = 15 Vdc, I_D = 100 μAdc)	2N5457	V_{GS}	–	–2.5	–	Vdc
ON CHARACTERISTICS						
Zero-Gate-Voltage Drain Current* (V_{DS} = 15 Vdc, V_{GS} = 0)	2N5457	I_{DSS}	1.0	3.0	5.0	mAdc
SMALL-SIGNAL CHARACTERISTICS						
Forward Transfer Admittance Common Source* (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)	2N5457	$\|y_{fs}\|$	1000	–	5000	μmhos
Output Admittance Common Source* (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)		$\|y_{os}\|$	–	10	50	μmhos
Input Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{iss}	–	4.5	7.0	pF
Reverse Transfer Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{rss}	–	1.5	3.0	pF

*Pulse Test: Pulse Width ≤ 630 ms; Duty Cycle ≤ 10%

FIG. 6.22
2N5457 Motorola n-channel JFET.

Maximum Ratings

The maximum rating list usually appears at the beginning of the specification sheet, with the maximum voltages between specific terminals, maximum current levels, and the maximum power dissipation level of the device. The specified maximum levels for V_{DS} and V_{DG} must not be exceeded at any point in the design operation of the device. The applied source V_{DD} can exceed these levels, but the actual level of voltage between these terminals must never exceed the level specified. Any good design will try to avoid these levels by a good margin of safety. The term *reverse* in V_{GSR} defines the maximum voltage with the source positive with respect to the gate (as normally biased for an *n*-channel device) before breakdown will occur. On some specification sheets it is referred to as BV_{DSS}—the *b*reakdown *v*oltage with the *d*rain-*s*ource *s*horted (V_{DS} = 0 V). Although normally designed to operate with I_G = 0 mA, if *forced* to accept a gate current, it could withstand 10 mA before damage would occur. The total device dissipation at 25°C (room temperature) is the maximum power the device can dissipate under normal operating conditions and is defined by

$$P_D = V_{DS}I_D \tag{6.11}$$

Note the similarity in format with the maximum power dissipation equation for the BJT transistor.

The derating factor is discussed in detail in Chapter 3, but for the moment recognize that the 2.82 mW/°C rating reveals that the dissipation rating *decreases* by 2.82 mW for each *increase* in temperature of 1°C above 25°C.

Electrical Characteristics

The electrical characteristics include the level of V_P in the "off" characteristics and I_{DSS} in the "on" characteristics. In this case $V_P = V_{GS(off)}$ has a range from −0.5 V to −6.0 V and I_{DSS} from 1 mA to 5 mA. The fact that both will vary from device to device with the same nameplate identification must be considered in the design process. The other quantities are defined under conditions appearing in parentheses. The small-signal characteristics are discussed in Chapter 8.

Case Construction and Terminal Identification

This particular JFET has the appearance provided on the specification sheet of Fig. 6.22. The terminal identification is also provided directly under the figure. JFETs are also available in top-hat containers, as shown in Fig. 6.23 with its terminal identification.

Operating Region

The specification sheet and the curve defined by the pinch-off levels at each level of V_{GS} define the region of operation for linear amplification on the drain characteristics as shown in Fig. 6.24. The ohmic region defines the minimum permissible values of V_{DS} at each level of V_{GS}, and $V_{DS_{max}}$ specifies the maximum value for this parameter. The saturation current

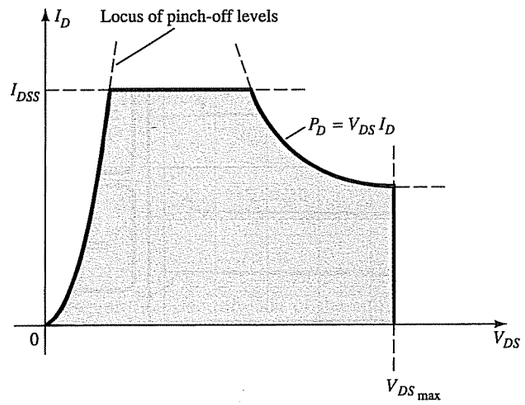
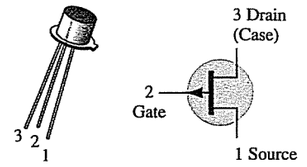


FIG. 6.24
Normal operating region for linear amplifier design.

2N2844
CASE 22-03, STYLE 12
TO-18 (TO-206AA)



JFETs
GENERAL PURPOSE
P-CHANNEL

FIG. 6.23
Top-hat container and terminal identification for a p-channel JFET.

I_{DSS} is the maximum drain current, and the maximum power dissipation level defines the curve drawn in the same manner as described for BJT transistors. The resulting shaded region is the normal operating region for amplifier design.

6.5 INSTRUMENTATION

Recall from Chapter 3 that hand-held instruments are available to measure the level of β_{dc} for the BJT transistor. Similar instrumentation is not available to measure the levels of I_{DSS} and V_P. However, the curve tracer introduced for the BJT transistor can also display the drain characteristics of the JFET transistor through a proper setting of the various controls. The vertical scale (in milliamperes) and the horizontal scale (in volts) have been set to provide a full display of the characteristics, as shown in Fig. 6.25. For the JFET of Fig. 6.25, each vertical division (in centimeters) reflects a 1-mA change in I_D, whereas each horizontal division has a value of 1 V. The step voltage is 500 mV/step (0.5 V/step), revealing that the top curve is defined by $V_{GS} = 0$ V and the next curve down is -0.5 V for the *n*-channel device. Using the same step voltage, we see the next curve is -1 V, then -1.5 V, and finally -2 V. By drawing a line from the top curve over to the I_D axis, we can estimate the level of I_{DSS} to be about 9 mA. The level of V_P can be estimated by noting the V_{GS} value of the bottom curve and taking into account the shrinking distance between curves as V_{GS} becomes more and more negative. In this case, V_P is certainly more negative than -2 V, and perhaps V_P is close to -2.5 V. However, keep in mind that the V_{GS} curves contract very quickly as they approach the cutoff condition, and perhaps $V_P = -3$ V is a better choice. It should also be noted that the step control is set for a five-step display, limiting the displayed curves to $V_{GS} = 0, -0.5, -1, -1.5$, and -2 V. If the step control had been increased to 10, the voltage per step could be reduced to 250 mV = 0.25 V and the curve for $V_{GS} = -2.25$ V would have been included as well as an additional curve between each step of Fig. 6.25. The $V_{GS} = -2.25$ V curve would reveal how quickly the curves are closing in on each other for the same step voltage. Fortunately, the level of V_P can be estimated to a reasonable degree of accuracy simply by applying a condition appearing in Table 6.1. That is, when $I_D = I_{DSS}/2$, then $V_{GS} = 0.3V_P$. For the characteristics of Fig. 6.25, $I_D = I_{DSS}/2 = 9\text{ mA}/2 = 4.5$ mA, and, as visible from Fig. 6.25, the corresponding level of V_{GS} is about -0.9 V. Using this information, we find that $V_P = V_{GS}/0.3 = -0.9\text{ V}/0.3 = -3$ V, which will be our choice for this device. Using this value, we find that at $V_{GS} = -2$ V,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$
$$= 9\text{ mA}\left(1 - \frac{-2\text{ V}}{-3\text{ V}}\right)^2$$
$$\cong 1\text{ mA}$$

as supported by Fig. 6.25.

At $V_{GS} = -2.5$ V, Shockley's equation results in $I_D = 0.25$ mA, with $V_P = -3$ V, clearly revealing how quickly the curves contract near V_P. The importance of the parameter g_m and how it is determined from the characteristics of Fig. 6.25 are described in Chapter 8 when small-signal ac conditions are examined.

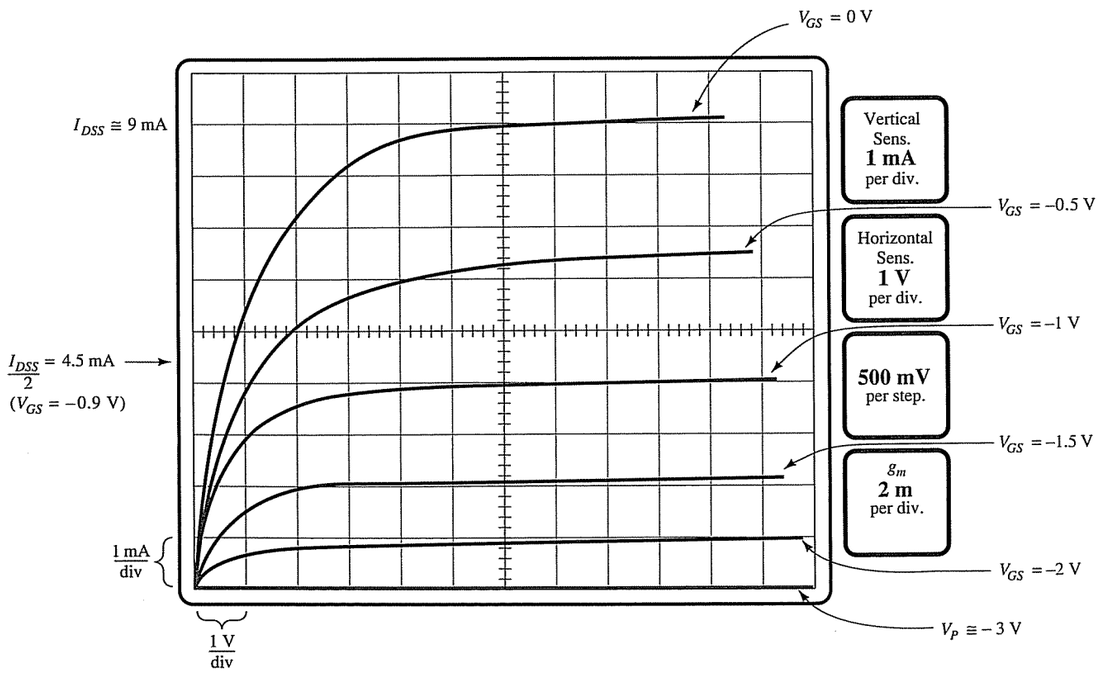


FIG. 6.25
Drain characteristics for a 2N4416 JFET transistor as displayed on a curve tracer.

6.6 IMPORTANT RELATIONSHIPS

A number of important equations and operating characteristics have been introduced in the last few sections that are of particular importance for the analysis to follow for the dc and ac configurations. To isolate and emphasize their importance, they are repeated below next to corresponding equations for the BJT transistor. The JFET equations are defined for the configuration of Fig. 6.26a whereas the BJT equations relate to Fig. 6.26b.

JFET		***BJT***
$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$	$\Leftrightarrow$	$I_C = \beta I_B$
$I_D = I_S$	$\Leftrightarrow$	$I_C \cong I_E$
$I_G \cong 0$ A	$\Leftrightarrow$	$V_{BE} \cong 0.7$ V

(6.12)

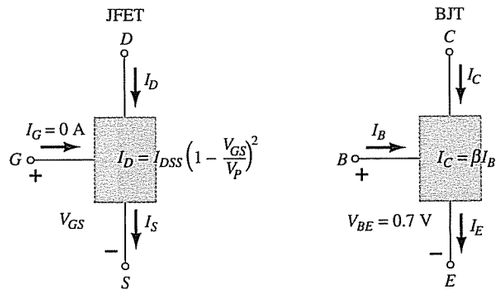


FIG. 6.26
(a) JFET versus (b) BJT.

A clear understanding of the effect of each of the equations above is sufficient background to approach the most complex of dc configurations. Recall that $V_{BE} = 0.7$ V was often the key to initiating an analysis of a BJT configuration. Similarly, the condition $I_G = 0$ A is often the starting point for the analysis of a JFET configuration. For the BJT configuration, I_B is normally the first parameter to be determined. For the JFET, it is normally V_{GS}. The number of similarities between the analysis of BJT and JFET dc configurations will become quite apparent in Chapter 7.

6.7 DEPLETION-TYPE MOSFET

As noted in the introduction, there are three types of FETs: JFETs, MOSFETs, and MESFETs. MOSFETs are further broken down into *depletion type* and *enhancement type*. The terms *depletion* and *enhancement* define their basic mode of operation; the name MOSFET stands for *m*etal–*o*xide–*s*emiconductor *f*ield-*e*ffect *t*ransistor. Since there are differences in the characteristics and operation of different types of MOSFET, they are covered in separate sections. In this section we examine the depletion-type MOSFET, which has characteristics similar to those of a JFET between cutoff and saturation at I_{DSS}, and also has the added feature of characteristics that extend into the region of opposite polarity for V_{GS}.

Basic Construction

The basic construction of the *n*-channel depletion-type MOSFET is provided in Fig. 6.27. A slab of *p*-type material is formed from a silicon base and is referred to as the *substrate*. It is the foundation on which the device is constructed. In some cases the substrate is internally connected to the source terminal. However, many discrete devices provide an additional terminal labeled *SS*, resulting in a four-terminal device, such as that in Fig. 6.27. The source and drain terminals are connected through metallic contacts to *n*-doped regions linked by an *n*-channel as shown in the figure. The gate is also connected to a metal contact surface but remains insulated from the *n*-channel by a very thin silicon dioxide (SiO_2) layer. SiO_2 is a type of insulator referred to as a *dielectric*, which sets up opposing (as indicated by the prefix *di-*) electric fields within the dielectric when exposed to an externally applied field. The fact that the SiO_2 layer is an insulating layer means that:

There is no direct electrical connection between the gate terminal and the channel of a MOSFET.

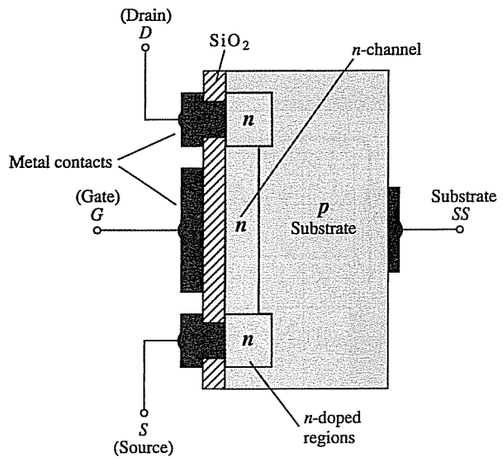


FIG. 6.27
n-Channel depletion-type MOSFET.

In addition:

It is the insulating layer of SiO_2 in the MOSFET construction that accounts for the very desirable high input impedance of the device.

In fact, the input resistance of a MOSFET is often that of a typical JFET, even though the input impedance of most JFETs is sufficiently high for most applications. Because of the very high input impedance, the gate current I_G is essentially 0 A for dc-biased configurations.

The reason for the label metal–oxide–semiconductor FET is now fairly obvious: *metal* for the drain, source, and gate connections to the proper surface—in particular, the gate terminal and the control to be offered by the surface area of the contact; *oxide* for the silicon dioxide insulating layer; and *semiconductor* for the basic structure on which the *n*- and *p*-type regions are diffused. The insulating layer between the gate and the channel has resulted in another name for the device: *insulated-gate FET*, or *IGFET*, although this label is used less and less in the literature.

Basic Operation and Characteristics

In Fig. 6.28 the gate-to-source voltage is set to 0 V by the direct connection from one terminal to the other, and a voltage V_{DS} is applied across the drain-to-source terminals. The result is an attraction for the positive potential at the drain by the *free* electrons of the *n*-channel and a current similar to that established through the channel of the JFET. In fact, the resulting current with $V_{GS} = 0$ V continues to be labeled I_{DSS}, as shown in Fig. 6.29.

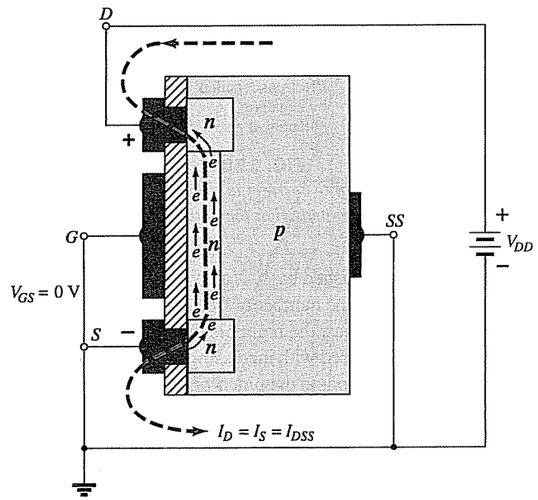


FIG. 6.28
n-Channel depletion-type MOSFET with $V_{GS} = 0$ V and applied voltage V_{DD}.

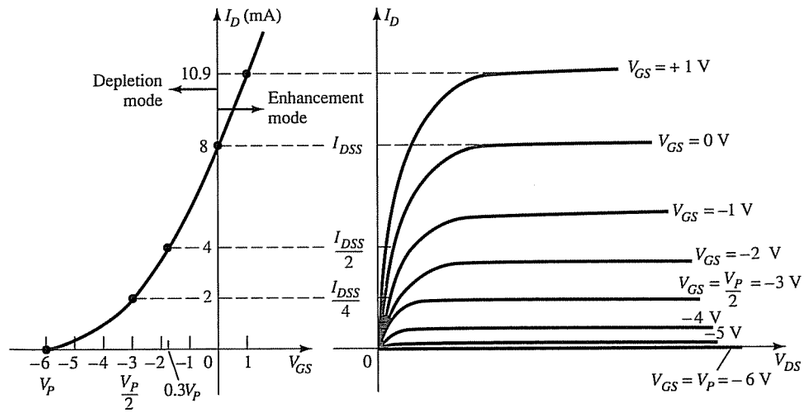


FIG. 6.29
Drain and transfer characteristics for an n-channel depletion-type MOSFET.

In Fig. 6.30, V_{GS} is set at a negative voltage such as −1 V. The negative potential at the gate will tend to pressure electrons toward the *p*-type substrate (like charges repel) and attract holes from the *p*-type substrate (opposite charges attract) as shown in Fig. 6.30. Depending on the

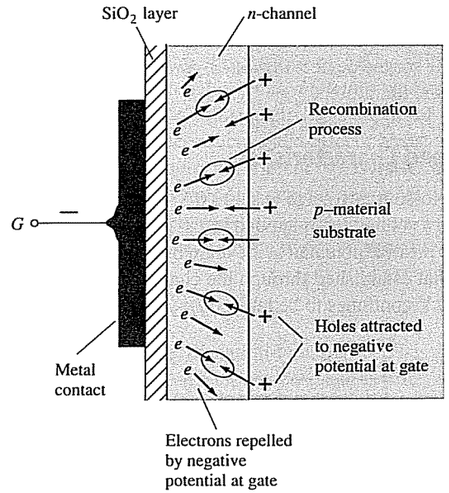


FIG. 6.30
Reduction in free carriers in a channel due to a negative potential at the gate terminal.

magnitude of the negative bias established by V_{GS}, a level of recombination between electrons and holes will occur that will reduce the number of free electrons in the *n*-channel available for conduction. The more negative the bias, the higher is the rate of recombination. The resulting level of drain current is therefore reduced with increasing negative bias for V_{GS}, as shown in Fig. 6.29 for $V_{GS} = -1$ V, -2 V, and so on, to the pinch-off level of -6 V. The resulting levels of drain current and the plotting of the transfer curve proceed exactly as described for the JFET.

For positive values of V_{GS}, the positive gate will draw additional electrons (free carriers) from the *p*-type substrate due to the reverse leakage current and establish new carriers through the collisions resulting between accelerating particles. As the gate-to-source voltage continues to increase in the positive direction, Fig. 6.29 reveals that the drain current will increase at a rapid rate for the reasons listed above. The vertical spacing between the $V_{GS} = 0$ V and $V_{GS} = +1$ V curves of Fig. 6.29 is a clear indication of how much the current has increased for the 1-V change in V_{GS}. Due to the rapid rise, the user must be aware of the maximum drain current rating since it could be exceeded with a positive gate voltage. That is, for the device of Fig. 6.29, the application of a voltage $V_{GS} = +4$ V would result in a drain current of 22.2 mA, which could possibly exceed the maximum rating (current or power) for the device. As revealed above, the application of a positive gate-to-source voltage has "enhanced" the level of free carriers in the channel compared to that encountered with $V_{GS} = 0$ V. For this reason the region of positive gate voltages on the drain or transfer characteristics is often referred to as the *enhancement region*, with the region between cutoff and the saturation level of I_{DSS} referred to as the *depletion region.*

It is particularly interesting and helpful that Shockley's equation will continue to be applicable for the depletion-type MOSFET characteristics in both the depletion and enhancement regions. For both regions, it is simply necessary that the proper sign be included with V_{GS} in the equation and the sign be carefully monitored in the mathematical operations.

EXAMPLE 6.3 Sketch the transfer characteristics for an *n*-channel depletion-type MOSFET with $I_{DSS} = 10$ mA and $V_P = -4$ V.

Solution:

$$\text{At } V_{GS} = 0 \text{ V}, \quad I_D = I_{DSS} = 10 \text{ mA}$$

$$V_{GS} = V_P = -4 \text{ V}, \quad I_D = 0 \text{ mA}$$

$$V_{GS} = \frac{V_P}{2} = \frac{-4 \text{ V}}{2} = -2 \text{ V}, \quad I_D = \frac{I_{DSS}}{4} = \frac{10 \text{ mA}}{4} = 2.5 \text{ mA}$$

and at $I_D = \dfrac{I_{DSS}}{2}$,

$$V_{GS} = 0.3V_P = 0.3(-4 \text{ V}) = -1.2 \text{ V}$$

all of which appear in Fig. 6.31.

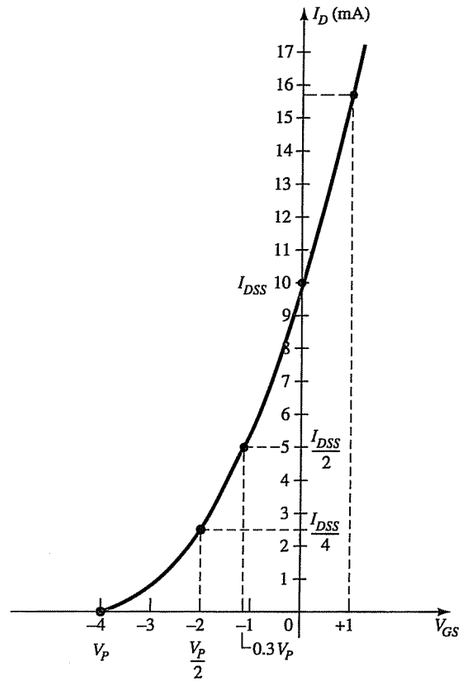


FIG. 6.31
Transfer characteristics for an n-channel depletion-type MOSFET with $I_{DSS} = 10$ mA and $V_P = -4$ V.

Before plotting the positive region of V_{GS}, keep in mind that I_D increases very rapidly with increasing positive values of V_{GS}. In other words, be conservative with the choice of values to be substituted into Shockley's equation. In this case, we try $+1$ V as follows:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= (10 \text{ mA})\left(1 - \frac{+1 \text{ V}}{-4 \text{ V}}\right)^2 = (10 \text{ mA})\,(1 + 0.25)^2 = (10 \text{ mA})\,(1.5625)$$

$$\cong 15.63 \text{ mA}$$

which is sufficiently high to finish the plot.

p-Channel Depletion-Type MOSFET

The construction of a *p*-channel depletion-type MOSFET is exactly the reverse of that appearing in Fig. 6.27. That is, there is now an *n*-type substrate and a *p*-type channel, as shown in Fig. 6.32a. The terminals remain as identified, but all the voltage polarities and the current directions are reversed, as shown in the same figure. The drain characteristics would appear exactly as in Fig. 6.29, but with V_{DS} having negative values, I_D having positive values as indicated (since the defined direction is now reversed), and V_{GS} having the opposite polarities as shown in Fig. 6.32c. The reversal in V_{GS} will result in a mirror image (about the I_D axis) for the transfer characteristics as shown in Fig. 6.32b. In other words,

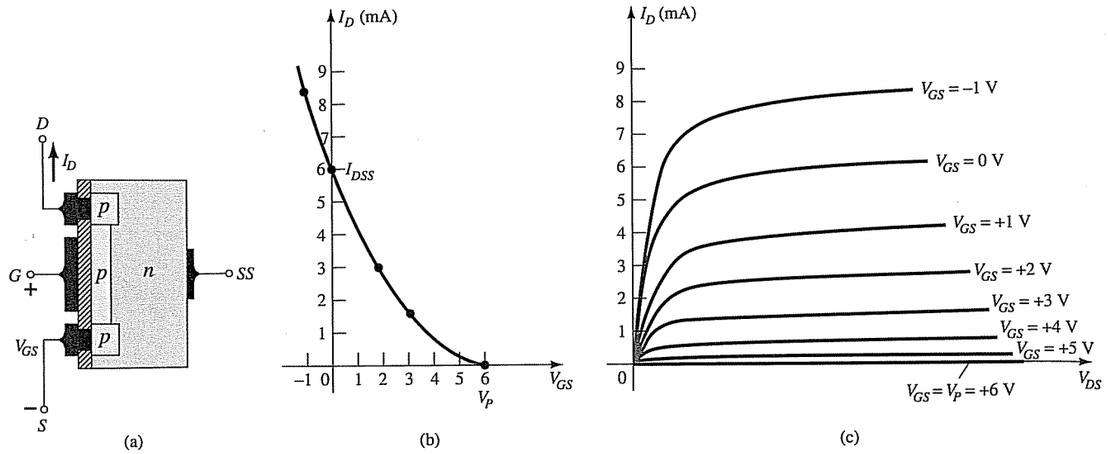


FIG. 6.32
p-Channel depletion-type MOSFET with $I_{DSS} = 6$ mA and $V_P = +6$ V.

the drain current will increase from cutoff at $V_{GS} = V_P$ in the positive V_{GS} region to I_{DSS} and then continue to increase for increasingly negative values of V_{GS}. Shockley's equation is still applicable and requires simply placing the correct sign for both V_{GS} and V_P in the equation.

Symbols, Specification Sheets, and Case Construction

The graphic symbols for an *n*- and *p*-channel depletion-type MOSFET are provided in Fig. 6.33. Note how the symbols chosen try to reflect the actual construction of the device. The lack of a direct connection (due to the gate insulation) between the gate and the channel is represented by a space between the gate and the other terminals of the symbol. The vertical line representing the channel is connected between the drain and the source and is "supported" by the substrate. Two symbols are provided for each type of channel to reflect the fact that in some cases the substrate is externally available, whereas in others it is not. For most of the analysis to follow in Chapter 7, the substrate and the source will be connected and the lower symbols will be employed.

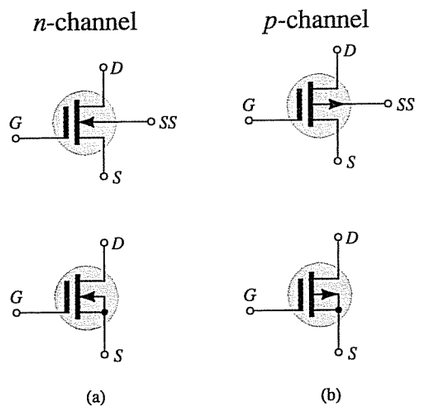
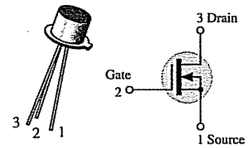


FIG. 6.33
Graphic symbols for (a) n-channel depletion-type MOSFETs and (b) p-channel depletion-type MOSFETs.

The device appearing in Fig. 6.34 has three terminals, with the terminal identification appearing in the same figure. The specification sheet for a depletion-type MOSFET is similar to that of a JFET. The levels of V_P and I_{DSS} are provided along with a list of maximum values and typical "on" and "off" characteristics. In addition, however, since I_D can extend beyond the I_{DSS} level, another point is normally provided that reflects a typical value of I_D for some positive voltage (for an *n*-channel device). For the unit of Fig. 6.34, I_D is specified as $I_{D(on)} = 9$ mA dc, with $V_{DS} = 10$ V and $V_{GS} = 3.5$ V.

2N3797

CASE 22-03, STYLE 2
TO-18 (TO-206AA)



MOSFETs
LOW POWER AUDIO

N-CHANNEL – DEPLETION

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage 2N3797	V_{DS}	20	Vdc
Gate–Source Voltage	V_{GS}	±10	Vdc
Drain Current	I_D	20	mAdc
Total Device Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	200 1.14	mW mW/°C
Junction Temperature Range	T_J	+175	°C
Storage Channel Temperature Range	T_{stg}	−65 to +200	°C

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain Source Breakdown Voltage ($V_{GS} = -7.0$ V, $I_D = 5.0$ μA)	2N3797	$V_{(BR)DSX}$	20	25	–	Vdc
Gate Reverse Current (1) ($V_{GS} = -10$ V, $V_{DS} = 0$) ($V_{GS} = -10$ V, $V_{DS} = 0$, $T_A = 150°C$)		I_{GSS}	– –	– –	1.0 200	pAdc
Gate Source Cutoff Voltage ($I_D = 2.0$ μA, $V_{DS} = 10$ V)	2N3797	$V_{GS(off)}$	–	−5.0	−7.0	Vdc
Drain-Gate Reverse Current (1) ($V_{DG} = 10$ V, $I_S = 0$)		I_{DGO}	–	–	1.0	pAdc
ON CHARACTERISTICS						
Zero-Gate-Voltage Drain Current ($V_{DS} = 10$ V, $V_{GS} = 0$)	2N3797	I_{DSS}	2.0	2.9	6.0	mAdc
On-State Drain Current ($V_{DS} = 10$ V, $V_{GS} = +3.5$ V)	2N3797	$I_{D(on)}$	9.0	14	18	mAdc
SMALL-SIGNAL CHARACTERISTICS						
Forward Transfer Admittance ($V_{DS} = 10$ V, $V_{GS} = 0$, f = 1.0 kHz)	2N3797	$\lvert y_{fs} \rvert$	1500	2300	3000	μmhos
($V_{DS} = 10$ V, $V_{GS} = 0$, f = 1.0 MHz)	2N3797		1500	–	–	
Output Admittance ($I_{DS} = 10$ V, $V_{GS} = 0$, f = 1.0 kHz)	2N3797	$\lvert y_{os} \rvert$	–	27	60	μmhos
Input Capacitance ($V_{DS} = 10$ V, $V_{GS} = 0$, f = 1.0 MHz)	2N3797	C_{iss}	–	6.0	8.0	pF
Reverse Transfer Capacitance ($V_{DS} = 10$ V, $V_{GS} = 0$, f = 1.0 MHz)		C_{rss}	–	0.5	0.8	pF
FUNCTIONAL CHARACTERISTICS						
Noise Figure ($V_{DS} = 10$ V, $V_{GS} = 0$, f = 1.0 kHz, $R_S = 3$ megohms)		NF	–	3.8	–	dB

(1) This value of current includes both the FET leakage current as well as the leakage current associated with the test socket and fixture when measured under best attainable conditions.

FIG. 6.34
2N3797 Motorola n-channel depletion-type MOSFET.

6.8 ENHANCEMENT-TYPE MOSFET

Although there are some similarities in construction and mode of operation between depletion-type and enhancement-type MOSFETs, the characteristics of the enhancement-type MOSFET are quite different from anything obtained thus far. The transfer curve is not defined by Shockley's equation, and the drain current is now cut off until the gate-to-source voltage reaches a specific magnitude. In particular, current control in an *n*-channel device is now effected by a positive gate-to-source voltage rather than the range of negative voltages encountered for *n*-channel JFETs and *n*-channel depletion-type MOSFETs.

Basic Construction

The basic construction of the *n*-channel enhancement-type MOSFET is provided in Fig. 6.35. A slab of *p*-type material is formed from a silicon base and is again referred to as the substrate. As with the depletion-type MOSFET, the substrate is sometimes internally connected to the source terminal, whereas in other cases a fourth lead is made available for external control of its potential level. The source and drain terminals are again connected through metallic contacts to *n*-doped regions, but note in Fig. 6.35 the absence of a channel between the two *n*-doped regions. This is the primary difference between the construction of depletion-type and enhancement-type MOSFETs—the absence of a channel as a constructed component of the device. The SiO_2 layer is still present to isolate the gate metallic platform from the region between the drain and source, but now it is simply separated from a section of the *p*-type material. In summary, therefore, the construction of an enhancement-type MOSFET is quite similar to that of the depletion-type MOSFET, except for the absence of a channel between the drain and source terminals.

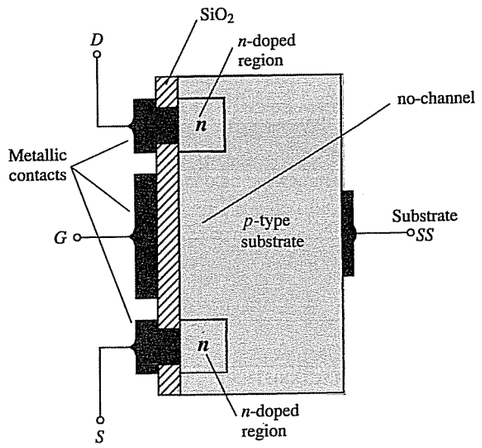


FIG. 6.35
n-Channel enhancement-type MOSFET.

Basic Operation and Characteristics

If V_{GS} is set at 0 V and a voltage applied between the drain and the source of the device of Fig. 6.35, the absence of an *n*-channel (with its generous number of free carriers) will result in a current of effectively 0 A—quite different from the depletion-type MOSFET and JFET, where $I_D = I_{DSS}$. It is not sufficient to have a large accumulation of carriers (electrons) at the drain and the source (due to the *n*-doped regions) if a path fails to exist between the two. With V_{DS} some positive voltage, V_{GS} at 0 V, and terminal *SS* directly connected to the source, there are in fact two reverse-biased *p*–*n* junctions between the *n*-doped regions and the *p*-substrate to oppose any significant flow between drain and source.

In Fig. 6.36, both V_{DS} and V_{GS} have been set at some positive voltage greater than 0 V, establishing the drain and the gate at a positive potential with respect to the source. The

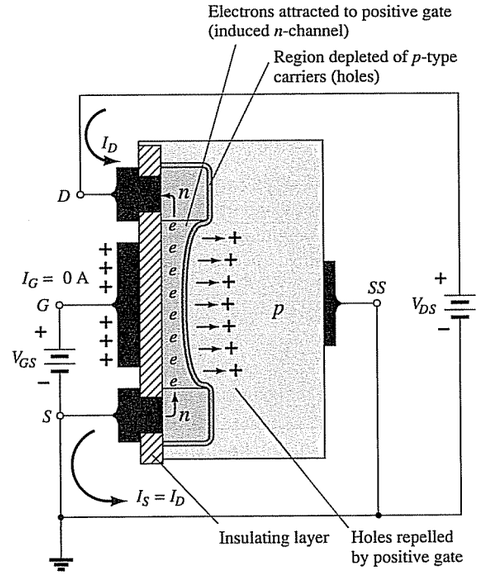


FIG. 6.36
Channel formation in the n-channel enhancement-type MOSFET.

positive potential at the gate will pressure the holes (since like charges repel) in the *p*-substrate along the edge of the SiO_2 layer to leave the area and enter deeper regions of the *p*-substrate, as shown in the figure. The result is a depletion region near the SiO_2 insulating layer void of holes. However, the electrons in the *p*-substrate (the minority carriers of the material) will be attracted to the positive gate and accumulate in the region near the surface of the SiO_2 layer. The SiO_2 layer and its insulating qualities will prevent the negative carriers from being absorbed at the gate terminal. As V_{GS} increases in magnitude, the concentration of electrons near the SiO_2 surface increases until eventually the induced *n*-type region can support a measurable flow between drain and source. The level of V_{GS} that results in the significant increase in drain current is called the *threshold voltage* and is given the symbol V_T. On specification sheets it is referred to as $V_{GS(Th)}$, although V_T is less unwieldy and will be used in the analysis to follow. Since the channel is nonexistent with $V_{GS} = 0$ V and "enhanced" by the application of a positive gate-to-source voltage, this type of MOSFET is called an *enhancement-type MOSFET.* Both depletion- and enhancement-type MOSFETs have enhancement-type regions, but the label was applied to the latter since it is its only mode of operation.

As V_{GS} is increased beyond the threshold level, the density of free carriers in the induced channel will increase, resulting in an increased level of drain current. However, if we hold V_{GS} constant and increase the level of V_{DS}, the drain current will eventually reach a saturation level as occurred for the JFET and depletion-type MOSFET. The leveling off of I_D is due to a pinching-off process depicted by the narrower channel at the drain end of the induced channel as shown in Fig. 6.37. Applying Kirchhoff's voltage law to the terminal voltages of the MOSFET of Fig. 6.37, we find that

$$\boxed{V_{DG} = V_{DS} - V_{GS}} \qquad \textbf{(6.13)}$$

If V_{GS} is held fixed at some value such as 8 V and V_{DS} is increased from 2 V to 5 V, the voltage V_{DG} [by Eq. (6.13)] will drop from −6 V to −3 V and the gate will become less and less positive with respect to the drain. This reduction in gate-to-drain voltage will in turn reduce the attractive forces for free carriers (electrons) in this region of the induced channel, causing a reduction in the effective channel width. Eventually, the channel will be reduced to the point of pinch-off and a saturation condition will be established as described

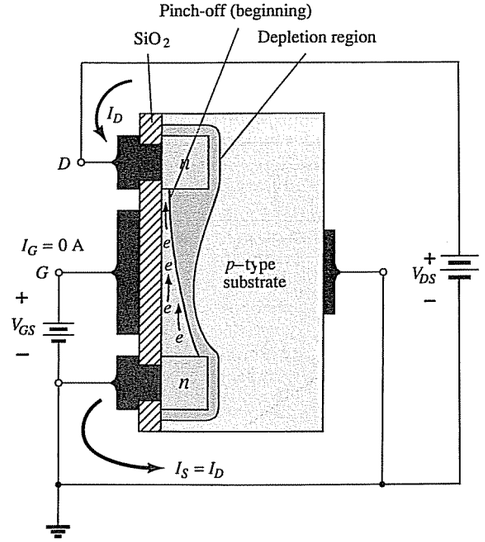


FIG. 6.37
Change in channel and depletion region with increasing level of V_{DS} for a fixed value of V_{GS}.

earlier for the JFET and depletion-type MOSFET. In other words, any further increase in V_{DS} at the fixed value of V_{GS} will not affect the saturation level of I_D until breakdown conditions are encountered.

The drain characteristics of Fig. 6.38 reveal that for the device of Fig. 6.37 with $V_{GS} = 8$ V, saturation occurs at a level of $V_{DS} = 6$ V. In fact, the saturation level for V_{DS} is related to the level of applied V_{GS} by

$$\boxed{V_{DS_{sat}} = V_{GS} - V_T} \tag{6.14}$$

Obviously, therefore, for a fixed value of V_T, the higher the level of V_{GS}, the greater is the saturation level for V_{DS}, as shown in Fig. 6.37 by the locus of saturation levels.

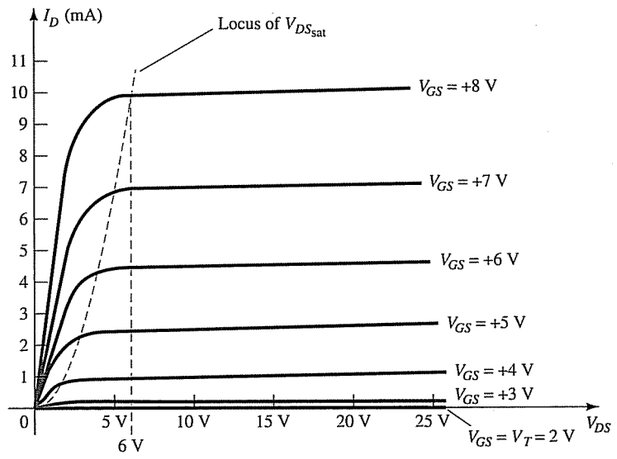


FIG. 6.38
Drain characteristics of an n-channel enhancement-type MOSFET with $V_T = 2$ V and $k = 0.278 \times 10^{-3}$ A/V^2.

For the characteristics of Fig. 6.37, the level of V_T is 2 V, as revealed by the fact that the drain current has dropped to 0 mA. In general, therefore:

For values of V_{GS} less than the threshold level, the drain current of an enhancement-type MOSFET is 0 mA.

Figure 6.38 clearly reveals that as the level of V_{GS} increases from V_T to 8 V, the resulting saturation level for I_D also increases from a level of 0 mA to 10 mA. In addition, it is quite noticeable that the spacing between the levels of V_{GS} increases as the magnitude of V_{GS} increases, resulting in ever-increasing increments in drain current.

For levels of $V_{GS} > V_T$, the drain current is related to the applied gate-to-source voltage by the following nonlinear relationship:

$$\boxed{I_D = k(V_{GS} - V_T)^2} \tag{6.15}$$

Again, it is the squared term that results in the nonlinear (curved) relationship between I_D and V_{GS}. The k term is a constant that is a function of the construction of the device. The value of k can be determined from the following equation [derived from Eq. (6.15)], where $I_{D(on)}$ and $V_{GS(on)}$ are the values for each at a particular point on the characteristics of the device.

$$\boxed{k = \frac{I_{D(on)}}{(V_{GS(on)} - V_T)^2}} \tag{6.16}$$

Substituting $I_{D(on)} = 10$ mA when $V_{GS(on)} = 8$ V from the characteristics of Fig. 6.38 yields

$$k = \frac{10\text{ mA}}{(8\text{ V} - 2\text{ V})^2} = \frac{10\text{ mA}}{(6\text{ V})^2} = \frac{10\text{ mA}}{36\text{ V}^2}$$
$$= \mathbf{0.278 \times 10^{-3}\ A/V^2}$$

and a general equation for I_D for the characteristics of Fig. 6.38 results in

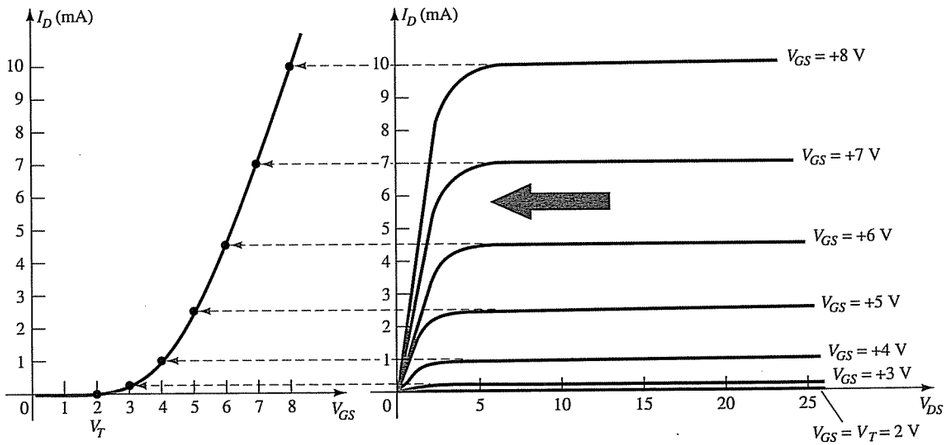
$$I_D = 0.278 \times 10^{-3}(V_{GS} - 2\text{ V})^2$$

Substituting $V_{GS} = 4$ V, we find that

$$I_D = 0.278 \times 10^{-3}(4\text{ V} - 2\text{ V})^2 = 0.278 \times 10^{-3}(2)^2$$
$$= 0.278 \times 10^{-3}(4) = \mathbf{1.11\text{ mA}}$$

as verified by Fig. 6.38. At $V_{GS} = V_T$, the squared term is 0, and $I_D = 0$ mA.

For the dc analysis of enhancement-type MOSFETs to appear in Chapter 7, the transfer characteristics will again be the characteristics to be employed in the graphical solution. In Fig. 6.39, the drain and transfer characteristics have been set side by side to describe the



Multisim
PSpice

FIG. 6.39
Sketching the transfer characteristics for an n-channel enhancement-type MOSFET from the drain characteristics.

transfer process from one to the other. Essentially, it proceeds as introduced earlier for the JFET and depletion-type MOSFETs. In this case, however, it must be remembered that the drain current is 0 mA for $V_{GS} \leq V_T$. At this point a measurable current will result for I_D and will increase as defined by Eq. (6.15). Note that in defining the points on the transfer characteristics from the drain characteristics, only the saturation levels are employed, thereby limiting the region of operation to levels of V_{DS} greater than the saturation levels as defined by Eq. (6.14).

The transfer curve of Fig. 6.39 is certainly quite different from those obtained earlier. For an *n*-channel (induced) device, it is now totally in the positive V_{GS} region and does not rise until $V_{GS} = V_T$. The question now surfaces as to how to plot the transfer characteristics given the levels of k and V_T as included below for a particular MOSFET:

$$I_D = 0.5 \times 10^{-3}(V_{GS} - 4\,\text{V})^2$$

First, a horizontal line is drawn at $I_D = 0$ mA from $V_{GS} = 0$ V to $V_{GS} = 4$ V as shown in Fig. 6.40a. Next, a level of V_{GS} greater than V_T such as 5 V is chosen and substituted into Eq. (6.15) to determine the resulting level of I_D as follows:

$$\begin{aligned} I_D &= 0.5 \times 10^{-3}(V_{GS} - 4\,\text{V})^2 \\ &= 0.5 \times 10^{-3}(5\,\text{V} - 4\,\text{V})^2 = 0.5 \times 10^{-3}(1)^2 \\ &= \mathbf{0.5\ mA} \end{aligned}$$

and a point on the plot is obtained as shown in Fig. 6.40b. Finally, additional levels of V_{GS} are chosen and the resulting levels of I_D obtained. In particular, at $V_{GS} = 6, 7$, and 8 V, the level of I_D is 2, 4.5, and 8 mA, respectively, as shown on the resulting plot of Fig. 6.40c.

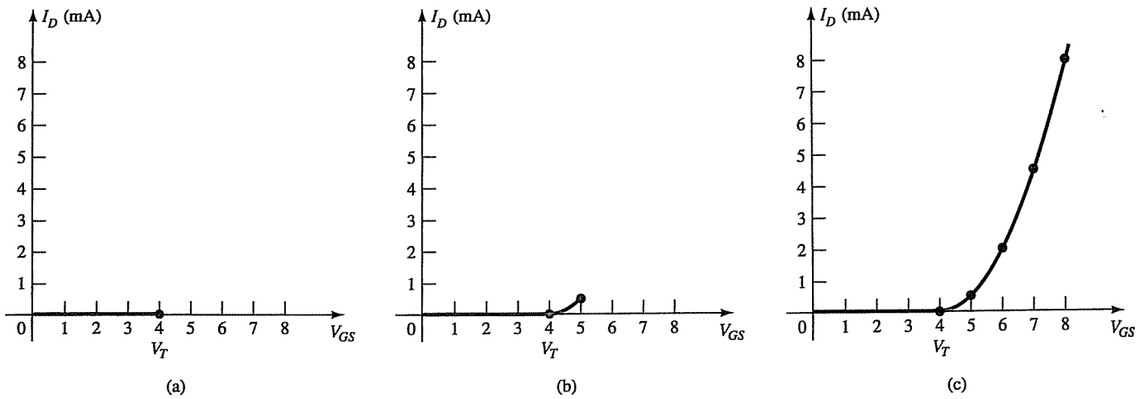


FIG. 6.40
Plotting the transfer characteristics of an n-channel enhancement-type MOSFET with $k = 0.5 \times 10^{-3}\,A/V^2$ and $V_T = 4$ V.

p-Channel Enhancement-Type MOSFETs

The construction of a *p*-channel enhancement-type MOSFET is exactly the reverse of that appearing in Fig. 6.35, as shown in Fig. 6.41a. That is, there is now an *n*-type substrate and *p*-doped regions under the drain and source connections. The terminals remain as identified, but all the voltage polarities and the current directions are reversed. The drain characteristics will appear as shown in Fig. 6.41c, with increasing levels of current resulting from increasingly negative values of V_{GS}. The transfer characteristics will be the mirror image (about the I_D axis) of the transfer curve of Fig. 6.39, with I_D increasing with increasingly negative values of V_{GS} beyond V_T, as shown in Fig. 6.41c. Equations (6.13) through (6.16) are equally applicable to *p*-channel devices.

Symbols, Specification Sheets, and Case Construction

The graphic symbols for the *n*- and *p*-channel enhancement-type MOSFETs are provided as Fig. 6.42. Again note how the symbols try to reflect the actual construction of

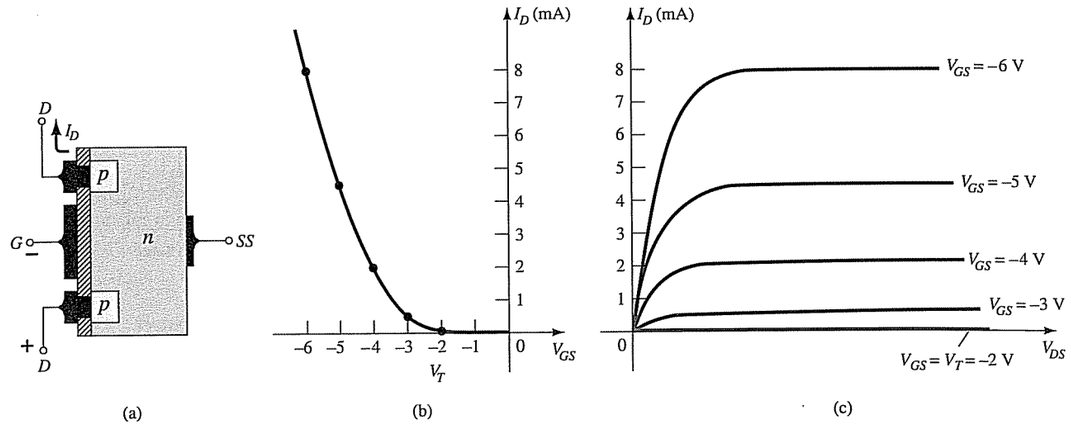


FIG. 6.41
p-Channel enhancement-type MOSFET with $V_T = 2$ V and $k = 0.5 \times 10^{-3}\,A/V^2$.

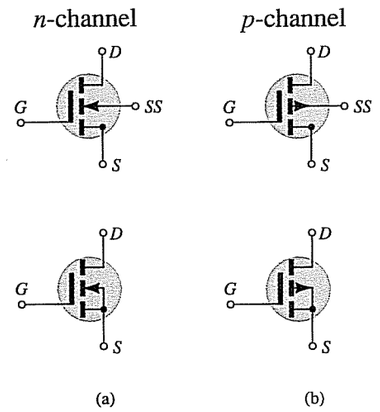


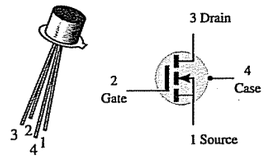
FIG. 6.42
Symbols for (a) n-channel enhancement-type MOSFETs and (b) p-channel enhancement-type MOSFETs.

the device. The dashed line between drain and source is chosen to reflect the fact that a channel does not exist between the two under no-bias conditions. It is, in fact, the only difference between the symbols for the depletion-type and enhancement-type MOSFETs.

The specification sheet for a Motorola *n*-channel enhancement-type MOSFET is provided as Fig. 6.43. The case construction and the terminal identification are provided next to the maximum ratings, which now include a maximum drain current of 30 mA dc. The specification sheet provides the level of I_{DSS} under "off" conditions, which is now simply 10 nA dc (at $V_{DS} = 10$ V and $V_{GS} = 0$ V), compared to the milliampere range for the JFET and the depletion-type MOSFET. The threshold voltage is specified as $V_{GS(\text{Th})}$ and has a range of 1 to 5 V dc, depending on the unit employed. Rather than provide a range of k in Eq. (6.15), a typical level of $I_{D(\text{on})}$ (3 mA in this case) is specified at a particular level of $V_{GS(\text{on})}$ (10 V for the specified I_D level). In other words, when $V_{GS} = 10$ V, $I_D = 3$ mA. The given levels of $V_{GS(\text{Th})}$, $I_{D(\text{on})}$, and $V_{GS(\text{on})}$ permit a determination of k from Eq. (6.16) and a writing of the general equation for the transfer characteristics. The handling requirements of MOSFETs are reviewed in Section 6.9.

2N4351

CASE 20-03, STYLE 2
TO-72 (TO-206AF)



MOSFET SWITCHING
N-CHANNEL – ENHANCEMENT

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DS}	25	Vdc
Drain–Gate Voltage	V_{DG}	30	Vdc
Gate–Source Voltage*	V_{GS}	30	Vdc
Drain Current	I_D	30	mAdc
Total Device Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	300 1.7	mW mW/°C
Junction Temperature Range	T_J	175	°C
Storage Temperature Range	T_{stg}	–65 to +175	°C

* Transient potentials of ± 75 Volt will not cause gate-oxide failure.

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage ($I_D = 10\ \mu A$, $V_{GS} = 0$)		$V_{(BR)DSX}$	25	–	Vdc
Zero-Gate-Voltage Drain Current ($V_{DS} = 10$ V, $V_{GS} = 0$)	$T_A = 25°C$ $T_A = 150°C$	I_{DSS}	– –	10 10	nAdc μAdc
Gate Reverse Current ($V_{GS} = \pm 15$ Vdc, $V_{DS} = 0$)		I_{GSS}	–	± 10	pAdc
ON CHARACTERISTICS					
Gate Threshold Voltage ($V_{DS} = 10$ V, $I_D = 10\mu A$)		$V_{GS(Th)}$	1.0	5	Vdc
Drain-Source On-Voltage ($I_D = 2.0$ mA, $V_{GS} = 10$V)		$V_{DS(on)}$	–	1.0	V
On-State Drain Current ($V_{GS} = 10$ V, $V_{DS} = 10$ V)		$I_{D(on)}$	3.0	–	mAdc
SMALL-SIGNAL CHARACTERISTICS					
Forward Transfer Admittance ($V_{DS} = 10$ V, $I_D = 2.0$ mA, f = 1.0 kHz)		$\lvert y_{fs} \rvert$	1000	–	μmho
Input Capacitance ($V_{DS} = 10$ V, $V_{GS} = 0$, f = 140 kHz)		C_{iss}	–	5.0	pF
Reverse Transfer Capacitance ($V_{DS} = 0$, $V_{GS} = 0$, f = 140 kHz)		C_{rss}	–	1.3	pF
Drain-Substrate Capacitance ($V_{D(SUB)} = 10$ V, f = 140 kHz)		$C_{d(sub)}$	–	5.0	pF
Drain-Source Resistance ($V_{GS} = 10$ V, $I_D = 0$, f = 1.0 kHz)		$r_{ds(on)}$	–	300	ohms
SWITCHING CHARACTERISTICS					
Turn-On Delay (Fig. 5)	$I_D = 2.0$ mAdc, $V_{DS} = 10$ Vdc, ($V_{GS} = 10$ Vdc) (See Figure 9; Times Circuit Determined)	t_{d1}	–	45	ns
Rise Time (Fig. 6)		t_r	–	65	ns
Turn-Off Delay (Fig. 7)		t_{d2}	–	60	ns
Fall Time (Fig. 8)		t_f	–	100	ns

FIG. 6.43
2N4351 Motorola n-channel enhancement-type MOSFET.

EXAMPLE 6.4 Using the data provided on the specification sheet of Fig. 6.43 and an average threshold voltage of $V_{GS(Th)} = 3$ V, determine:

a. The resulting value of k for the MOSFET.
b. The transfer characteristics.

Solution:

a. Eq. (6.16):
$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS(Th)})^2}$$
$$= \frac{3\text{ mA}}{(10\text{ V} - 3\text{ V})^2} = \frac{3\text{ mA}}{(7\text{ V})^2} = \frac{3 \times 10^{-3}}{49}\text{A/V}^2$$
$$= \mathbf{0.061 \times 10^{-3}\,A/V^2}$$

b. Eq. (6.15):
$$I_D = k(V_{GS} - V_T)^2$$
$$= 0.061 \times 10^{-3}(V_{GS} - 3\text{ V})^2$$

For $V_{GS} = 5$ V,
$$I_D = 0.061 \times 10^{-3}(5\text{ V} - 3\text{ V})^2 = 0.061 \times 10^{-3}(2)^2$$
$$= 0.061 \times 10^{-3}(4) = 0.244\text{ mA}$$

For $V_{GS} = 8$, 10, 12, and 14 V, I_D will be 1.525, 3 (as defined), 4.94, and 7.38 mA, respectively. The transfer characteristics are sketched in Fig. 6.44.

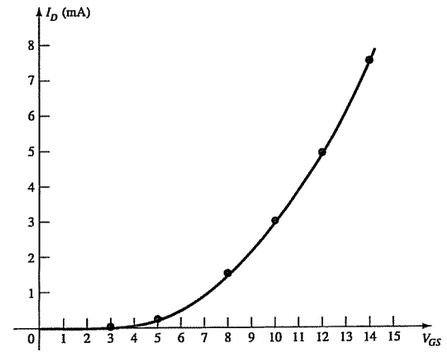


FIG. 6.44
Solution to Example 6.4.

6.9 MOSFET HANDLING

The thin SiO_2 layer between the gate and the channel of MOSFETs has the positive effect of providing a high-input-impedance characteristic for the device, but because of its extremely thin layer, it introduces a concern for its handling that was not present for the BJT or JFET transistors. There is often sufficient accumulation of static charge (picked up from the surroundings) to establish a potential difference across the thin layer that can break down the layer and establish conduction through it. It is therefore imperative to leave the shorting (or conduction) shipping foil (or ring) connecting the leads of the device together until the device is to be inserted in the system. The shorting ring prevents the possibility of applying a potential across any two terminals of the device. With the ring, the potential difference between any two terminals is maintained at 0 V. At the very least always touch ground to permit discharge of the accumulated static charge before handling the device, and always pick up the transistor by the casing.

There are often transients (sharp changes in voltage or current) in a network when elements are removed or inserted if the power is on. The transient levels can often be more than the device can handle, and therefore the power should always be off when network changes are made.

The maximum gate-to-source voltage is normally provided in the list of maximum ratings of the device. One method of ensuring that this voltage is not exceeded (perhaps by transient effects) for either polarity is to introduce two Zener diodes, as shown in Fig. 6.45. The Zeners are back to back to ensure protection for either polarity. If both are 30-V Zeners and a positive transient of 40 V appears, the lower Zener will "fire" at 30 V and the upper will turn on with a 0-V drop (ideally—for the positive "on" region of a semiconductor diode) across the other diode. The result is a maximum of 30 V for the gate-to-source voltage. One disadvantage introduced by the Zener protection is that the off resistance of a Zener diode is less than the input impedance established by the SiO_2 layer. The result is a reduction in input resistance, but even so, it is still high enough for most applications. So many of the discrete devices now have the Zener protection that some of the concerns listed above are not as troublesome. However, it is still best to be somewhat cautious when handling discrete MOSFET devices.

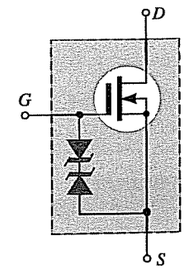


FIG. 6.45
Zener-protected MOSFET.

6.10 VMOS

One of the disadvantages of the typical MOSFET is the reduced power-handling levels (typically, less than 1 W) compared to BJT transistors. This shortfall for a device with so many positive characteristics can be softened by changing the construction mode from one of a planar nature such as shown in Fig. 6.27 to one with a vertical structure as shown in Fig. 6.46. All the elements of the planar MOSFET are present in the vertical metal–oxide–silicon FET (VMOS)—the metallic surface connection to the terminals of the device, the SiO_2 layer between the gate, and the *p*-type region between the drain and the source for the growth of the induced *n*-channel (enhancement-mode operation). The term *vertical* is due primarily to the fact that the channel is now formed in the vertical direction rather than the horizontal direction as for the planar device. However, the channel of Fig. 6.46 also has the appearance of a "V" cut in the semiconductor base, which often stands out as a characteristic for memorization of the name of the device. The construction of Fig. 6.46 is somewhat simplistic in nature, leaving out some of the transition levels of doping, but it does permit a description of the most important facets of its operation.

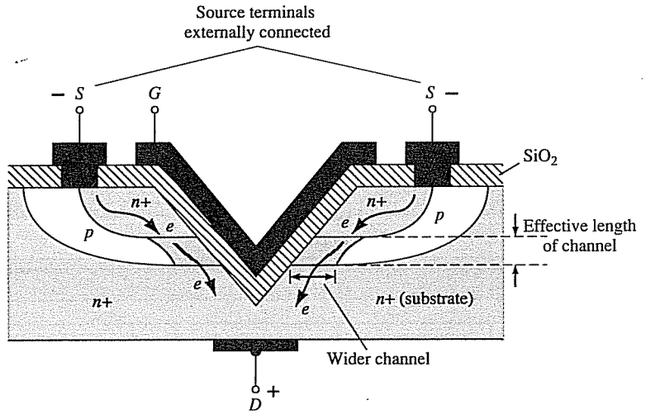


FIG. 6.46
VMOS construction.

The application of a positive voltage to the drain and a negative voltage to the source with the gate at 0 V or some typical positive "on" level as shown in Fig. 6.46 results in the induced *n*-channel in the narrow *p*-type region of the device. The length of the channel is now defined by the vertical height of the *p*-region, which can be made significantly less than that of a channel using planar construction. On a horizontal plane the length of the channel is limited to 1 μm to 2 μm (1 μm $= 10^{-6}$ m). Diffusion layers (such as the *p*-region of Fig. 6.46) can be controlled to small fractions of a micrometer. Since decreasing channel lengths result in reduced resistance levels, the power dissipation level of the device (power lost in the form of heat) at operating current levels will be reduced. In addition, the contact area between the channel and the n^+ region is greatly increased by the vertical mode construction, contributing to a further decrease in the resistance level and an increased area for current between the doping layers. There is also the existence of two conduction paths between drain and source, as shown in Fig. 6.46, to further contribute to a higher current rating. The net result is a device with drain currents that can reach the ampere levels with power levels exceeding 10 W.

In general:

Compared with commercially available planar MOSFETs, VMOS FETs have reduced channel resistance levels and higher current and power ratings.

An additional important characteristic of the vertical construction is:

VMOS FETs have a positive temperature coefficient, which combats the possibility of thermal runaway.

If the temperature of a device should increase due to the surrounding medium or currents of the device, the resistance levels will increase, causing a reduction in drain current rather than an increase as encountered for a conventional device. Negative temperature coefficients result in decreased levels of resistance with increases in temperature, which fuel the growing current levels and result in further temperature instability and thermal runaway.

Another positive characteristic of the VMOS configuration is:

The reduced charge storage levels result in faster switching times for VMOS construction compared to those for conventional planar construction.

In fact, VMOS devices typically have switching times less than one-half that encountered for the typical BJT transistor.

6.11 CMOS

A very effective logic circuit can be established by constructing a *p*-channel and an *n*-channel MOSFET on the same substrate as shown in Fig. 6.47. Note the induced *p*-channel on the left and the induced *n*-channel on the right for the *p*- and *n*-channel devices, respectively. The configuration is referred to as a *complementary MOSFET* arrangement (CMOS); it has extensive applications in computer logic design. The relatively high input impedance, fast switching speeds, and lower operating power levels of the CMOS configuration have resulted in a whole new discipline referred to as *CMOS logic design.*

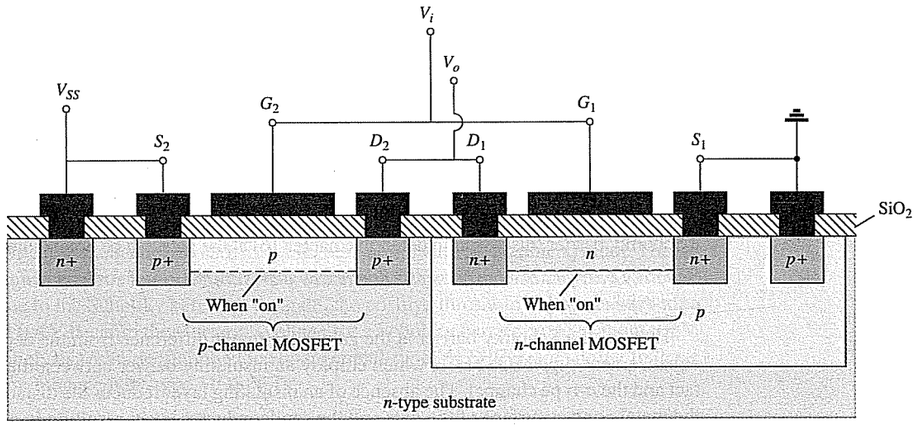


FIG. 6.47
CMOS with the connections indicated in Fig. 6.48.

One very effective use of the complementary arrangement is as an inverter, as shown in Fig. 6.48. As introduced for switching transistors, an inverter is a logic element that "inverts" the applied signal. That is, if the logic levels of operation are 0 V (0-state) and 5 V (1-state), an input level of 0 V will result in an output level of 5 V, and vice versa. Note in Fig. 6.48 that both gates are connected to the applied signal and both drain to the output V_o. The source of the *p*-channel MOSFET (Q_2) is connected directly to the applied voltage V_{SS}, whereas the source of the *n*-channel MOSFET (Q_1) is connected to ground. For the logic levels defined above, the application of 5 V at the input should result in approximately 0 V at the output. With 5 V at V_i (with respect to ground), $V_{GS_1} = V_i$, and Q_1 is "on," resulting in a relatively low resistance between drain and source as shown in Fig. 6.49. Since V_i and V_{SS} are at 5 V, $V_{GS_2} = 0$ V, which is less than the required V_T for the device, resulting in an "off" state. The resulting resistance level between drain and source is quite high for Q_2, as shown in Fig. 6.49. A simple application of the voltage-divider rule will reveal that V_o is very close to 0 V, or the 0-state, establishing the desired inversion process. For an applied voltage V_i of 0 V (0-state), $V_{GS_1} = 0$ V, and Q_1 will be "off" with $V_{SS_2} = -5$ V, turning on the *p*-channel MOSFET. The result is that Q_2 will present a small resistance level, Q_1 a high resistance, and $V_o = V_{SS} = 5$ V (the 1-state). Since the drain current that flows for either case is limited by the "off" transistor to the leakage value, the power dissipated by the device in either state is very low. Additional comment on the application of CMOS logic is presented in Chapter 13.

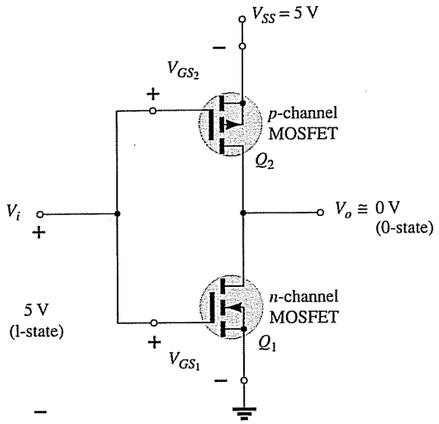


FIG. 6.48
CMOS inverter.

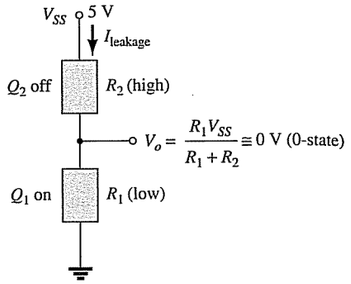


FIG. 6.49
Relative resistance levels for $V_i = 5$ V (1-state).

Multisim

6.12 MESFETs

As noted in earlier discussions, the use of GaAs in the construction of semiconductor devices has been around for quite a few decades. Unfortunately, however, the manufacturing costs, lower resulting density in ICs, and production problems have kept it from prominence in the industry until the last few years. The need for high-speed devices and improved production methods in recent years have established a strong demand for large-scale integrated circuits using GaAs.

Although the Si MOSFETs just described can be made using GaAs instead, it is a more difficult manufacturing process due to diffusion problems. However, the production of FETs using a Schottky barrier (discussed in detail in Chapter 16) at the gate can be done quite efficiently:

Schottky barriers are barriers established by depositing a metal such as tungsten on an n-type channel

The use of a Schottky barrier at the gate is the major difference from the depletion- and enhancement-type MOSFETs, which employ an insulating barrier between the metal contact and the n-type channel. The absence of an insulating layer reduces the distance between the metal contact surface of the gate and the semiconductor layer, resulting in a lower level of stray capacitance between the two surfaces (recall the effect of distance between the plates of a capacitor and its terminal capacitance). The result of the lower capacitance level is a reduced sensitivity to high frequencies (forming a shorting effect), which further supports the high mobility of carriers in the GaAs material.

The presence of a metal–semiconductor junction is the reason such FETs are called *metal–semiconductor field-effect transistors* (MESFETs). The basic construction of a MESFET is provided in Fig. 6.50. Note in Fig. 6.50 that the gate terminal is connected directly to a

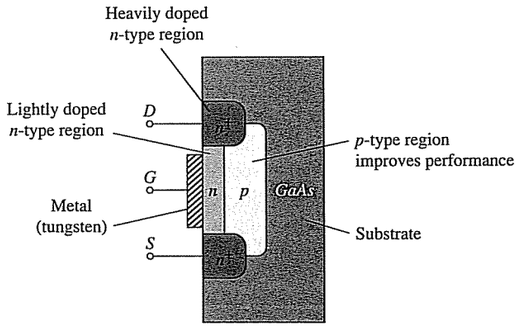


FIG. 6.50
Basic construction of an n-channel MESFET.

metallic conductor lying directly against the n-channel between the source and drain terminals. The only difference from the depletion-type MOSFET construction is the absence of the insulator at the gate. When a negative voltage is applied to the gate, it will attract free negative carriers (electrons) in the channel to the metal surface, reducing the number of carriers in the channel. The result is a reduced drain current, as shown in Fig. 6.51, for increasing values of negative voltage at the gate terminal. For positive voltages at the gate, additional electrons will be attracted into the channel and the current will rise as shown by the drain characteristics of Fig. 6.51. The fact that the drain and transfer characteristics of the depletion-type MESFET are so similar to those of the depletion-type MOSFET results in analysis techniques similar to those applied to depletion-type MOSFETs. The defined polarities and current directions for the MESFET are provided in Fig. 6.52 along with the symbol for the device.

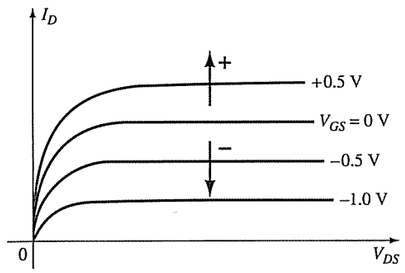


FIG. 6.51
Characteristics of an n-channel MESFET.

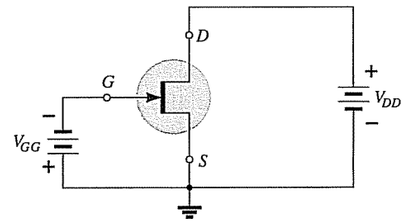


FIG. 6.52
Symbol and basic biasing arrangement for an n-channel MESFET.

There are also enhancement-type MESFETs with a construction the same as in Fig. 6.50 but without the initial channel, as shown in Fig. 6.53 along with its graphic symbol. The response and characteristics are essentially the same as for the enhancement-type MOSFET. However, due to the Schottky barrier at the gate, the positive threshold voltage is limited to 0 V to about 0.4 V because the "turn-on" voltage for a Schottky barrier diode is about 0.7 V. Again, the analysis techniques applied to enhancement-type MESFETs are similar to those employed for enhancement-type MOSFETs.

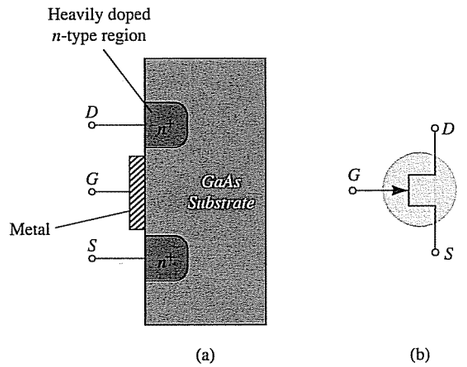
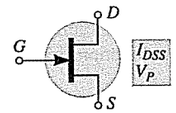
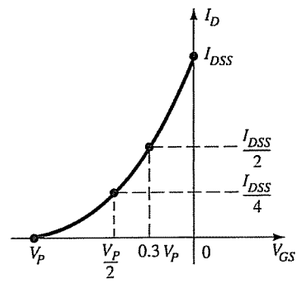
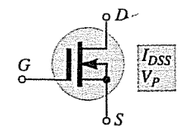
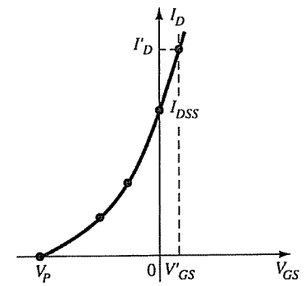
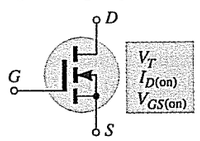
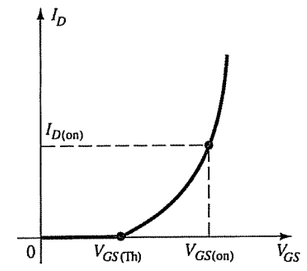
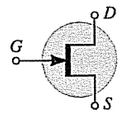
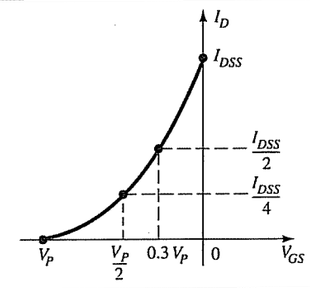
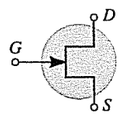
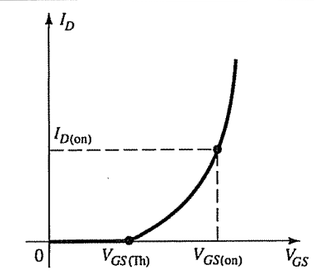


FIG. 6.53
Enhancement-type MESFET: (a) construction; (b) symbol.

It is important to realize, however, that the channel must be an n-type material in a MESFET. The mobility of holes in GaAs is relatively low compared to that of the negatively charged carriers, losing the advantage of using GaAs for high-speed applications. The result is:

Depletion-type and enhancement-type MESFETs are made with an n-channel between the drain and the source, and therefore only n-type MESFETs are commercially available.

TABLE 6.2
Field Effect Transistors

Type	Symbol and Basic Relationships	Transfer Curve	Input Resistance and Capacitance
JFET (*n*-channel)	$I_G = 0$ A, $I_D = I_S$  $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$		$R_i > 100\,\text{M}\Omega$ C_i: (1 – 10) pF
MOSFET depletion type (*n*-channel)	$I_G = 0$ A, $I_D = I_S$  $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$		$R_i > 10^{10}\,\Omega$ C_i: (1 – 10) pF
MOSFET enhancement type (*n*-channel)	$I_G = 0$ A, $I_D = I_S$  $I_D = k(V_{GS} - V_{GS(Th)})^2$ $k = \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS(Th)})^2}$		$R_i > 10^{10}\,\Omega$ C_i: (1 – 10) pF
MESFET depletion type (*n*-channel)	$I_G = 0$ A, $I_D = I_S$  $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$ $I_G = 0$ A, $I_D = I_S$		$R_i > 10^{12}\,\Omega$ C_i: (1 – 5) pF
MESFET enhancement type (*n*-channel)	 $I_D = k(V_{GS} - V_{GS(Th)})^2$ $k = \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS(Th)})^2}$		$R_i > 10^{12}\,\Omega$ C_i: (1 – 5) pF

For both types of MESFETs the channel length (identified in Figs. 6.50 and 6.53) should be made as short as possible for high-speed applications. The length is typically between 0.1 μm and 1 μm.

6.13 SUMMARY TABLE

Since the transfer curves and some important characteristics vary from one type of FET to another, Table 6.2 was developed to clearly display the differences from one device to the next. A clear understanding of all the curves and parameters of the table will provide a sufficient background for the dc and ac analyses to follow. Take a moment to ensure that each curve is recognizable and its derivation understood, and then establish a basis for comparison of the levels of the important parameters of R_i and C_i for each device.

6.14 SUMMARY

Important Conclusions and Concepts

1. A **current-controlled device** is one in which a current defines the operating conditions of the device, whereas a **voltage-controlled device** is one in which a particular voltage defines the operating conditions.
2. The JFET can actually be used as a **voltage-controlled resistor** because of a unique sensitivity of the drain-to-source impedance to the gate-to-source voltage.
3. The **maximum current** for any JFET is labeled I_{DSS} and occurs when $V_{GS} = 0$ V.
4. The **minimum current** for a JFET occurs at pinch-off defined by $V_{GS} = V_P$.
5. The relationship between the drain current and the gate-to-source voltage of a JFET is a **nonlinear one** defined by Shockley's equation. As the current level approaches I_{DSS}, the sensitivity of I_D to changes in V_{GS} increases significantly.
6. The transfer characteristics (I_D versus V_{GS}) are characteristics **of the device itself** and are not sensitive to the network in which the JFET is employed.
7. When $V_{GS} = V_P/2$, $I_D = I_{DSS}/4$; and at a point where $I_D = I_{DSS}/2$, $V_{GS} \cong 0.3$ V.
8. Maximum operating conditions are determined by the **product** of the drain-to-source voltage and the drain current.
9. MOSFETs are available in one of two types: **depletion and enhancement**.
10. The depletion-type MOSFET has the same transfer characteristics as a JFET for drain currents up to the I_{DSS} level. At this point the characteristics of a depletion-type MOSFET **continue to levels above** I_{DSS}, whereas those of the JFET will end.
11. The arrow in the symbol of *n*-channel JFETs or MOSFETs will **always point in to the center of the symbol**, whereas those of a *p*-channel device will always point out of the center of the symbol.
12. The transfer characteristics of an enhancement-type MOSFET are **not defined by Shockley's equation** but rather by a nonlinear equation controlled by the gate-to-source voltage, the threshold voltage, and a constant *k* defined by the device employed. The resulting plot of I_D versus V_{GS} **rises exponentially with incrseasing values of** V_{GS}.
13. Always handle MOSFETs with **additional care** due to the static electricity that exists in places we might least suspect. Do not remove any shorting mechanism between the leads of the device until it is installed.
14. A CMOS (complementary MOSFET) device employs a unique **combination of a *p*-channel and an *n*-channel MOSFET** with a single set of external leads. It has the advantages of a very high input impedance, fast switching speeds, and low operating power levels, all of which make it very useful in logic circuits.
15. A depletion-type MESFET includes a metal–semiconductor junction, resulting in characteristics that **match those of an *n*-channel depletion-type JFET**. Enhancement-type MESFETs have the same characteristics as enhancement-type MOSFETs. The result of this similarity is that the **same type of dc and ac analysis techniques can be applied to MESFETs as was applied to JFETs**.

Equations

JFET:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$I_D = I_{DSS}\big|_{V_{GS}=0\text{ V}}, \quad I_D = 0\text{ mA}\big|_{V_{GS}=V_P}, \quad I_D = \frac{I_{DSS}}{4}\bigg|_{V_{GS}=V_P/2}, \quad V_{GS} \cong 0.3V_P\big|_{I_D=I_{DSS}/2}$$

$$V_{GS} = V_P\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)$$

$$P_D = V_{DS}I_D$$

$$r_d = \frac{r_o}{(1 - V_{GS}/V_P)^2}$$

MOSFET (enhancement):

$$I_D = k(V_{GS} - V_T)^2$$

$$k = \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_T)^2}$$

6.15 COMPUTER ANALYSIS

PSpice Windows

The characteristics of an *n*-channel JFET can be displayed using the same procedure employed for the transistor in Section 3.13. The series of curves across the characteristics plotted against various values of voltage requires a nested sweep within the sweep for the drain-to-source voltage. The required configuration of Fig. 6.54 is constructed using procedures described in the previous chapters. In particular, note the complete absence of resistors since the input impedance is assumed to be infinite, resulting in a gate current of 0 A. The JFET is found under **Part** in the **Place Part** dialog box. It can be called up by simply typing in **JFET** in the provided space under the **Part** heading. Once in place, a single click on the symbol followed by **Edit-PSpice Model** will result in the **PSpice Model Editor Lite** dialog box. Note that **Beta** is equal to 1.304 mA/V^2 and **Vto** is -3 V. For the junction field effect transistor **Beta** is defined by

$$\boxed{\text{Beta} = \frac{I_{DSS}}{|V_P|^2}} \quad (\text{A/V}^2) \tag{6.17}$$

The parameter **Vto** defines $V_{GS} = V_P = -3$ V as the pinch-off voltage. Using Eq. (6.17), one can solve for I_{DSS} and find that it is about 11.37 mA. Once the plots are obtained one can check whether both of these parameters are accurately defined the characteristics. With the network established, select a **New Simulation** to obtain the **New Simulation** dialog box. Using **Fig 6.54** as the name followed by **Create** results in the **Simulation Settings** dialog box, in which **DC Sweep** is selected under the **Analysis type** heading. The **Sweep variable** is set as a **Voltage source** with the **Name VDD**. The **Start Value** is 0 V, the **End Value** is 10 V, and the **Increment** is 0.01 V. Now select **Secondary Sweep** and apply the **Name VGG** with a **Start Value** of 0 V, an **End Value** of -5 V, and an **Increment** of -1 V. Finally, the **Secondary Sweep** must be enabled by ensuring the check appears in the box to the left of the listing, followed by an **OK** to leave the dialog box. A **Simulation**, and the **SCHEMATIC** screen will appear with a horizontal axis labeled **VDD** extending from 0 V to 10 V. Continue with the sequence **Trace-Add Trace** to obtain the **Add Traces** dialog box, and select **ID(J1)** to obtain the characteristics of Fig. 6.55. Note in particular that I_{DSS} is very close to 11.7 mA as predicted based on the value of Beta. Also note that cutoff does occur at $V_{GS} = V_P = -3$ V. The labels appearing on the graph were added using **Plot-Label-Text**.

The transfer characteristics can be obtained by setting up a **New Simulation** that has a single sweep since there is only one curve to plot. Once **DC Sweep** is again selected, the

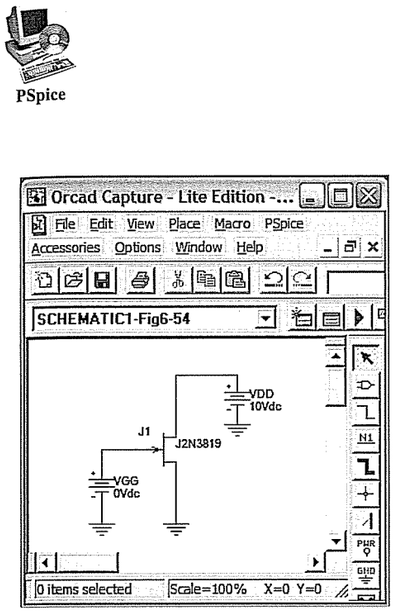


FIG. 6.54
Network used to obtain the characteristics of the n-channel J2N3819 JFET.

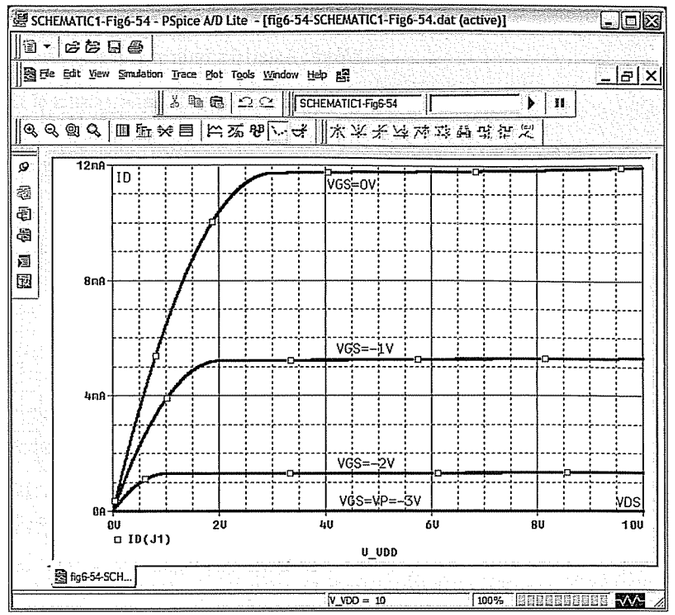


FIG. 6.55
Drain characteristics for the n-channel J2N3819 JFET of Fig. 6.54.

Name is **VGG** with a **Start Value** of -3 V, an **End Value** of 0 V, and an **Increment** of 0.01 V. Since there is no need for a secondary nested sweep, select **OK**, and the simulation is performed. When the graph appears, select **Trace-Add Trace-ID(J1)** to obtain the transfer characteristics of Fig. 6.56. Note how the axis is set with the -3 V to the far left and the 0 V to the far right. Again, I_{DSS} is very close to the predicted 11.7 mA and $V_P = -3$ V.

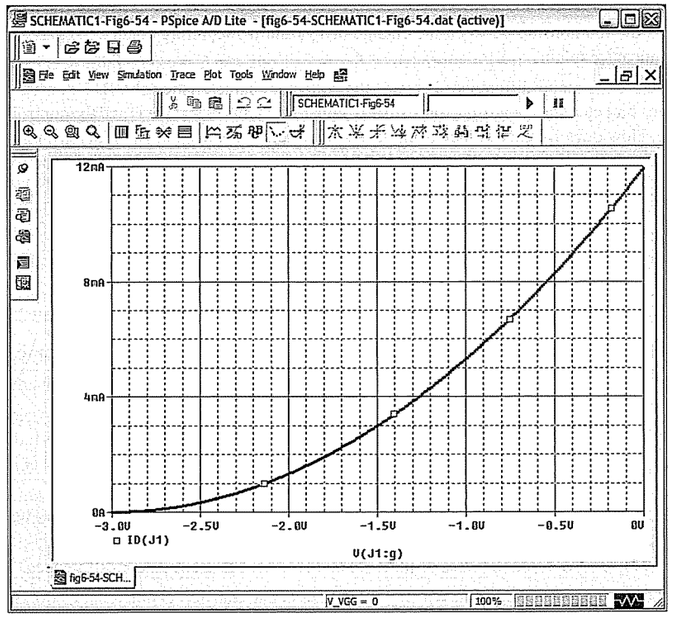


FIG. 6.56
Transfer characteristics for the n-channel J2N3819 JFET of Fig. 6.54.

PROBLEMS

*Note: Asterisks indicate more difficult problems.

6.2 Construction and Characteristics of JFETs

1. a. Draw the basic construction of a *p*-channel JFET.
   b. Apply the proper biasing between drain and source and sketch the depletion region for $V_{GS} = 0$ V.
2. Using the characteristics of Fig. 6.11, determine I_D for the following levels of V_{GS} (with $V_{DS} > V_P$):
   a. $V_{GS} = 0$ V.
   b. $V_{GS} = -1$ V.
   c. $V_{GS} = -1.5$ V.
   d. $V_{GS} = -1.8$ V.
   e. $V_{GS} = -4$ V.
   f. $V_{GS} = -6$ V.
3. a. Determine V_{DS} for $V_{GS} = 0$ V and $I_D = 6$ mA using the characteristics of Fig. 6.11.
   b. Using the results of part (a), calculate the resistance of the JFET for the region $I_D = 0$ to 6 mA for $V_{GS} = 0$ V.
   c. Determine V_{DS} for $V_{GS} = -1$ V and $I_D = 3$ mA.
   d. Using the results of part (c), calculate the resistance of the JFET for the region $I_D = 0$ to 3 mA for $V_{GS} = -1$ V.
   e. Determine V_{DS} for $V_{GS} = -2$ V and $I_D = 1.5$ mA.
   f. Using the results of part (e), calculate the resistance of the JFET for the region $I_D = 0$ to 1.5 mA for $V_{GS} = -2$ V.
   g. Defining the result of part (b) as r_o, determine the resistance for $V_{GS} = -1$ V using Eq. (6.1) and compare with the results of part (d).
   h. Repeat part (g) for $V_{GS} = -2$ V using the same equation, and compare the results with part (f).
   i. Based on the results of parts (g) and (h), does Eq. (6.1) appear to be a valid approximation?
4. Using the characteristics of Fig. 6.11:
   a. Determine the difference in drain current (for $V_{DS} > V_P$) between $V_{GS} = 0$ V and $V_{GS} = -1$ V.
   b. Repeat part (a) between $V_{GS} = -1$ and -2 V.
   c. Repeat part (a) between $V_{GS} = -2$ and -3 V.
   d. Repeat part (a) between $V_{GS} = -3$ and -4 V.
   e. Is there a marked change in the difference in current levels as V_{GS} becomes increasingly negative?
   f. Is the relationship between the change in V_{GS} and the resulting change in I_D linear or nonlinear? Explain.
5. What are the major differences between the collector characteristics of a BJT transistor and the drain characteristics of a JFET transistor? Compare the units of each axis and the controlling variable. How does I_C react to increasing levels of I_B versus changes in I_D to increasingly negative values of V_{GS}? How does the spacing between steps of I_B compare to the spacing between steps of V_{GS}? Compare $V_{C_{sat}}$ to V_P in defining the nonlinear region at low levels of output voltage.
6. a. Describe in your own words why I_G is effectively 0 A for a JFET transistor.
   b. Why is the input impedance to a JFET so high?
   c. Why is the terminology *field effect* appropriate for this important three-terminal device?
7. Given $I_{DSS} = 12$ mA and $|V_P| = 6$ V, sketch a probable distribution of characteristic curves for the JFET (similar to Fig. 6.11).
8. In general, comment on the polarity of the various voltages and direction of the currents for an *n*-channel JFET versus a *p*-channel JFET.

6.3 Transfer Characteristics

9. Given the characteristics of Fig. 6.57:
   a. Sketch the transfer characteristics directly from the drain characteristics.
   b. Using Fig. 6.57 to establish the values of I_{DSS} and V_P, sketch the transfer characteristics using Shockley's equation.
   c. Compare the characteristics of parts (a) and (b). Are there any major differences?
10. a. Given $I_{DSS} = 12$ mA and $V_P = -4$ V, sketch the transfer characteristics for the JFET transistor.
    b. Sketch the drain characteristics for the device of part (a).

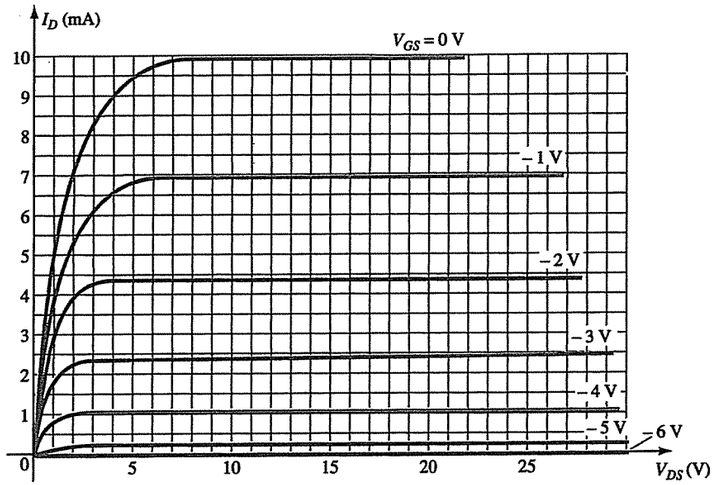


FIG. 6.57
Problems 9 and 17.

11. Given $I_{DSS} = 9$ mA and $V_P = -3.5$ V, determine I_D when:
    a. $V_{GS} = 0$ V.
    b. $V_{GS} = -2$ V.
    c. $V_{GS} = -3.5$ V.
    d. $V_{GS} = -5$ V.
12. Given $I_{DSS} = 16$ mA and $V_P = -5$ V, sketch the transfer characteristics using the data points of Table 6.1. Determine the value of I_D at $V_{GS} = -3$ V from the curve, and compare it to the value determined using Shockley's equation. Repeat the above for $V_{GS} = -1$ V.
13. A *p*-channel JFET has device parameters of $I_{DSS} = 7.5$ mA and $V_P = 4$ V. Sketch the transfer characteristics.
14. Given $I_{DSS} = 6$ mA and $V_P = -4.5$ V:
    a. Determine I_D at $V_{GS} = -2$ and -3.6 V.
    b. Determine V_{GS} at $I_D = 3$ and 5.5 mA.
15. Given a *Q*-point of $I_{D_Q} = 3$ mA and $V_{GS} = -3$ V, determine I_{DSS} if $V_P = -6$ V.

6.4 Specification Sheets (JFETs)

16. Define the region of operation for the 2N5457 JFET of Fig. 6.22 using the range of I_{DSS} and V_P provided. That is, sketch the transfer curve defined by the maximum I_{DSS} and V_P and the transfer curve for the minimum I_{DSS} and V_P. Then, shade in the resulting area between the two curves.
17. Define the region of operation for the JFET of Fig. 6.57 if $V_{DS_{max}} = 25$ V and $P_{D_{max}} = 120$ mW.

6.5 Instrumentation

18. Using the characteristics of Fig. 6.25, determine I_D at $V_{GS} = -0.7$ V and $V_{DS} = 10$ V.
19. Referring to Fig. 6.25, is the locus of pinch-off values defined by the region of $V_{DS} < |V_P| = 3$ V?
20. Determine V_P for the characteristics of Fig. 6.25 using I_{DSS} and I_D at some value of V_{GS}. That is, simply substitute into Shockley's equation and solve for V_P. Compare the result to the assumed value of -3 V from the characteristics.
21. Using $I_{DSS} = 9$ mA and $V_P = -3$ V for the characteristics of Fig. 6.25, calculate I_D at $V_{GS} = -1$ V using Shockley's equation and compare to the level in Fig. 6.25.
22. a. Calculate the resistance associated with the JFET of Fig. 6.25 for $V_{GS} = 0$ V from $I_D = 0$ mA to 4 mA.
    b. Repeat part (a) for $V_{GS} = -0.5$ V from $I_D = 0$ to 3 mA.
    c. Assigning the label r_o to the result of part (a) and r_d to that of part (b), use Eq. (6.1) to determine r_d and compare to the result of part (b).

6.7 Depletion-Type MOSFET

23. **a.** Sketch the basic construction of a *p*-channel depletion-type MOSFET.
b. Apply the proper drain-to-source voltage and sketch the flow of electrons for $V_{GS} = 0$ V.

24. In what ways is the construction of a depletion-type MOSFET similar to that of a JFET? In what ways is it different?

25. Explain in your own words why the application of a positive voltage to the gate of an *n*-channel depletion-type MOSFET will result in a drain current exceeding I_{DSS}.

26. Given a depletion-type MOSFET with $I_{DSS} = 6$ mA and $V_P = -3$ V, determine the drain current at $V_{GS} = -1, 0, 1$, and 2 V. Compare the difference in current levels between -1 V and 0 V with the difference between 1 V and 2 V. In the positive V_{GS} region, does the drain current increase at a significantly higher rate than for negative values? Does the I_D curve become more and more vertical with increasing positive values of V_{GS}? Is there a linear or a nonlinear relationship between I_D and V_{GS}? Explain.

27. Sketch the transfer and drain characteristics of an *n*-channel depletion-type MOSFET with $I_{DSS} = 12$ mA and $V_P = -8$ V for a range of $V_{GS} = -V_P$ to $V_{GS} = 1$ V.

28. Given $I_D = 14$ mA and $V_{GS} = 1$ V, determine V_P if $I_{DSS} = 9.5$ mA for a depletion-type MOSFET.

29. Given $I_D = 4$ mA at $V_{GS} = -2$ V, determine I_{DSS} if $V_P = -5$ V.

30. Using an average value of 2.9 mA for the I_{DSS} of the 2N3797 MOSFET of Fig. 6.34, determine the level of V_{GS} that will result in a maximum drain current of 20 mA if $V_P = -5$ V.

31. If the drain current for the 2N3797 MOSFET of Fig. 6.34 is 8 mA, what is the maximum permissible value of V_{DS} utilizing the maximum power rating?

6.8 Enhancement-Type MOSFET

32. **a.** What is the significant difference between the construction of an enhancement-type MOSFET and a depletion-type MOSFET?
b. Sketch a *p*-channel enhancement-type MOSFET with the proper biasing applied ($V_{DS} > 0$ V, $V_{GS} > V_T$) and indicate the channel, the direction of electron flow, and the resulting depletion region.
c. In your own words, briefly describe the basic operation of an enhancement-type MOSFET.

33. **a.** Sketch the transfer and drain characteristics of an *n*-channel enhancement-type MOSFET if $V_T = 3.5$ V and $k = 0.4 \times 10^{-3}$ A/V^2.
b. Repeat part (a) for the transfer characteristics if V_T is maintained at 3.5 V but k is increased by 100% to 0.8×10^{-3} A/V^2.

34. **a.** Given $V_{GS(Th)} = 4$ V and $I_{D(on)} = 4$ mA at $V_{GS(on)} = 6$ V, determine k and write the general expression for I_D in the format of Eq. (6.15).
b. Sketch the transfer characteristics for the device of part (a).
c. Determine I_D for the device of part (a) at $V_{GS} = 2, 5$, and 10 V.

35. Given the transfer characteristics of Fig. 6.58, determine V_T and k and write the general equation for I_D.

36. Given $k = 0.4 \times 10^{-3}$ A/V^2 and $I_{D(on)} = 3$ mA with $V_{GS(on)} = 4$ V, determine V_T.

37. The maximum drain current for the 2N4351 *n*-channel enhancement-type MOSFET is 30 mA. Determine V_{GS} at this current level if $k = 0.06 \times 10^{-3}$ A/V^2 and V_T is the maximum value.

38. Does the current of an enhancement-type MOSFET increase at about the same rate as a depletion-type MOSFET for the conduction region? Carefully review the general format of the equations, and if your mathematics background includes differential calculus, calculate dI_D/dV_{GS} and compare its magnitude.

39. Sketch the transfer characteristics of a *p*-channel enhancement-type MOSFET if $V_T = -5$ V and $k = 0.45 \times 10^{-3}$ A/V^2.

40. Sketch the curve of $I_D = 0.5 \times 10^{-3}(V_{GS}^2)$ and $I_D = 0.5 \times 10^{-3}(V_{GS} - 4)^2$ for V_{GS} from 0 V to 10 V. Does $V_T = 4$ V have a significant effect on the level of I_D for this region?

6.10 VMOS

41. **a.** Describe in your own words why the VMOS FET can withstand a higher current and power rating than devices constructed with standard techniques.
b. Why do VMOS FETs have reduced channel resistance levels?
c. Why is a positive temperature coefficient desirable?

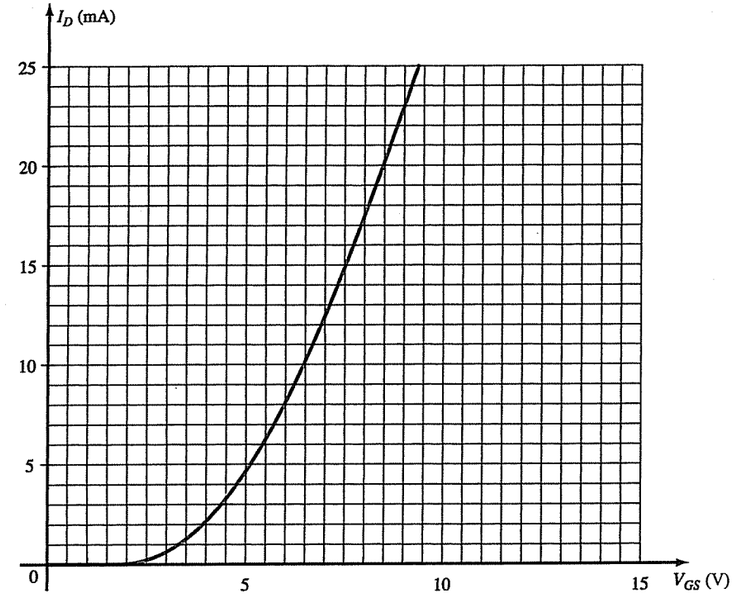


FIG. 6.58
Problem 35.

6.11 CMOS

***42.** **a.** Describe in your own words the operation of the network of Fig. 6.48 with $V_i = 0$ V.
b. If the "on" MOSFET of Fig. 6.48 (with $V_i = 0$ V) has a drain current of 4 mA with $V_{DS} = 0.1$ V, what is the approximate resistance level of the device? If $I_D = 0.5$ μA for the "off" transistor, what is the approximate resistance of the device? Do the resulting resistance levels suggest that the desired output voltage level will result?

43. Research CMOS logic at your local or college library, and describe the range of applications and basic advantages of the approach.

7 FET Biasing

CHAPTER OUTLINE

7.1 Introduction
7.2 Fixed-Bias Configuration
7.3 Self-Bias Configuration
7.4 Voltage-Divider Biasing
7.5 Depletion-Type MOSFETs
7.6 Enhancement-Type MOSFETs
7.7 Summary Table
7.8 Combination Networks
7.9 Design
7.10 Troubleshooting
7.11 *p*-Channel FETs
7.12 Universal JFET Bias Curve
7.13 Practical Applications
7.14 Summary
7.15 Computer Analysis

7.1 INTRODUCTION

In Chapter 4 we found that the biasing levels for a silicon transistor configuration can be obtained using the approximate characteristic equations $V_{BE} = 0.7\,\text{V}$, $I_C = \beta I_B$, and $I_C \cong I_E$. The link between input and output variables is provided by β, which is assumed to be fixed in magnitude for the analysis to be performed. The fact that beta is a constant establishes a *linear* relationship between I_C and I_B. Doubling the value of I_B will double the level of I_C, and so on.

For the field-effect transistor, the relationship between input and output quantities is *nonlinear* due to the squared term in Shockley's equation. Linear relationships result in straight lines when plotted on a graph of one variable versus the other, whereas nonlinear functions result in curves as obtained for the transfer characteristics of a JFET. The nonlinear relationship between I_D and V_{GS} can complicate the mathematical approach to the dc analysis of FET configurations. A graphical approach may limit solutions to tenths-place accuracy, but it is a quicker method for most FET amplifiers. Since the graphical approach is in general the most popular, the analysis of this chapter will have a graphical orientation rather than use direct mathematical techniques.

Another distinct difference between the analysis of BJT and FET transistors is that:

The input controlling variable for a BJT transistor is a current level, whereas for the FET a voltage is the controlling variable.

In both cases, however, the controlled variable on the output side is a current level that also defines the important voltage levels of the output circuit.

The general relationships that can be applied to the dc analysis of all FET amplifiers are

$$\boxed{I_G \cong 0\,\text{A}} \tag{7.1}$$

and

$$\boxed{I_D = I_S} \tag{7.2}$$

For JFETS and depletion-type MOSFETs and MESFETs, Shockley's equation is applied to relate the input and output quantities:

$$\boxed{I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2} \tag{7.3}$$

For enhancement-type MOSFETs and MESFETs, the following equation is applicable:

$$\boxed{I_D = k(V_{GS} - V_T)^2} \tag{7.4}$$

It is particularly important to realize that all of the equations above are for the *device only*! They do not change with each network configuration so long as the device is in the active region. The network simply defines the level of current and voltage associated with the operating point through its own set of equations. In reality, the dc solution of BJT and FET networks is the solution of simultaneous equations established by the device and the network. The solution can be determined using a mathematical or graphical approach—a fact to be demonstrated by the first few networks to be analyzed. However, as noted earlier, the graphical approach is the most popular for FET networks and is employed in this book.

The first few sections of this chapter are limited to JFETs and the graphical approach to analysis. The depletion-type MOSFET will then be examined with its increased range of operating points, followed by the enhancement-type MOSFET. Finally, problems of a design nature are investigated to fully test the concepts and procedures introduced in the chapter.

7.2 FIXED-BIAS CONFIGURATION

The simplest of biasing arrangements for the *n*-channel JFET appears in Fig. 7.1. Referred to as the fixed-bias configuration, it is one of the few FET configurations that can be solved just as directly using either a mathematical or a graphical approach. Both

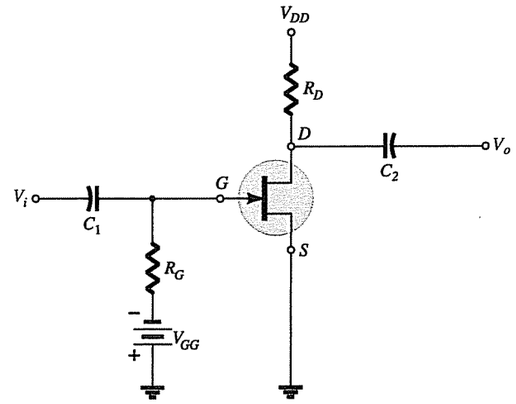


FIG. 7.1
Fixed-bias configuration.

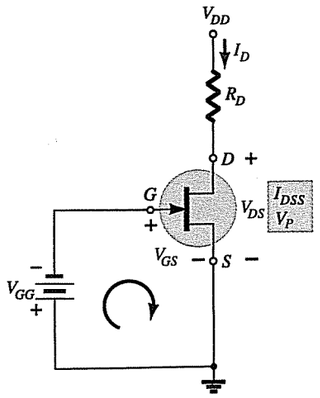


FIG. 7.2
Network for dc analysis.

methods are included in this section to demonstrate the difference between the two philosophies and also to establish the fact that the same solution can be obtained using either method.

The configuration of Fig. 7.1 includes the ac levels V_i and V_o and the coupling capacitors (C_1 and C_2). Recall that the coupling capacitors are "open circuits" for the dc analysis and low impedances (essentially short circuits) for the ac analysis. The resistor R_G is present to ensure that V_i appears at the input to the FET amplifier for the ac analysis (Chapter 8). For the dc analysis,

$$I_G \cong 0\,\text{A}$$

and

$$V_{R_G} = I_G R_G = (0\,\text{A})R_G = 0\,\text{V}$$

The zero-volt drop across R_G permits replacing R_G by a short-circuit equivalent, as appearing in the network of Fig. 7.2, specifically redrawn for the dc analysis.

The fact that the negative terminal of the battery is connected directly to the defined positive potential of V_{GS} clearly reveals that the polarity of V_{GS} is directly opposite to that of V_{GG}. Applying Kirchhoff's voltage law in the clockwise direction of the indicated loop of Fig. 7.2 results in

$$-V_{GG} - V_{GS} = 0$$

and

$$\boxed{V_{GS} = -V_{GG}} \qquad \textbf{(7.5)}$$

Since V_{GG} is a fixed dc supply, the voltage V_{GS} is fixed in magnitude, resulting in the designation "fixed-bias configuration."

The resulting level of drain current I_D is now controlled by Shockley's equation:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Since V_{GS} is a fixed quantity for this configuration, its magnitude and sign can simply be substituted into Shockley's equation and the resulting level of I_D calculated. This is one of the few instances in which a mathematical solution to a FET configuration is quite direct.

A graphical analysis would require a plot of Shockley's equation as shown in Fig. 7.3. Recall that choosing $V_{GS} = V_P/2$ will result in a drain current of $I_{DSS}/4$ when plotting the equation. For the analysis of this chapter, the three points defined by I_{DSS}, V_P, and the intersection just described will be sufficient for plotting the curve.

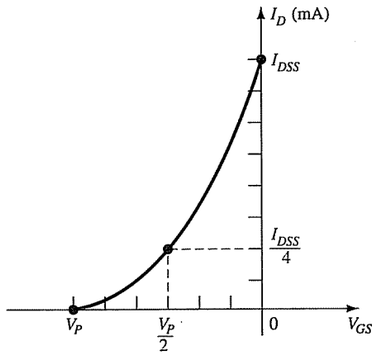


FIG. 7.3
Plotting Shockley's equation.

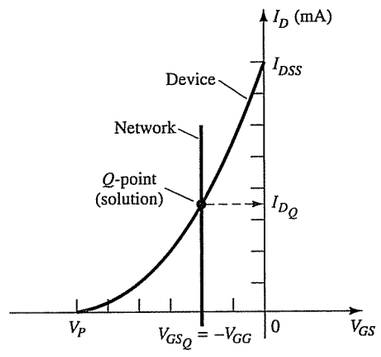


FIG. 7.4
Finding the solution for the fixed-bias configuration.

In Fig. 7.4, the fixed level of V_{GS} has been superimposed as a vertical line at $V_{GS} = -V_{GG}$. At any point on the vertical line, the level of V_{GS} is $-V_{GG}$—the level of I_D must simply be determined on this vertical line. The point where the two curves intersect is the common solution to the configuration—commonly referred to as the *quiescent* or *operating point*. The subscript Q will be applied to drain current and gate-to-source voltage to identify their levels at the Q-point. Note in Fig. 7.4 that the quiescent level of I_D is determined by drawing a horizontal line from the Q-point to the vertical I_D axis. It is important to realize that once the network of Fig. 7.1 is constructed and operating, the dc levels of I_D and V_{GS} that will be measured by the meters of Fig. 7.5 are the quiescent values defined by Fig. 7.4.

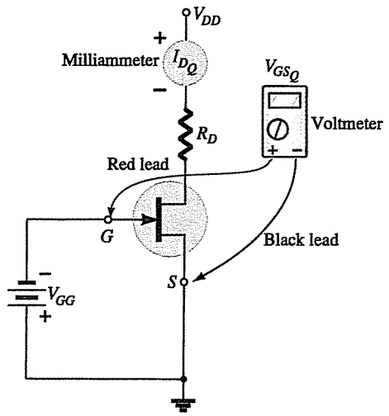


FIG. 7.5
Measuring the quiescent values of I_D and V_{GS}.

The drain-to-source voltage of the output section can be determined by applying Kirchhoff's voltage law as follows:

$$+V_{DS} + I_D R_D - V_{DD} = 0$$

and

$$\boxed{V_{DS} = V_{DD} - I_D R_D} \qquad \textbf{(7.6)}$$

Recall that single-subscript voltages refer to the voltage at a point with respect to ground. For the configuration of Fig. 7.2,

$$\boxed{V_S = 0\,\text{V}} \qquad \textbf{(7.7)}$$

Using double-subscript notation, we have

$$V_{DS} = V_D - V_S$$

or

$$V_D = V_{DS} + V_S = V_{DS} + 0\,\text{V}$$

and

$$\boxed{V_D = V_{DS}} \qquad \textbf{(7.8)}$$

In addition,

$$V_{GS} = V_G - V_S$$

or

$$V_G = V_{GS} + V_S = V_{GS} + 0\,\text{V}$$

and

$$\boxed{V_G = V_{GS}} \qquad \textbf{(7.9)}$$

The fact that $V_D = V_{DS}$ and $V_G = V_{GS}$ is fairly obvious from the fact that $V_S = 0\,\text{V}$, but the derivations above were included to emphasize the relationship that exists between double-subscript and single-subscript notation. Since the configuration requires two dc supplies, its use is limited and will not be included in the forthcoming list of the most common FET configurations.

EXAMPLE 7.1 Determine the following for the network of Fig. 7.6:

PSpice

a. V_{GS_Q}.
b. I_{D_Q}.
c. V_{DS}.
d. V_D.
e. V_G.
f. V_S.

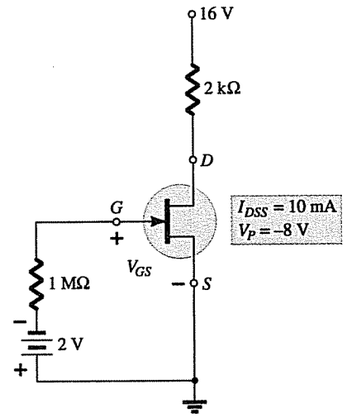


FIG. 7.6
Example 7.1.

Solution:

Mathematical Approach

a. $V_{GS_Q} = -V_{GG} = \mathbf{-2\,V}$

b. $$I_{D_Q} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 10\,\text{mA}\left(1 - \frac{-2\,\text{V}}{-8\,\text{V}}\right)^2$$
$$= 10\,\text{mA}(1 - 0.25)^2 = 10\,\text{mA}(0.75)^2 = 10\,\text{mA}(0.5625)$$
$$= \mathbf{5.625\,mA}$$

c. $$V_{DS} = V_{DD} - I_D R_D = 16\,\text{V} - (5.625\,\text{mA})(2\,\text{k}\Omega)$$
$$= 16\,\text{V} - 11.25\,\text{V} = \mathbf{4.75\,V}$$

d. $V_D = V_{DS} = \mathbf{4.75\,V}$

e. $V_G = V_{GS} = \mathbf{-2\,V}$

f. $V_S = \mathbf{0\,V}$

Graphical Approach The resulting Shockley curve and the vertical line at $V_{GS} = -2\,\text{V}$ are provided in Fig. 7.7. It is certainly difficult to read beyond the second place without significantly increasing the size of the figure, but a solution of 5.6 mA from the graph of Fig. 7.7 is quite acceptable.

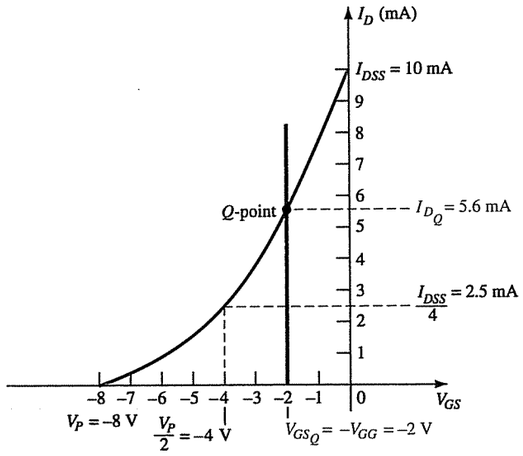


FIG. 7.7
Graphical solution for the network of Fig. 7.6.

a. Therefore,
$$V_{GS_Q} = -V_{GG} = \mathbf{-2\,V}$$

b. $I_{D_Q} = \mathbf{5.6\,mA}$

c. $$V_{DS} = V_{DD} - I_D R_D = 16\,\text{V} - (5.6\,\text{mA})(2\,\text{k}\Omega)$$
$$= 16\,\text{V} - 11.2\,\text{V} = \mathbf{4.8\,V}$$

d. $V_D = V_{DS} = \mathbf{4.8\,V}$

e. $V_G = V_{GS} = \mathbf{-2\,V}$

f. $V_S = \mathbf{0\,V}$

The results clearly confirm the fact that the mathematical and graphical approaches generate solutions that are quite close.

7.3 SELF-BIAS CONFIGURATION

The self-bias configuration eliminates the need for two dc supplies. The controlling gate-to-source voltage is now determined by the voltage across a resistor R_S introduced in the source leg of the configuration as shown in Fig. 7.8.

FIG. 7.8
JFET self-bias configuration.

For the dc analysis, the capacitors can again be replaced by "open circuits" and the resistor R_G replaced by a short-circuit equivalent since $I_G = 0\,\text{A}$. The result is the network of Fig. 7.9 for the important dc analysis.

The current through R_S is the source current I_S, but $I_S = I_D$ and

$$V_{R_S} = I_D R_S$$

For the indicated closed loop of Fig. 7.9, we find that

$$-V_{GS} - V_{R_S} = 0$$

and
$$V_{GS} = -V_{R_S}$$

or
$$\boxed{V_{GS} = -I_D R_S} \qquad \textbf{(7.10)}$$

Note in this case that V_{GS} is a function of the output current I_D and not fixed in magnitude as occurred for the fixed-bias configuration.

Equation (7.10) is defined by the network configuration, and Shockley's equation relates the input and output quantities of the device. Both equations relate the same two variables, permitting either a mathematical or a graphical solution.

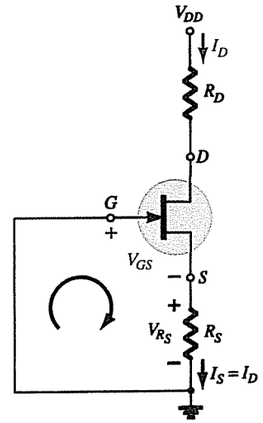


FIG. 7.9
DC analysis of the self-bias configuration.

A mathematical solution could be obtained simply by substituting Eq. (7.10) into Shockley's equation as follows:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= I_{DSS}\left(1 - \frac{-I_D R_S}{V_P}\right)^2$$

or

$$I_D = I_{DSS}\left(1 + \frac{I_D R_S}{V_P}\right)^2$$

By performing the squaring process indicated and rearranging terms, we obtain an equation of the following form:

$$I_D^2 + K_1 I_D + K_2 = 0$$

The quadratic equation can then be solved for the appropriate solution for I_D.

The sequence above defines the mathematical approach. The graphical approach requires that we first establish the device transfer characteristics as shown in Fig. 7.10. Since Eq. (7.10) defines a straight line on the same graph, let us now identify two points on the graph that are on the line and simply draw a straight line between the two points. The most obvious condition to apply is $I_D = 0\,\text{A}$ since it results in $V_{GS} = -I_D R_S = (0\,\text{A})R_S = 0\,\text{V}$. For Eq. (7.10), therefore, one point on the straight line is defined by $I_D = 0\,\text{A}$ and $V_{GS} = 0\,\text{V}$, as appearing on Fig. 7.10.

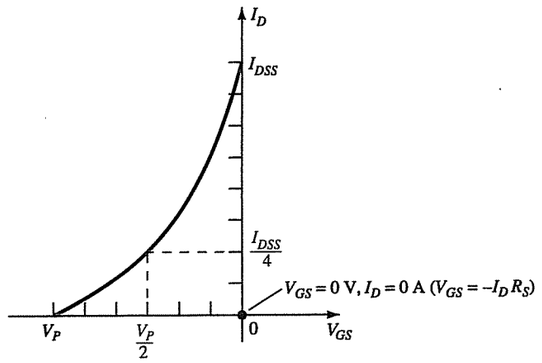


FIG. 7.10
Defining a point on the self-bias line.

The second point for Eq. (7.10) requires that a level of V_{GS} or I_D be chosen and the corresponding level of the other quantity be determined using Eq. (7.10). The resulting levels of I_D and V_{GS} will then define another point on the straight line and permit the drawing of the straight line. Suppose, for example, that we choose a level of I_D equal to one-half the saturation level. That is,

$$I_D = \frac{I_{DSS}}{2}$$

Then

$$V_{GS} = -I_D R_S = -\frac{I_{DSS} R_S}{2}$$

The result is a second point for the straight-line plot as shown in Fig. 7.11. The straight line as defined by Eq. (7.10) is then drawn and the quiescent point obtained at the intersection of the straight-line plot and the device characteristic curve. The quiescent values of I_D and V_{GS} can then be determined and used to find the other quantities of interest.

The level of V_{DS} can be determined by applying Kirchhoff's voltage law to the output circuit, with the result that

$$V_{R_S} + V_{DS} + V_{R_D} - V_{DD} = 0$$

and

$$V_{DS} = V_{DD} - V_{R_S} - V_{R_D} = V_{DD} - I_S R_S - I_D R_D$$

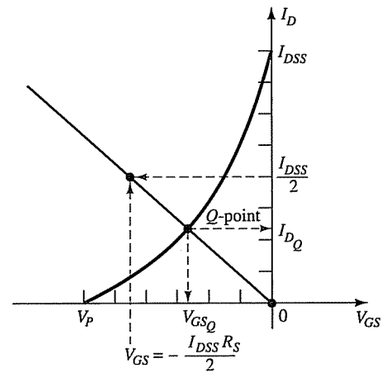


FIG. 7.11
Sketching the self-bias line.

but

$$I_D = I_S$$

and

$$\boxed{V_{DS} = V_{DD} - I_D(R_S + R_D)} \qquad \textbf{(7.11)}$$

In addition,

$$\boxed{V_S = I_D R_S} \qquad \textbf{(7.12)}$$

$$\boxed{V_G = 0\,\text{V}} \qquad \textbf{(7.13)}$$

and

$$\boxed{V_D = V_{DS} + V_S = V_{DD} - V_{R_D}} \qquad \textbf{(7.14)}$$

EXAMPLE 7.2 Determine the following for the network of Fig. 7.12:

a. V_{GS_Q}.
b. I_{D_Q}.
c. V_{DS}.
d. V_S.
e. V_G.
f. V_D.

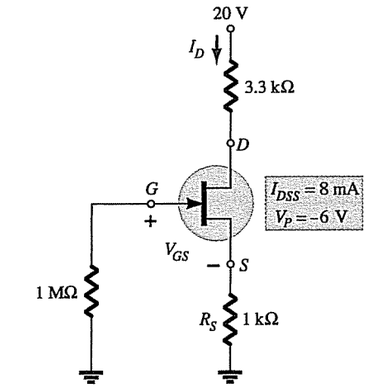


FIG. 7.12
Example 7.2.

Multisim PSpice

Solution:

a. The gate-to-source voltage is determined by

$$V_{GS} = -I_D R_S$$

Choosing $I_D = 4\,\text{mA}$, we obtain

$$V_{GS} = -(4\,\text{mA})(1\,\text{k}\Omega) = -4\,\text{V}$$

The result is the plot of Fig. 7.13 as defined by the network.

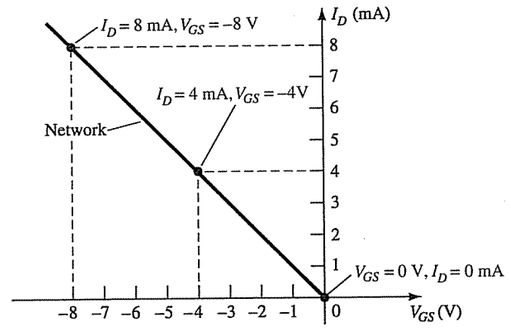


FIG. 7.13
Sketching the self-bias line for the network of Fig. 7.12.

If we happen to choose $I_D = 8$ mA, the resulting value of V_{GS} would be -8 V, as shown on the same graph. In either case, the same straight line will result, clearly demonstrating that any appropriate value of I_D can be chosen as long as the corresponding value of V_{GS} as determined by Eq. (7.10) is employed. In addition, keep in mind that the value of V_{GS} could be chosen and the value of I_D calculated with the same resulting plot.

For Shockley's equation, if we choose $V_{GS} = V_P/2 = -3$ V, we find that $I_D = I_{DSS}/4 = 8\text{ mA}/4 = 2$ mA, and the plot of Fig. 7.14 will result, representing the characteristics of the device. The solution is obtained by superimposing the network characteristics defined by Fig. 7.13 on the device characteristics of Fig. 7.14 and finding the point of intersection of the two as indicated on Fig. 7.15. The resulting operating point results in a quiescent value of gate-to-source voltage of

$$V_{GS_Q} = \mathbf{-2.6\ V}$$

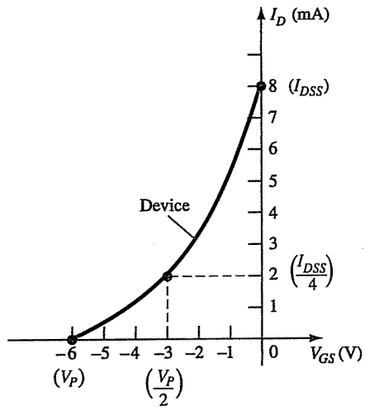


FIG. 7.14
Sketching the device characteristics for the JFET of Fig. 7.12.

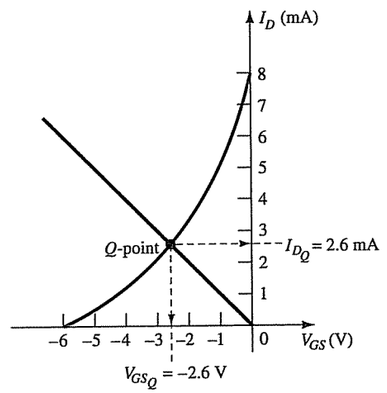


FIG. 7.15
Determining the Q-point for the network of Fig. 7.12.

b. At the quiescent point

$$I_{D_Q} = \mathbf{2.6\ mA}$$

c. Eq. (7.11): $V_{DS} = V_{DD} - I_D(R_S + R_D)$
$= 20\text{ V} - (2.6\text{ mA})(1\text{ k}\Omega + 3.3\text{ k}\Omega)$
$= 20\text{ V} - 11.18\text{ V}$
$= \mathbf{8.82\ V}$

d. Eq. (7.12): $V_S = I_D R_S$
$= (2.6\text{ mA})(1\text{ k}\Omega)$
$= \mathbf{2.6\ V}$

e. Eq. (7.13): $V_G = \mathbf{0\ V}$

f. Eq. (7.14): $V_D = V_{DS} + V_S = 8.82\text{ V} + 2.6\text{ V} = \mathbf{11.42\ V}$
or $V_D = V_{DD} - I_D R_D = 20\text{ V} - (2.6\text{ mA})(3.3\text{ k}\Omega) = \mathbf{11.42\ V}$

Mathcad

Mathcad will now be used to find the quiescent conditions for Example 7.2 using a process described in detail in Section 2.2. The two simultaneous equations that defined the Q-point for the network of Fig. 7.12 are

$$I_D = -\frac{V_{GS}}{R_S} = -\frac{V_{GS}}{1\text{ k}\Omega}$$

and

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 8\text{ mA}\left(1 - \frac{V_{GS}}{-6\text{ V}}\right)^2$$

After calling up Mathcad, we must first provide guesses for the two variables I_D and V_{GS}. The chosen values are 8 mA and -5 V, respectively. Each is entered by first entering the variable followed by **Shift:.** Next, the word **Given** must be entered, followed by the two simultaneous equations using the equal sign obtained from **Ctrl =**. Finally, the variables to be determined must be defined by **Find (ID, VGS)** as shown in Fig. 7.16. The results will appear once the equal sign is entered.

Mathcad returns a value of -2.59 V for **VGS**, which is very close to the calculated level of -2.6 V. In addition, the current of 2.59 mA is very close to the calculated level of 2.6 mA.

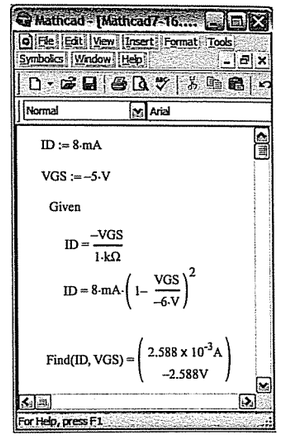


FIG. 7.16
Determining the quiescent point of operation for the network of Example 7.2.

EXAMPLE 7.3 Find the quiescent point for the network of Fig. 7.12 if:

a. $R_S = 100\ \Omega$.
b. $R_S = 10\text{ k}\Omega$.

Solution: Note Fig. 7.17.

a. With the I_D scale,

$$I_{D_Q} \cong \mathbf{6.4\ mA}$$

From Eq. (7.10),

$$V_{GS_Q} \cong \mathbf{-0.64\ V}$$

b. With the V_{GS} scale,

$$V_{GS_Q} \cong \mathbf{-4.6\ V}$$

From Eq. (7.10),

$$I_{D_Q} \cong \mathbf{0.46\ mA}$$

In particular, note how lower levels of R_S bring the load line of the network closer to the I_D axis, whereas increasing levels of R_S bring the load line closer to the V_{GS} axis.

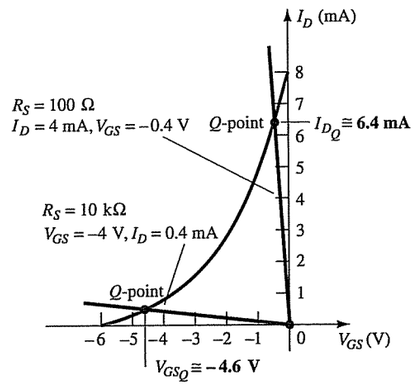


FIG. 7.17
Example 7.3.

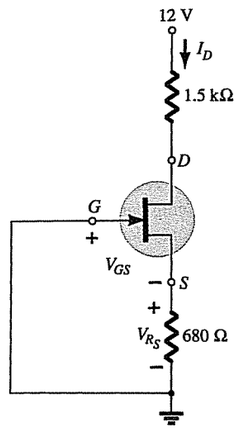


FIG. 7.19
Sketching the dc equivalent of the network of Fig. 7.18.

EXAMPLE 7.4 Determine the following for the common-gate configuration of Fig. 7.18:

a. V_{GS_Q}.
b. I_{D_Q}.
c. V_D.
d. V_G.
e. V_S.
f. V_{DS}.

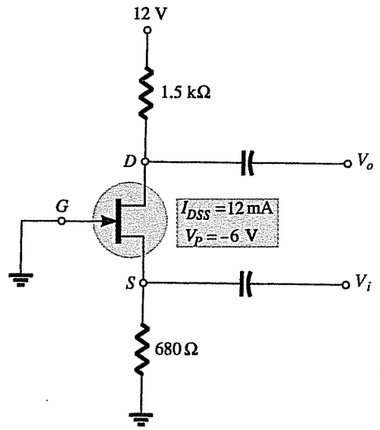


FIG. 7.18
Example 7.4.

Solution: The grounded gate terminal and the location of the input establish strong similarities with the common-base BJT amplifier. Although different in appearance from the basic structure of Fig. 7.8, the resulting dc network of Fig. 7.19 has the same basic structure as Fig. 7.9. The dc analysis can therefore proceed in the same manner as recent examples.

a. The transfer characteristics and load line appear in Fig. 7.20. In this case, the second point for the sketch of the load line is determined by choosing (arbitrarily) $I_D = 6\,\text{mA}$ and solving for V_{GS}. That is,

$$V_{GS} = -I_D R_S = -(6\,\text{mA})(680\,\Omega) = -4.08\,\text{V}$$

as shown in Fig. 7.20. The device transfer curve is sketched using

$$I_D = \frac{I_{DSS}}{4} = \frac{12\,\text{mA}}{4} = 3\,\text{mA}$$

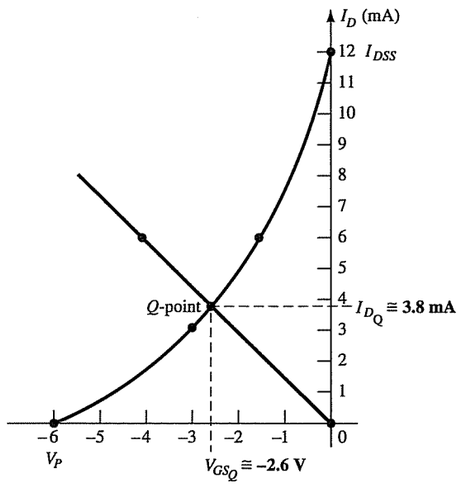


FIG. 7.20
Determining the Q-point for the network of Fig. 7.18.

and the associated value of V_{GS},

$$V_{GS} = \frac{V_P}{2} = -\frac{6\,\text{V}}{2} = -3\,\text{V}$$

as shown on Fig. 7.20. Using the resulting quiescent point of Fig. 7.20 results in

$$V_{GS_Q} \cong \mathbf{-2.6\,V}$$

b. From Fig. 7.20,

$$I_{D_Q} \cong \mathbf{3.8\,mA}$$

c. $V_D = V_{DD} - I_D R_D$
$= 12\,\text{V} - (3.8\,\text{mA})(1.5\,\text{k}\Omega) = 12\,\text{V} - 5.7\,\text{V}$
$= \mathbf{6.3\,V}$

d. $V_G = \mathbf{0\,V}$

e. $V_S = I_D R_S = (3.8\,\text{mA})(680\,\Omega)$
$= \mathbf{2.58\,V}$

f. $V_{DS} = V_D - V_S$
$= 6.3\,\text{V} - 2.58\,\text{V}$
$= \mathbf{3.72\,V}$

7.4 VOLTAGE-DIVIDER BIASING

The voltage-divider bias arrangement applied to BJT transistor amplifiers is also applied to FET amplifiers as demonstrated by Fig. 7.21. The basic construction is exactly the same, but the dc analysis of each is quite different. $I_G = 0\,\text{A}$ for FET amplifiers, but the magnitude of I_B for common-emitter BJT amplifiers can affect the dc levels of current and voltage in both the input and output circuits. Recall that I_B provides the link between input and output circuits for the BJT voltage-divider configuration, whereas V_{GS} does the same for the FET configuration.

The network of Fig. 7.21 is redrawn as shown in Fig. 7.22 for the dc analysis. Note that all the capacitors, including the bypass capacitor C_S, have been replaced by an "open-circuit" equivalent. In addition, the source V_{DD} was separated into two equivalent sources to permit a further separation of the input and output regions of the network. Since $I_G = 0\,\text{A}$, Kirchhoff's current law requires that $I_{R_1} = I_{R_2}$, and the series equivalent circuit appearing to the left of the figure can be used to find the level of V_G. The voltage V_G, equal to the voltage across R_2, can be found using the voltage-divider rule as follows:

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2} \qquad \textbf{(7.15)}$$

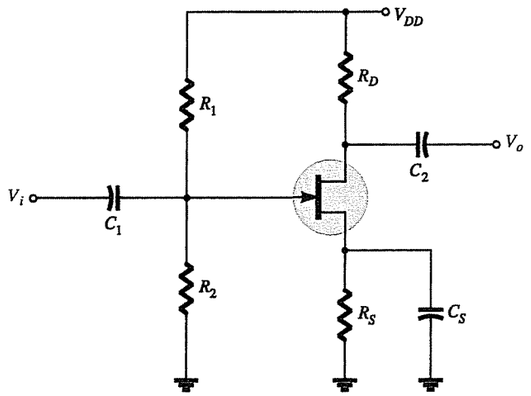


FIG. 7.21
Voltage-divider bias arrangement.

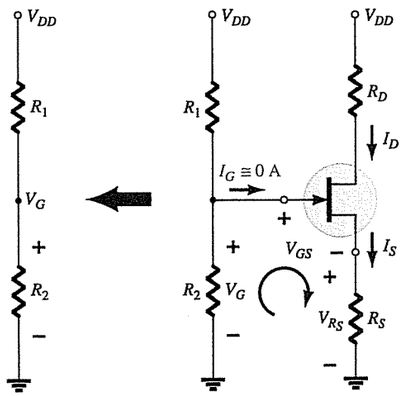


FIG. 7.22
Redrawn network of Fig. 7.21 for dc analysis.

Applying Kirchhoff's voltage law in the clockwise direction to the indicated loop of Fig. 7.22 results in

$$V_G - V_{GS} - V_{R_S} = 0$$

and

$$V_{GS} = V_G - V_{R_S}$$

Substituting $V_{R_S} = I_S R_S = I_D R_S$, we have

$$\boxed{V_{GS} = V_G - I_D R_S} \tag{7.16}$$

The result is an equation that continues to include the same two variables appearing in Shockley's equation: V_{GS} and I_D. The quantities V_G and R_S are fixed by the network construction. Equation (7.16) is still the equation for a straight line, but the origin is no longer a point in the plotting of the line. The procedure for plotting Eq. (7.16) is not a difficult one and will proceed as follows. Since any straight line requires two points to be defined, let us first use the fact that anywhere on the horizontal axis of Fig. 7.23 the current $I_D = 0$ mA. If we therefore select I_D to be 0 mA, we are in essence stating that we are somewhere on the horizontal axis. The exact location can be determined simply by substituting $I_D = 0$ mA into Eq. (7.16) and finding the resulting value of V_{GS} as follows:

$$V_{GS} = V_G - I_D R_S$$
$$= V_G - (0\,\text{mA})R_S$$

and

$$\boxed{V_{GS} = V_G|_{I_D = 0\,\text{mA}}} \tag{7.17}$$

The result specifies that whenever we plot Eq. (7.16), if we choose $I_D = 0$ mA, the value of V_{GS} for the plot will be V_G volts. The point just determined appears in Fig. 7.23.

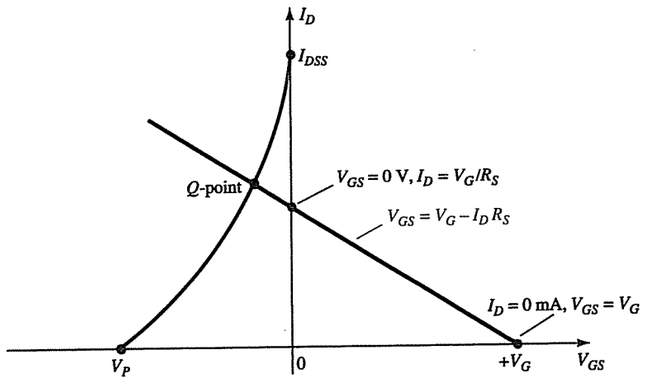


FIG. 7.23
Sketching the network equation for the voltage-divider configuration.

For the other point, let us now employ the fact that at any point on the vertical axis $V_{GS} = 0$ V and solve for the resulting value of I_D:

$$V_{GS} = V_G - I_D R_S$$
$$0\,\text{V} = V_G - I_D R_S$$

and

$$\boxed{I_D = \frac{V_G}{R_S}\bigg|_{V_{GS} = 0\,\text{V}}} \tag{7.18}$$

The result specifies that whenever we plot Eq. (7.16), if $V_{GS} = 0$ V, the level of I_D is determined by Eq. (7.18). This intersection also appears on Fig. 7.23.

The two points defined above permit the drawing of a straight line to represent Eq. (7.16). The intersection of the straight line with the transfer curve in the region to the left of the vertical axis will define the operating point and the corresponding levels of I_D and V_{GS}.

Since the intersection on the vertical axis is determined by $I_D = V_G/R_S$ and V_G is fixed by the input network, increasing values of R_S will reduce the level of the I_D intersection as

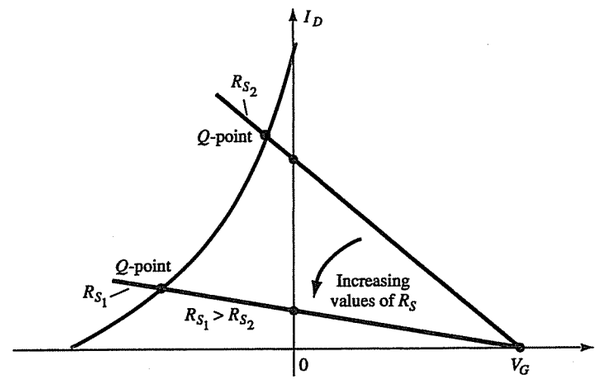


FIG. 7.24
Effect of R_S on the resulting Q-point.

shown in Fig. 7.24. It is fairly obvious from Fig. 7.24 that:

Increasing values of R_S result in lower quiescent values of I_D and more negative values of V_{GS}.

Once the quiescent values of I_{D_Q} and V_{GS_Q} are determined, the remaining network analysis can be performed in the usual manner. That is,

$$\boxed{V_{DS} = V_{DD} - I_D(R_D + R_S)} \tag{7.19}$$

$$\boxed{V_D = V_{DD} - I_D R_D} \tag{7.20}$$

$$\boxed{V_S = I_D R_S} \tag{7.21}$$

$$\boxed{I_{R_1} = I_{R_2} = \frac{V_{DD}}{R_1 + R_2}} \tag{7.22}$$

EXAMPLE 7.5 Determine the following for the network of Fig. 7.25:

a. I_{D_Q} and V_{GS_Q}.
b. V_D.
c. V_S.
d. V_{DS}.
e. V_{DG}.

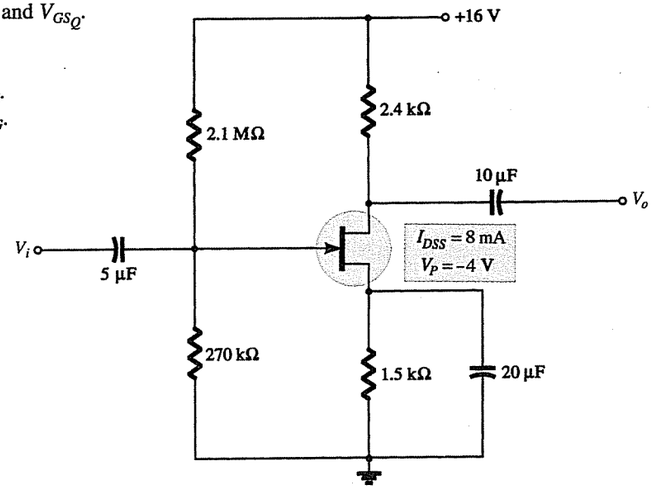


FIG. 7.25
Example 7.5.

Solution:

a. For the transfer characteristics, if $I_D = I_{DSS}/4 = 8\,\text{mA}/4 = 2\,\text{mA}$, then $V_{GS} = V_P/2 = -4\,\text{V}/2 = -2\,\text{V}$. The resulting curve representing Shockley's equation appears in Fig. 7.26. The network equation is defined by

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

$$= \frac{(270\,\text{k}\Omega)(16\,\text{V})}{2.1\,\text{M}\Omega + 0.27\,\text{M}\Omega}$$

$$= 1.82\,\text{V}$$

and

$$V_{GS} = V_G - I_D R_S$$

$$= 1.82\,\text{V} - I_D(1.5\,\text{k}\Omega)$$

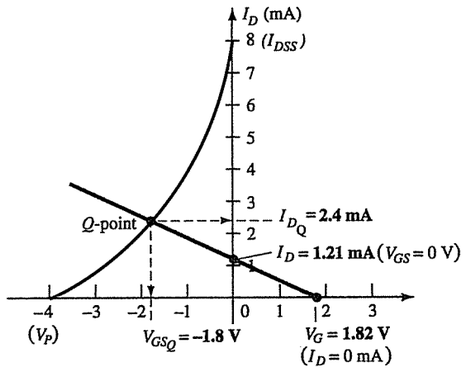


FIG. 7.26
Determining the Q-point for the network of Fig. 7.25.

When $I_D = 0\,\text{mA}$,

$$V_{GS} = +1.82\,\text{V}$$

When $V_{GS} = 0\,\text{V}$,

$$I_D = \frac{1.82\,\text{V}}{1.5\,\text{k}\Omega} = 1.21\,\text{mA}$$

The resulting bias line appears on Fig. 7.26 with quiescent values of

$$I_{D_Q} = \mathbf{2.4\,mA}$$

and

$$V_{GS_Q} = \mathbf{-1.8\,V}$$

b. $V_D = V_{DD} - I_D R_D$

$= 16\,\text{V} - (2.4\,\text{mA})(2.4\,\text{k}\Omega)$

$= \mathbf{10.24\,V}$

c. $V_S = I_D R_S = (2.4\,\text{mA})(1.5\,\text{k}\Omega)$

$= \mathbf{3.6\,V}$

d. $V_{DS} = V_{DD} - I_D(R_D + R_S)$

$= 16\,\text{V} - (2.4\,\text{mA})(2.4\,\text{k}\Omega + 1.5\,\text{k}\Omega)$

$= \mathbf{6.64\,V}$

or $V_{DS} = V_D - V_S = 10.24\,\text{V} - 3.6\,\text{V}$

$= \mathbf{6.64\,V}$

e. Although seldom requested, the voltage V_{DG} can easily be determined using

$$V_{DG} = V_D - V_G$$

$$= 10.24\,\text{V} - 1.82\,\text{V}$$

$$= \mathbf{8.42\,V}$$

Although the basic construction of the network in the next example is quite different from the voltage-divider bias arrangement, the resulting equations require a solution very similar to that just described. Note that the network employs a supply at the drain and the source.

EXAMPLE 7.6 Determine the following for the network of Fig. 7.27:

a. I_{D_Q} and V_{GS_Q}.
b. V_{DS}.
c. V_D.
d. V_S.



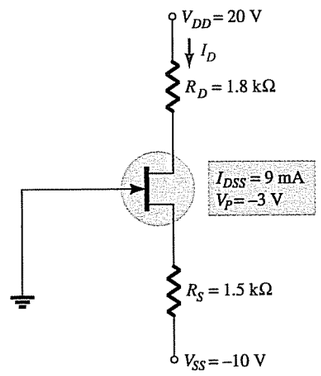


FIG. 7.27
Example 7.6.

Solution:

a. An equation for V_{GS} in terms of I_D is obtained by applying Kirchhoff's voltage law to the input section of the network as redrawn in Fig. 7.28:

$$-V_{GS} - I_S R_S + V_{SS} = 0$$

or

$$V_{GS} = V_{SS} - I_S R_S$$

but

$$I_S = I_D$$

and

$$\boxed{V_{GS} = V_{SS} - I_D R_S} \qquad \textbf{(7.23)}$$

The result is an equation very similar in format to Eq. (7.16) that can be superimposed on the transfer characteristics using the procedure described for Eq. (7.16). That is, for this example,

$$V_{GS} = 10\,\text{V} - I_D(1.5\,\text{k}\Omega)$$

For $I_D = 0\,\text{mA}$,

$$V_{GS} = V_{SS} = 10\,\text{V}$$

For $V_{GS} = 0\,\text{V}$,

$$0 = 10\,\text{V} - I_D(1.5\,\text{k}\Omega)$$

and

$$I_D = \frac{10\,\text{V}}{1.5\,\text{k}\Omega} = 6.67\,\text{mA}$$

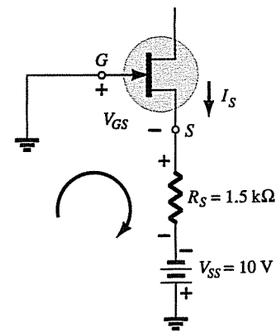


FIG. 7.28
Determining the network equation for the configuration of Fig. 7.27.

The resulting plot points are identified on Fig. 7.29.

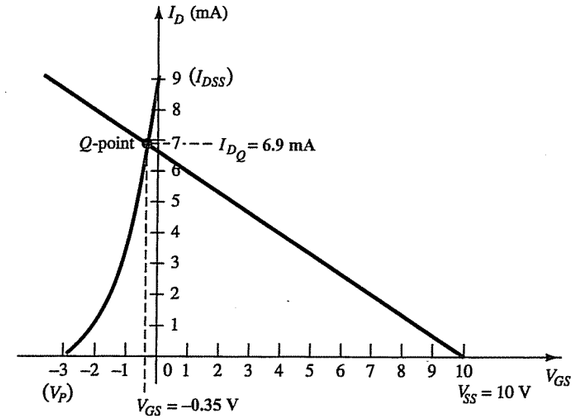


FIG. 7.29
Determining the Q-point for the network of Fig. 7.27.

The transfer characteristics are sketched using the plot point established by $V_{GS} = V_P/2 = -3\text{ V}/2 = -1.5\text{ V}$ and $I_D = I_{DSS}/4 = 9\text{ mA}/4 = 2.25\text{ mA}$, as also appearing on Fig. 7.29. The resulting operating point establishes the following quiescent levels:

$$I_{D_Q} = \mathbf{6.9\text{ mA}}$$
$$V_{GS_Q} = \mathbf{-0.35\text{ V}}$$

b. Applying Kirchhoff's voltage law to the output side of Fig. 7.27 results in

$$-V_{SS} + I_S R_S + V_{DS} + I_D R_D - V_{DD} = 0$$

Substituting $I_S = I_D$ and rearranging gives

$$\boxed{V_{DS} = V_{DD} + V_{SS} - I_D(R_D + R_S)} \qquad \textbf{(7.24)}$$

which for this example results in

$$V_{DS} = 20\text{ V} + 10\text{ V} - (6.9\text{ mA})(1.8\text{ k}\Omega + 1.5\text{ k}\Omega)$$
$$= 30\text{ V} - 22.77\text{ V}$$
$$= \mathbf{7.23\text{ V}}$$

c. $$V_D = V_{DD} - I_D R_D$$
$$= 20\text{ V} - (6.9\text{ mA})(1.8\text{ k}\Omega) = 20\text{ V} - 12.42\text{ V}$$
$$= \mathbf{7.58\text{ V}}$$

d. $$V_{DS} = V_D - V_S$$
or $$V_S = V_D - V_{DS}$$
$$= 7.58\text{ V} - 7.23\text{ V}$$
$$= \mathbf{0.35\text{ V}}$$

7.5 DEPLETION-TYPE MOSFETs

The similarities in appearance between the transfer curves of JFETs and depletion-type MOSFETs permit a similar analysis of each in the dc domain. The primary difference between the two is the fact that depletion-type MOSFETs permit operating points with positive values of V_{GS} and levels of I_D that exceed I_{DSS}. In fact, for all the configurations discussed thus far, the analysis is the same if the JFET is replaced by a depletion-type MOSFET.

The only undefined part of the analysis is how to plot Shockley's equation for positive values of V_{GS}. How far into the region of positive values of V_{GS} and values of I_D greater than I_{DSS} does the transfer curve have to extend? For most situations, this required range will be fairly well defined by the MOSFET parameters and the resulting bias line of the network. A few examples will reveal the effect of the change in device on the resulting analysis.

EXAMPLE 7.7 For the *n*-channel depletion-type MOSFET of Fig. 7.30, determine:

a. I_{D_Q} and V_{GS_Q}.
b. V_{DS}.

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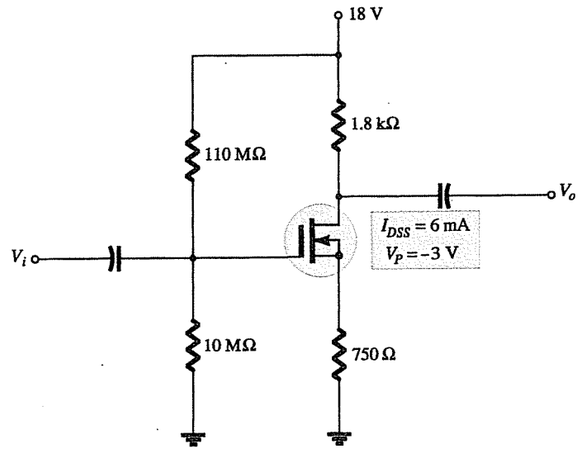


FIG. 7.30
Example 7.7.

Solution:

a. For the transfer characteristics, a plot point is defined by $I_D = I_{DSS}/4 = 6\text{ mA}/4 = 1.5\text{ mA}$ and $V_{GS} = V_P/2 = -3\text{ V}/2 = -1.5\text{ V}$. Considering the level of V_P and the fact that Shockley's equation defines a curve that rises more rapidly as V_{GS} becomes more positive, a plot point will be defined at $V_{GS} = +1\text{ V}$. Substituting into Shockley's equation yields

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$
$$= 6\text{ mA}\left(1 - \frac{+1\text{ V}}{-3\text{ V}}\right)^2 = 6\text{ mA}\left(1 + \frac{1}{3}\right)^2 = 6\text{ mA}(1.778)$$
$$= 10.67\text{ mA}$$

The resulting transfer curve appears in Fig. 7.31. Proceeding as described for JFETs, we have

$$\text{Eq. (7.15):} \quad V_G = \frac{10\text{ M}\Omega(18\text{ V})}{10\text{ M}\Omega + 110\text{ M}\Omega} = 1.5\text{ V}$$
$$\text{Eq. (7.16):} \quad V_{GS} = V_G - I_D R_S = 1.5\text{ V} - I_D(750\ \Omega)$$

Setting $I_D = 0\text{ mA}$ results in

$$V_{GS} = V_G = 1.5\text{ V}$$

Setting $V_{GS} = 0\text{ V}$ yields

$$I_D = \frac{V_G}{R_S} = \frac{1.5\text{ V}}{750\ \Omega} = 2\text{ mA}$$

The plot points and resulting bias line appear in Fig. 7.31. The resulting operating point is given by

$$I_{D_Q} = \mathbf{3.1\text{ mA}}$$
$$V_{GS_Q} = \mathbf{-0.8\text{ V}}$$

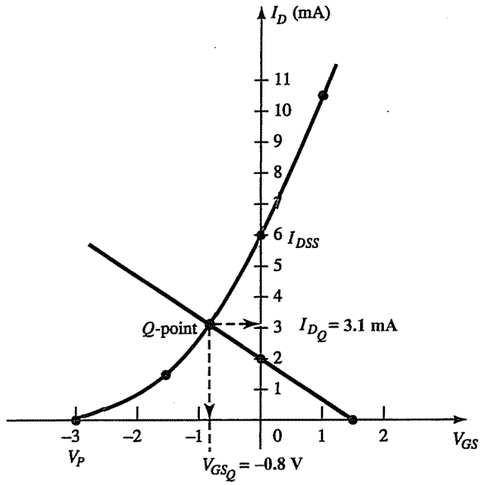


FIG. 7.31
Determining the Q-point for the network of Fig. 7.30.

b. Eq. (7.19):

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$
$$= 18\,\text{V} - (3.1\,\text{mA})(1.8\,\text{k}\Omega + 750\,\Omega)$$
$$\cong \mathbf{10.1\,V}$$

EXAMPLE 7.8 Repeat Example 7.7 with $R_S = 150\,\Omega$.

Solution:

a. The plot points are the same for the transfer curve as shown in Fig. 7.32. For the bias line,

$$V_{GS} = V_G - I_D R_S = 1.5\,\text{V} - I_D(150\,\Omega)$$

Setting $I_D = 0\,\text{mA}$ results in

$$V_{GS} = 1.5\,\text{V}$$

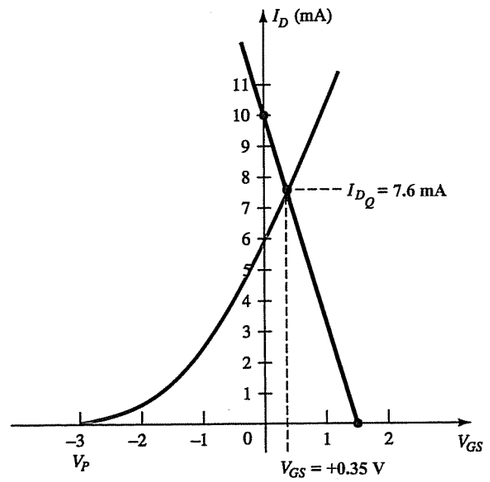


FIG. 7.32
Example 7.8.

Setting $V_{GS} = 0\,\text{V}$ yields

$$I_D = \frac{V_G}{R_S} = \frac{1.5\,\text{V}}{150\,\Omega} = 10\,\text{mA}$$

The bias line is included on Fig. 7.32. Note in this case that the quiescent point results in a drain current that exceeds I_{DSS}, with a positive value for V_{GS}. The result is

$$I_{D_Q} = \mathbf{7.6\,mA}$$
$$V_{GS_Q} = \mathbf{+0.35\,V}$$

b. Eq. (7.19):

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$
$$= 18\,\text{V} - (7.6\,\text{mA})(1.8\,\text{k}\Omega + 150\,\Omega)$$
$$= \mathbf{3.18\,V}$$

EXAMPLE 7.9 Determine the following for the network of Fig. 7.33:

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a. I_{D_Q} and V_{GS_Q}.
b. V_D.

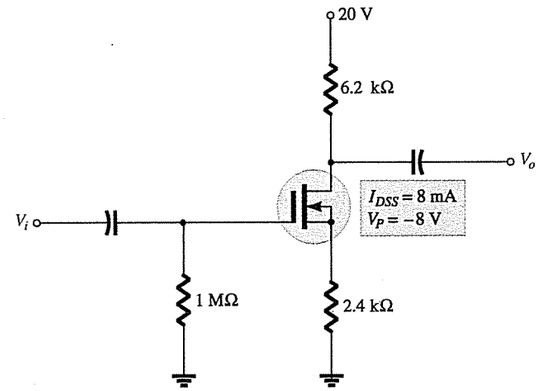


FIG. 7.33
Example 7.9.

Solution:

a. The self-bias configuration results in

$$V_{GS} = -I_D R_S$$

as obtained for the JFET configuration, establishing the fact that V_{GS} must be less than 0 V. There is therefore no requirement to plot the transfer curve for positive values of V_{GS}, although it was done on this occasion to complete the transfer characteristics. A plot point for the transfer characteristics for $V_{GS} < 0\,\text{V}$ is

$$I_D = \frac{I_{DSS}}{4} = \frac{8\,\text{mA}}{4} = 2\,\text{mA}$$

and

$$V_{GS} = \frac{V_P}{2} = \frac{-8\,\text{V}}{2} = -4\,\text{V}$$

and for $V_{GS} > 0\,\text{V}$, since $V_P = -8\,\text{V}$, we will choose

$$V_{GS} = +2\,\text{V}$$

and

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 8\,\text{mA}\left(1 - \frac{+2\,\text{V}}{-8\,\text{V}}\right)^2$$
$$= 12.5\,\text{mA}$$

The resulting transfer curve appears in Fig. 7.34. For the network bias line, at $V_{GS} = 0\,\text{V}$, $I_D = 0\,\text{mA}$. Choosing $V_{GS} = -6\,\text{V}$ gives

$$I_D = -\frac{V_{GS}}{R_S} = -\frac{-6\,\text{V}}{2.4\,\text{k}\Omega} = 2.5\,\text{mA}$$

The resulting Q-point is given by

$$I_{D_Q} = \mathbf{1.7\,mA}$$
$$V_{GS_Q} = \mathbf{-4.3\,V}$$

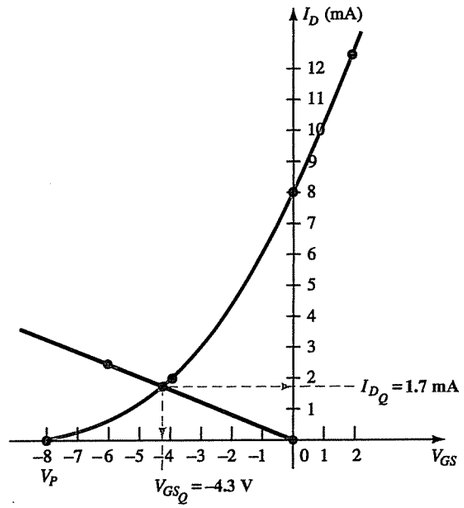


FIG. 7.34
Determining the Q-point for the network of Fig. 7.33.

b. $V_D = V_{DD} - I_D R_D$
$= 20\,\text{V} - (1.7\,\text{mA})(6.2\,\text{k}\Omega)$
$= \mathbf{9.46\,V}$

The example to follow employs a design that can also be applied to JFET transistors. At first impression it appears rather simplistic, but in fact it often causes some confusion when first analyzed due to the special point of operation.

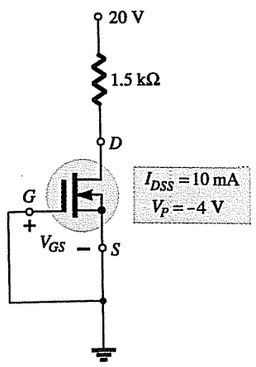


FIG. 7.35
Example 7.10.

EXAMPLE 7.10 Determine V_{DS} for the network of Fig. 7.35.

Solution: The direct connection between the gate and source terminals requires that

$$V_{GS} = 0\,\text{V}$$

Since V_{GS} is fixed at 0 V, the drain current must be I_{DSS} (by definition). In other words,

$$V_{GS_Q} = \mathbf{0\,V}$$

and

$$I_{D_Q} = \mathbf{10\,mA}$$

There is therefore no need to draw the transfer curve, and

$$V_D = V_{DD} - I_D R_D = 20\,\text{V} - (10\,\text{mA})(1.5\,\text{k}\Omega)$$
$$= 20\,\text{V} - 15\,\text{V}$$
$$= \mathbf{5\,V}$$

7.6 ENHANCEMENT-TYPE MOSFETs

The transfer characteristics of the enhancement-type MOSFET are quite different from those encountered for the JFET and depletion-type MOSFETs, resulting in a graphical solution quite different from those of the preceding sections. First and foremost, recall that for the *n*-channel enhancement-type MOSFET, the drain current is zero for levels of gate-to-source voltage less than the threshold level $V_{GS(\text{Th})}$, as shown in Fig. 7.36. For levels of V_{GS} greater than $V_{GS(\text{Th})}$, the drain current is defined by

$$\boxed{I_D = k(V_{GS} - V_{GS(\text{Th})})^2} \qquad \textbf{(7.25)}$$

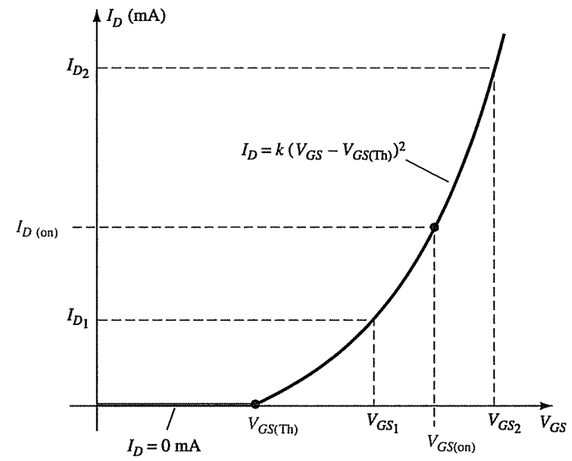


FIG. 7.36
Transfer characteristics of an n-channel enhancement-type MOSFET.

Since specification sheets typically provide the threshold voltage and a level of drain current ($I_{D(\text{on})}$) and its corresponding level of $V_{GS(\text{on})}$, two points are defined immediately as shown in Fig. 7.36. To complete the curve, the constant k of Eq. (7.25) must be determined from the specification sheet data by substituting into Eq. (7.25) and solving for k as follows:

$$I_D = k(V_{GS} - V_{GS(\text{Th})})^2$$
$$I_{D(\text{on})} = k(V_{GS(\text{on})} - V_{GS(\text{Th})})^2$$

and

$$\boxed{k = \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_{GS(\text{Th})})^2}} \qquad \textbf{(7.26)}$$

Once k is defined, other levels of I_D can be determined for chosen values of V_{GS}. Typically, a point between $V_{GS(\text{Th})}$ and $V_{GS(\text{on})}$ and one just greater than $V_{GS(\text{on})}$ will provide a sufficient number of points to plot Eq. (7.25) (note I_{D_1} and I_{D_2} on Fig. 7.36).

Feedback Biasing Arrangement

A popular biasing arrangement for enhancement-type MOSFETs is provided in Fig. 7.37. The resistor R_G brings a suitably large voltage to the gate to drive the MOSFET "on." Since $I_G = 0\,\text{mA}$ and $V_{R_G} = 0\,\text{V}$, the dc equivalent network appears as shown in Fig. 7.38.

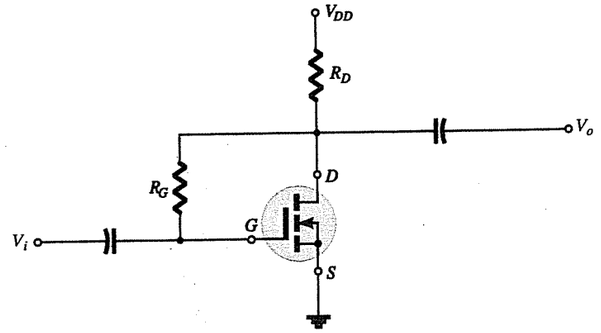


FIG. 7.37
Feedback biasing arrangement.

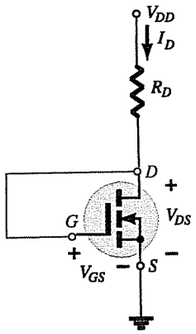


FIG. 7.38
DC equivalent of the network of Fig. 7.37.

A direct connection now exists between drain and gate, resulting in

$$V_D = V_G$$

and

$$\boxed{V_{DS} = V_{GS}} \tag{7.27}$$

For the output circuit,

$$V_{DS} = V_{DD} - I_D R_D$$

which becomes the following after substituting Eq. (7.27):

$$\boxed{V_{GS} = V_{DD} - I_D R_D} \tag{7.28}$$

The result is an equation that relates the same two variables as Eq. (7.25), permitting the plot of both on the same set of axes.

Since Eq. (7.28) is that of a straight line, the same procedure described earlier can be employed to determine the two points that will define the plot on the graph. Substituting $I_D = 0$ mA into Eq. (7.28) gives

$$\boxed{V_{GS} = V_{DD}|_{I_D = 0\,\text{mA}}} \tag{7.29}$$

Substituting $V_{GS} = 0$ V into Eq. (7.28), we have

$$\boxed{I_D = \frac{V_{DD}}{R_D}\bigg|_{V_{GS} = 0\,\text{V}}} \tag{7.30}$$

The plots defined by Eqs. (7.25) and (7.28) appear in Fig. 7.39 with the resulting operating point.

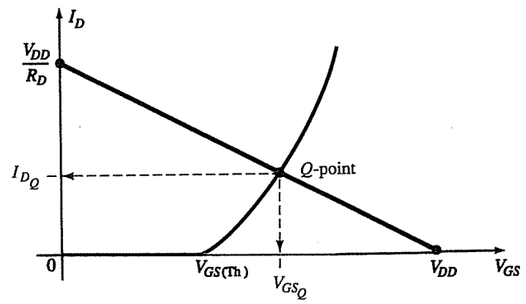


FIG. 7.39
Determining the Q-point for the network of Fig. 7.37.

EXAMPLE 7.11 Determine I_{D_Q} and V_{DS_Q} for the enhancement-type MOSFET of Fig. 7.40.

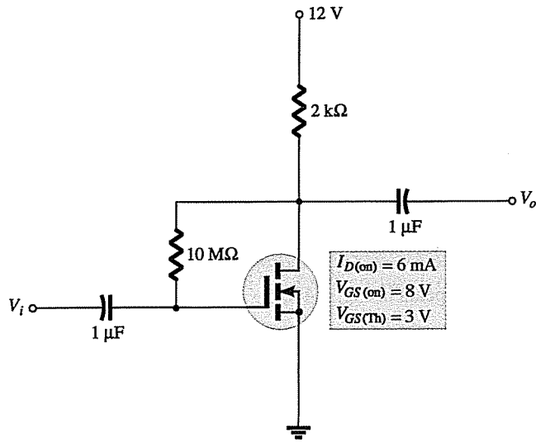


FIG. 7.40
Example 7.11.

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Solution:

Plotting the Transfer Curve Two points are defined immediately as shown in Fig. 7.41. Solving for k, we obtain

$$\text{Eq. (7.26):} \quad k = \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_{GS(\text{Th})})^2}$$

$$= \frac{6\,\text{mA}}{(8\,\text{V} - 3\,\text{V})^2} = \frac{6 \times 10^{-3}}{25}\,\text{A/V}^2$$

$$= \mathbf{0.24 \times 10^{-3}\,A/V^2}$$

For $V_{GS} = 6$ V (between 3 and 8 V):

$$I_D = 0.24 \times 10^{-3}(6\,\text{V} - 3\,\text{V})^2 = 0.24 \times 10^{-3}(9)$$

$$= 2.16\,\text{mA}$$

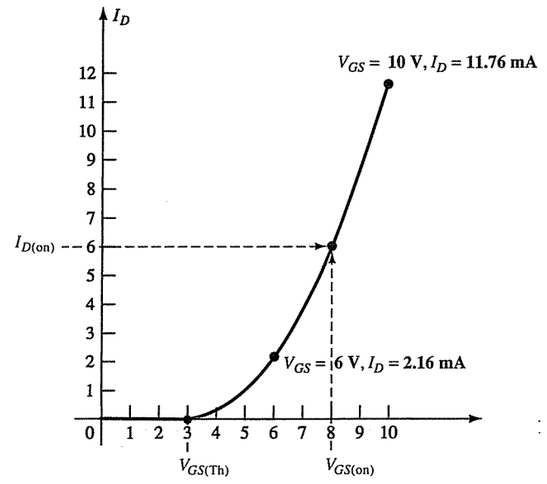


FIG. 7.41
Plotting the transfer curve for the MOSFET of Fig. 7.40.

as shown on Fig. 7.41. For $V_{GS} = 10\,\text{V}$ (slightly greater than $V_{GS(\text{Th})}$),

$$I_D = 0.24 \times 10^{-3}(10\,\text{V} - 3\,\text{V})^2 = 0.24 \times 10^{-3}(49)$$
$$= 11.76\,\text{mA}$$

as also appearing on Fig. 7.41. The four points are sufficient to plot the full curve for the range of interest as shown in Fig. 7.41.

For the Network Bias Line

$$V_{GS} = V_{DD} - I_D R_D$$
$$= 12\,\text{V} - I_D(2\,\text{k}\Omega)$$

Eq. (7.29): $V_{GS} = V_{DD} = 12\,\text{V}|_{I_D = 0\,\text{mA}}$

Eq. (7.30): $I_D = \dfrac{V_{DD}}{R_D} = \dfrac{12\,\text{V}}{2\,\text{k}\Omega} = 6\,\text{mA}|_{V_{GS} = 0\,\text{V}}$

The resulting bias line appears in Fig. 7.42.

At the operating point,

$$I_{D_Q} = \mathbf{2.75\,mA}$$

and

$$V_{GS_Q} = 6.4\,\text{V}$$

with

$$V_{DS_Q} = V_{GS_Q} = \mathbf{6.4\,V}$$

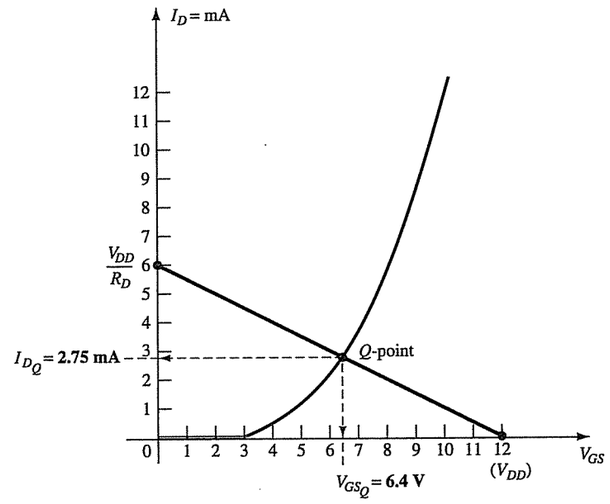


FIG. 7.42
Determining the Q-point for the network of Fig. 7.40.

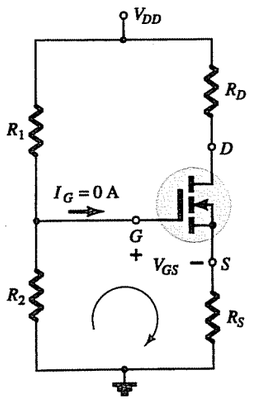


FIG. 7.43
Voltage-divider biasing arrangement for an n-channel enhancement MOSFET.

Voltage-Divider Biasing Arrangement

A second popular biasing arrangement for the enhancement-type MOSFET appears in Fig. 7.43. The fact that $I_G = 0\,\text{mA}$ results in the following equation for V_{GG} as derived from an application of the voltage-divider rule:

$$\boxed{V_G = \frac{R_2 V_{DD}}{R_1 + R_2}} \qquad \textbf{(7.31)}$$

Applying Kirchhoff's voltage law around the indicated loop of Fig. 7.43 results in

$$+V_G - V_{GS} - V_{R_S} = 0$$

and

$$V_{GS} = V_G - V_{R_S}$$

or

$$\boxed{V_{GS} = V_G - I_D R_S} \qquad \textbf{(7.32)}$$

For the output section,

$$V_{R_S} + V_{DS} + V_{R_D} - V_{DD} = 0$$

and

$$V_{DS} = V_{DD} - V_{R_S} - V_{R_D}$$

or

$$\boxed{V_{DS} = V_{DD} - I_D(R_S + R_D)} \qquad \textbf{(7.33)}$$

Since the characteristics are a plot of I_D versus V_{GS} and Eq. (7.32) relates the same two variables, the two curves can be plotted on the same graph and a solution determined at their intersection. Once I_{D_Q} and V_{GS_Q} are known, all the remaining quantities of the network such as V_{DS}, V_D, and V_S can be determined.

EXAMPLE 7.12 Determine I_{D_Q}, V_{GS_Q}, and V_{DS} for the network of Fig. 7.44.

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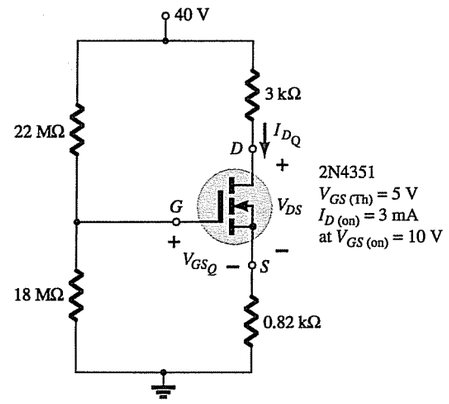


FIG. 7.44
Example 7.12.

Solution:

Network

Eq. (7.31): $V_G = \dfrac{R_2 V_{DD}}{R_1 + R_2} = \dfrac{(18\,\text{M}\Omega)(40\,\text{V})}{22\,\text{M}\Omega + 18\,\text{M}\Omega} = 18\,\text{V}$

Eq. (7.32): $V_{GS} = V_G - I_D R_S = 18\,\text{V} - I_D(0.82\,\text{k}\Omega)$

When $I_D = 0\,\text{mA}$,

$$V_{GS} = 18\,\text{V} - (0\,\text{mA})(0.82\,\text{k}\Omega) = 18\,\text{V}$$

as appearing on Fig. 7.45. When $V_{GS} = 0\,\text{V}$,

$$V_{GS} = 18\,\text{V} - I_D(0.82\,\text{k}\Omega)$$
$$0 = 18\,\text{V} - I_D(0.82\,\text{k}\Omega)$$
$$I_D = \frac{18\,\text{V}}{0.82\,\text{k}\Omega} = 21.95\,\text{mA}$$

as appearing on Fig. 7.45.

Device

$$V_{GS(\text{Th})} = 5\,\text{V}, \qquad I_{D(\text{on})} = 3\,\text{mA with } V_{GS(\text{on})} = 10\,\text{V}$$

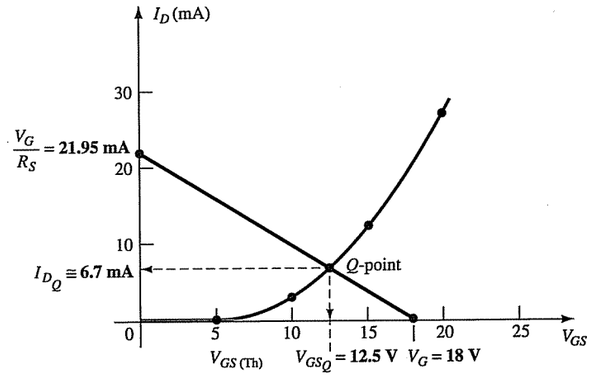


FIG. 7.45
Determining the Q-point for the network of Example 7.12.

Eq. (7.26):
$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS(Th)})^2} = \frac{3\text{ mA}}{(10\text{ V} - 5\text{ V})^2} = 0.12 \times 10^{-3}\text{ A/V}^2$$

and
$$I_D = k(V_{GS} - V_{GS(Th)})^2 = 0.12 \times 10^{-3}(V_{GS} - 5)^2$$

which is plotted on the same graph (Fig. 7.45). From Fig. 7.45,

$$I_{D_Q} \cong \mathbf{6.7\text{ mA}}$$
$$V_{GS_Q} = \mathbf{12.5\text{ V}}$$

Eq. (7.33):
$$V_{DS} = V_{DD} - I_D(R_S + R_D)$$
$$= 40\text{ V} - (6.7\text{ mA})(0.82\,\text{k}\Omega + 3.0\,\text{k}\Omega)$$
$$= 40\text{ V} - 25.6\text{ V}$$
$$= \mathbf{14.4\text{ V}}$$

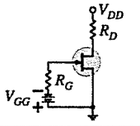
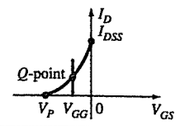
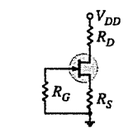
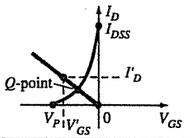
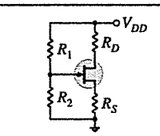
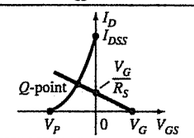
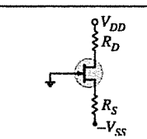
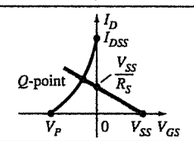
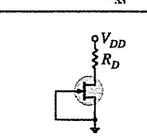
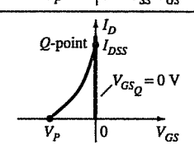
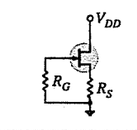
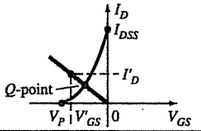
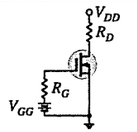
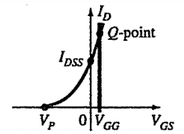
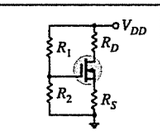
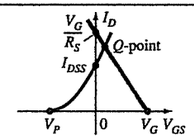
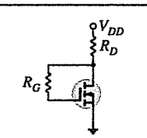
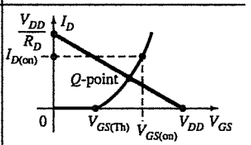
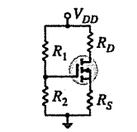
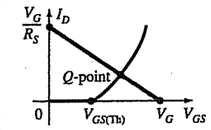
7.7 SUMMARY TABLE

Now that the most popular biasing arrangements for the various FETs have been introduced, Table 7.1 reviews the basic results and demonstrates the similarity in approach for a number of configurations. It also reveals that the general analysis of dc configurations for FETs is not overly complex. Once the transfer characteristics are established, the network self-bias line can be drawn and the *Q*-point determined at the intersection of the device transfer characteristic and the network bias curve. The remaining analysis is simply an application of the basic laws of circuit analysis.

7.8 COMBINATION NETWORKS

Now that the dc analysis of a variety of BJT and FET configurations is established, the opportunity to analyze networks with both types of devices presents itself. Fundamentally, the analysis simply requires that we *first* approach the device that will provide a terminal voltage or current level. The door is then usually open to calculating other quantities and concentrating on the remaining unknowns. These are usually particularly interesting problems due to the challenge of finding the opening and then using the results of the past few sections and Chapter 4 to find the important quantities for each device. The equations and relationships used are simply those we have employed on more than one occasion—there is no need to develop any new methods of analysis.

TABLE 7.1
FET Bias Configurations

Type	Configuration	Pertinent Equations	Graphical Solution
JFET Fixed-bias		$V_{GS_Q} = -V_{GG}$ $V_{DS} = V_{DD} - I_D R_S$	
JFET Self-bias		$V_{GS} = -I_D R_S$ $V_{DS} = V_{DD} - I_D(R_D + R_S)$	
JFET Voltage-divider bias		$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$ $V_{GS} = V_G - I_D R_S$ $V_{DS} = V_{DD} - I_D(R_D + R_S)$	
JFET Common-gate		$V_{GS} = V_{SS} - I_D R_S$ $V_{DS} = V_{DD} + V_{SS} - I_D(R_D + R_S)$	
JFET ($V_{GS_Q} = 0$ V)		$V_{GS_Q} = 0$ V $I_{D_Q} = I_{DSS}$	
JFET ($R_D = 0\ \Omega$)		$V_{GS} = -I_D R_S$ $V_D = V_{DD}$ $V_S = I_D R_S$ $V_{DS} = V_{DD} - I_S R_S$	
Depletion-type MOSFET Fixed-bias (and MESFETs)		$V_{GS_Q} = +V_{GG}$ $V_{DS} = V_{DD} - I_D R_S$	
Depletion-type MOSFET Voltage-divider bias (and MESFETs)		$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$ $V_{GS} = V_G - I_S R_S$ $V_{DS} = V_{DD} - I_D(R_D + R_S)$	
Enhancement type MOSFET Feedback configuration (and MESFETs)		$V_{GS} = V_{DS}$ $V_{GS} = V_{DD} - I_D R_D$	
Enhancement type MOSFET Voltage-divider bias (and MESFETs)		$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$ $V_{GS} = V_G - I_D R_S$	

EXAMPLE 7.13 Determine the levels of V_D and V_C for the network of Fig. 7.46.



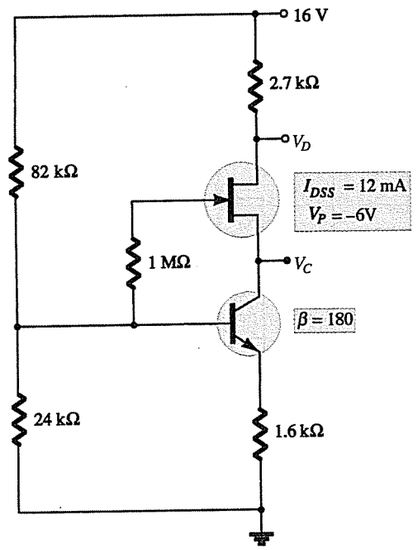


FIG. 7.46
Example 7.13.

Solution: From experience we now realize that V_{GS} is typically an important quantity to determine or write an equation for when analyzing JFET networks. Since V_{GS} is a level for which an immediate solution is not obvious, let us turn our attention to the transistor configuration. The voltage-divider configuration is one where the approximate technique can be applied ($\beta R_E = 180 \times 1.6\,\text{k}\Omega = 288\,\text{k}\Omega > 10R_2 = 240\,\text{k}\Omega$), permitting a determination of V_B using the voltage-divider rule on the input circuit.

For V_B,

$$V_B = \frac{24\,\text{k}\Omega(16\,\text{V})}{82\,\text{k}\Omega + 24\,\text{k}\Omega} = 3.62\,\text{V}$$

Using the fact that $V_{BE} = 0.7\,\text{V}$ results in

$$V_E = V_B - V_{BE} = 3.62\,\text{V} - 0.7\,\text{V}$$
$$= 2.92\,\text{V}$$

and

$$I_E = \frac{V_{RE}}{R_E} = \frac{V_E}{R_E} = \frac{2.92\,\text{V}}{1.6\,\text{k}\Omega} = 1.825\,\text{mA}$$

with

$$I_C \cong I_E = 1.825\,\text{mA}$$

Continuing, we find for this configuration that

$$I_D = I_S = I_C$$

and

$$V_D = 16\,\text{V} - I_D(2.7\,\text{k}\Omega)$$
$$= 16\,\text{V} - (1.825\,\text{mA})(2.7\,\text{k}\Omega) = 16\,\text{V} - 4.93\,\text{V}$$
$$= \mathbf{11.07\,V}$$

The question of how to determine V_C is not as obvious. Both V_{CE} and V_{DS} are unknown quantities, preventing us from establishing a link between V_D and V_C or from V_E to V_D. A more careful examination of Fig. 7.46 reveals that V_C is linked to V_B by V_{GS} (assuming that $V_{R_G} = 0\,\text{V}$). Since we know V_B if we can find V_{GS}, V_C can be determined from

$$V_C = V_B - V_{GS}$$

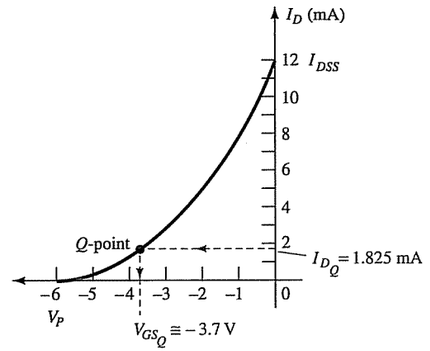


FIG. 7.47
Determining the Q-point for the network of Fig. 7.46.

The question then arises as to how to find the level of V_{GS_Q} from the quiescent value of I_D. The two are related by Shockley's equation:

$$I_{D_Q} = I_{DSS}\left(1 - \frac{V_{GS_Q}}{V_P}\right)^2$$

and V_{GS_Q} could be found mathematically by solving for V_{GS_Q} and substituting numerical values. However, let us turn to the graphical approach and simply work in the reverse order employed in the preceding sections. The JFET transfer characteristics are first sketched as shown in Fig. 7.47. The level of I_{D_Q} is then established by a horizontal line as shown in the same figure. V_{GS_Q} is then determined by dropping a line down from the operating point to the horizontal axis, resulting in

$$V_{GS_Q} = \mathbf{-3.7\,V}$$

The level of V_C is given by

$$V_C = V_B - V_{GS_Q} = 3.62\,\text{V} - (-3.7\,\text{V})$$
$$= \mathbf{7.32\,V}$$

EXAMPLE 7.14 Determine V_D for the network of Fig. 7.48.



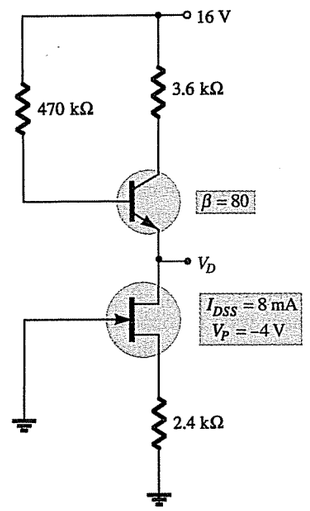


FIG. 7.48
Example 7.14.

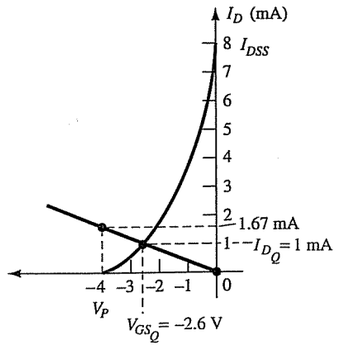


FIG. 7.49
Determining the Q-point for the network of Fig. 7.48.

Solution: In this case, there is no obvious path for determining a voltage or current level for the transistor configuration. However, turning to the self-biased JFET, we can derive an equation for V_{GS} and determine the resulting quiescent point using graphical techniques. That is,

$$V_{GS} = -I_D R_S = -I_D(2.4\,\text{k}\Omega)$$

resulting in the self-bias line appearing in Fig. 7.49, which establishes a quiescent point at

$$V_{GS_Q} = -2.6\,\text{V}$$
$$I_{D_Q} = 1\,\text{mA}$$

For the transistor,

$$I_E \cong I_C = I_D = 1\,\text{mA}$$

and

$$I_B = \frac{I_C}{\beta} = \frac{1\,\text{mA}}{80} = 12.5\,\mu\text{A}$$

$$V_B = 16\,\text{V} - I_B(470\,\text{k}\Omega)$$
$$= 16\,\text{V} - (12.5\,\mu\text{A})(470\,\text{k}\Omega) = 16\,\text{V} - 5.875\,\text{V}$$
$$= 10.125\,\text{V}$$

and

$$V_E = V_D = V_B - V_{BE}$$
$$= 10.125\,\text{V} - 0.7\,\text{V}$$
$$= \mathbf{9.425\,V}$$

7.9 DESIGN

The design process is not limited solely to dc conditions. The area of application, level of amplification desired, signal strength, and operating conditions are just a few of the conditions that enter into the total design process. However, we first concentrate on establishing the chosen dc conditions.

For example, if the levels of V_D and I_D are specified for the network of Fig. 7.50, the level of V_{GS_Q} can be determined from a plot of the transfer curve and R_S can then be determined from $V_{GS} = -I_D R_S$. If V_{DD} is specified, the level of R_D can then be calculated from $R_D = (V_{DD} - V_D)/I_D$. Of course, the values of R_S and R_D may not be standard commercial values, requiring that the nearest commercial values be employed. However, with the tolerance (range of values) normally specified for the parameters of a network, the slight variation due to the choice of standard values will seldom cause a real concern in the design process.

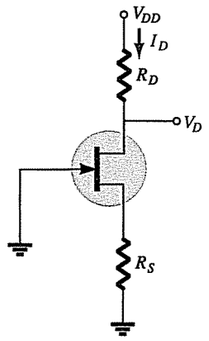


FIG. 7.50
Self-bias configuration to be designed.

The above is only one possibility for the design phase involving the network of Fig. 7.50. It is possible that only V_{DD} and R_D are specified together with the level of V_{DS}. The device to be employed may have to be specified along with the level of R_S. It appears logical that the device chosen should have a maximum V_{DS} greater than the specified value by a safe margin.

In general, it is good design practice for linear amplifiers to choose operating points that do not crowd the saturation level (I_{DSS}) or cutoff (V_P) regions. Levels of V_{GS_Q} close to $V_P/2$ or levels of I_{D_Q} near $I_{DSS}/2$ are certainly reasonable starting points in the design. Of course, in every design procedure the maximum levels of I_D and V_{DS} as appearing on the specification sheet must not be exceeded.

The examples to follow have a design or synthesis orientation in that specific levels are provided and network parameters such as R_D, R_S, V_{DD}, and so on, must be determined. In any case, the approach is in many ways the opposite of that described in previous sections. In some cases, it is just a matter of applying Ohm's law in its appropriate form. In particular, if resistive levels are requested, the result is often obtained simply by applying Ohm's law in the following form:

$$R_{\text{unknown}} = \frac{V_R}{I_R} \qquad \textbf{(7.34)}$$

where V_R and I_R are often parameters that can be found directly from the specified voltage and current levels.

EXAMPLE 7.15 For the network of Fig. 7.51, the levels of V_{D_Q} and I_{D_Q} are specified. Determine the required values of R_D and R_S. What are the closest standard commercial values?

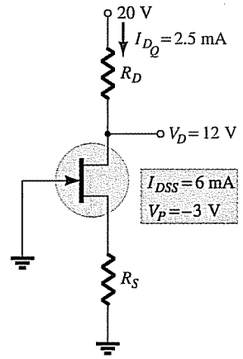


FIG. 7.51
Example 7.15.

Solution: As defined by Eq. (7.34),

$$R_D = \frac{V_{R_D}}{I_{D_Q}} = \frac{V_{DD} - V_{D_Q}}{I_{D_Q}}$$

and

$$= \frac{20\,\text{V} - 12\,\text{V}}{2.5\,\text{mA}} = \frac{8\,\text{V}}{2.5\,\text{mA}} = \mathbf{3.2\,k\Omega}$$

Plotting the transfer curve in Fig. 7.52 and drawing a horizontal line at $I_{D_Q} = 2.5$ mA results in $V_{GS_Q} = -1$ V, and applying $V_{GS} = -I_D R_S$ establishes the level of R_S:

$$R_S = \frac{-(V_{GS_Q})}{I_{D_Q}} = \frac{-(-1\,\text{V})}{2.5\,\text{mA}} = \mathbf{0.4\,k\Omega}$$

The nearest standard commercial values are

$$R_D = 3.2\,\text{k}\Omega \Rightarrow \mathbf{3.3\,k\Omega}$$
$$R_S = 0.4\,\text{k}\Omega \Rightarrow \mathbf{0.39\,k\Omega}$$

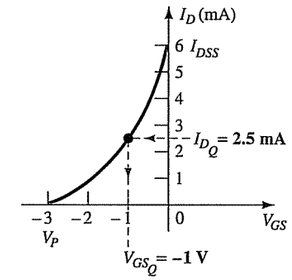


FIG. 7.52
Determining V_{GS_Q} for the network of Fig. 7.51.

EXAMPLE 7.16 For the voltage-divider bias configuration of Fig. 7.53, if $V_D = 12$ V and $V_{GS_Q} = -2$ V, determine the value of R_S.

Solution: The level of V_G is determined as follows:

$$V_G = \frac{47\,\text{k}\Omega(16\,\text{V})}{47\,\text{k}\Omega + 91\,\text{k}\Omega} = 5.44\,\text{V}$$

with

$$I_D = \frac{V_{DD} - V_D}{R_D}$$
$$= \frac{16\,\text{V} - 12\,\text{V}}{1.8\,\text{k}\Omega} = 2.22\,\text{mA}$$

The equation for V_{GS} is then written and the known values substituted:

$$V_{GS} = V_G - I_D R_S$$
$$-2\,\text{V} = 5.44\,\text{V} - (2.22\,\text{mA})R_S$$
$$-7.44\,\text{V} = -(2.22\,\text{mA})R_S$$

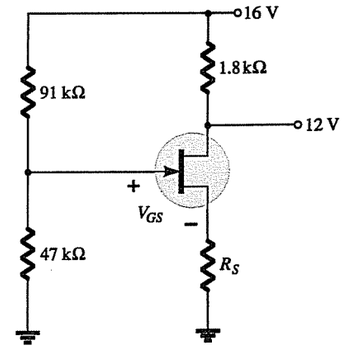


FIG. 7.53
Example 7.16.

and $$R_S = \frac{7.44\text{ V}}{2.22\text{ mA}} = \mathbf{3.35\ k\Omega}$$

The nearest standard commercial value is 3.3 kΩ.

EXAMPLE 7.17 The levels of V_{DS} and I_D are specified as $V_{DS} = \frac{1}{2}V_{DD}$ and $I_D = I_{D(on)}$ for the network of Fig. 7.54. Determine the levels of V_{DD} and R_D.

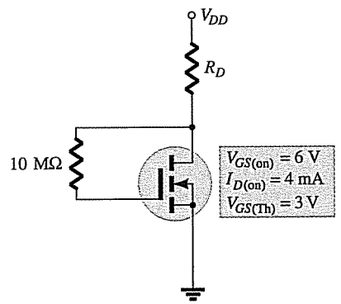


FIG. 7.54
Example 7.17.

Solution: Given $I_D = I_{D(on)} = 4$ mA and $V_{GS} = V_{GS(on)} = 6$ V, for this configuration,

$$V_{DS} = V_{GS} = \tfrac{1}{2}V_{DD}$$

and $$6\text{ V} = \tfrac{1}{2}V_{DD}$$

so that $$V_{DD} = \mathbf{12\ V}$$

Applying Eq. (7.34) yields

$$R_D = \frac{V_{R_D}}{I_D} = \frac{V_{DD} - V_{DS}}{I_{D(on)}} = \frac{V_{DD} - \frac{1}{2}V_{DD}}{I_{D(on)}} = \frac{\frac{1}{2}V_{DD}}{I_{D(on)}}$$

and $$R_D = \frac{6\text{ V}}{4\text{ mA}} = \mathbf{1.5\ k\Omega}$$

which is a standard commercial value.

7.10 TROUBLESHOOTING

How often has a network been carefully constructed only to find that when the power is applied, the response is totally unexpected and fails to match the theoretical calculations. What is the next step? Is it a bad connection? A misreading of the color code for a resistive element? An error in the construction process? The range of possibilities seems vast and often frustrating. The troubleshooting process first described in the analysis of BJT transistor configurations should narrow down the list of possibilities and isolate the problem area following a definite plan of attack. In general, the process begins with a rechecking of the network construction and the terminal connections. This is usually followed by the checking of voltage levels between specific terminals and ground or between terminals of the network. Seldom are current levels measured since such maneuvers require disturbing the network structure to insert the meter. Of course, once the voltage levels are obtained, current levels can be calculated using Ohm's law. In any case, some idea of the expected voltage or current level must be known for the measurement to have any importance. In total, therefore, the troubleshooting process can begin with some hope of success only if the basic operation of the network is understood along with some expected levels of voltage or current. For the *n*-channel JFET amplifier, it is clearly understood that the quiescent value of V_{GS_Q} is limited to 0 V or a negative voltage. For the network of Fig. 7.55, V_{GS_Q} is limited to negative values in the range 0 V to V_P. If a meter is hooked up as shown in Fig. 7.55, with the positive lead (normally red) to the gate and the negative lead (usually black) to the source, the resulting reading should have a negative sign and a magnitude of a few volts. Any other response should be considered suspicious and needs to be investigated.

The level of V_{DS} is typically between 25% and 75% of V_{DD}. A reading of 0 V for V_{DS} clearly indicates that either the output circuit has an "open" or the JFET is internally short-circuited between drain and source. If V_D is V_{DD} volts, there is obviously no drop across R_D, due to the lack of current through R_D, and the connections should be checked for continuity.

If the level of V_{DS} seems inappropriate, the continuity of the output circuit can easily be checked by grounding the negative lead of the voltmeter and measuring the voltage levels from V_{DD} to ground using the positive lead. If $V_D = V_{DD}$, the current through R_D may be zero, but there is continuity between V_D and V_{DD}. If $V_S = V_{DD}$, the device is not open between drain and source, but it is also not "on." The continuity through to V_S is confirmed, however. In this case, it is possible that there is a poor ground connection between R_S and ground that may not be obvious. The internal connection between the wire of the lead and the terminal connector may have separated. Other possibilities also exist, such as a shorted device from drain to source, but the troubleshooter will simply have to narrow down the possible causes for the malfunction.

The continuity of a network can also be checked simply by measuring the voltage across any resistor of the network (except for R_G in the JFET configuration). An indication of 0 V immediately reveals the lack of current through the element due to an open circuit in the network.

The most sensitive element in the BJT and JFET configurations is the amplifier itself. The application of excessive voltage during the construction or testing phase or the use of incorrect resistor values resulting in high current levels can destroy the device. If you question the condition of the amplifier, the best test for the FET is the curve tracer since it not only reveals whether the device is operable, but also its range of current and voltage levels. Some testers may reveal that the device is still fundamentally sound but do not reveal whether its range of operation has been severely reduced.

The development of good troubleshooting techniques comes primarily from experience and a level of confidence in what to expect and why. There are, of course, times when the reasons for a strange response seem to disappear mysteriously when you check a network. In such cases, it is best not to breathe a sigh of relief and continue with the construction. The cause for such a sensitive "make or break" situation should be found and corrected, or it may reoccur at the most inopportune moment.

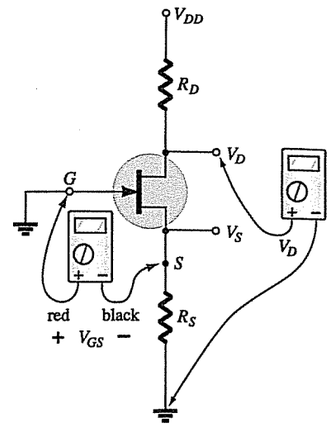


FIG. 7.55
Checking the dc operation of the JFET self-bias configuration.

7.11 *p*-CHANNEL FETs

The analysis thus far has been limited solely to *n*-channel FETs. For *p*-channel FETs, a mirror image of the transfer curves is employed, and the defined current directions are reversed as shown in Fig. 7.56 for the various types of FETs.

Note for each configuration of Fig. 7.56 that each supply voltage is now a negative voltage drawing current in the indicated direction. In particular, note that the double-subscript notation for voltages continues as defined for the *n*-channel device: V_{GS}, V_{DS}, and so on. In this case, however, V_{GS} is positive (positive or negative for the depletion-type MOSFET) and V_{DS} negative.

Due to the similarities between the analysis of *n*-channel and *p*-channel devices, one can assume an *n*-channel device and reverse the supply voltage and perform the entire analysis. When the results are obtained, the magnitude of each quantity will be correct, although the current direction and voltage polarities will have to be reversed. However, the next example will demonstrate that with the experience gained through the analysis of *n*-channel devices, the analysis of *p*-channel devices is quite straightforward.

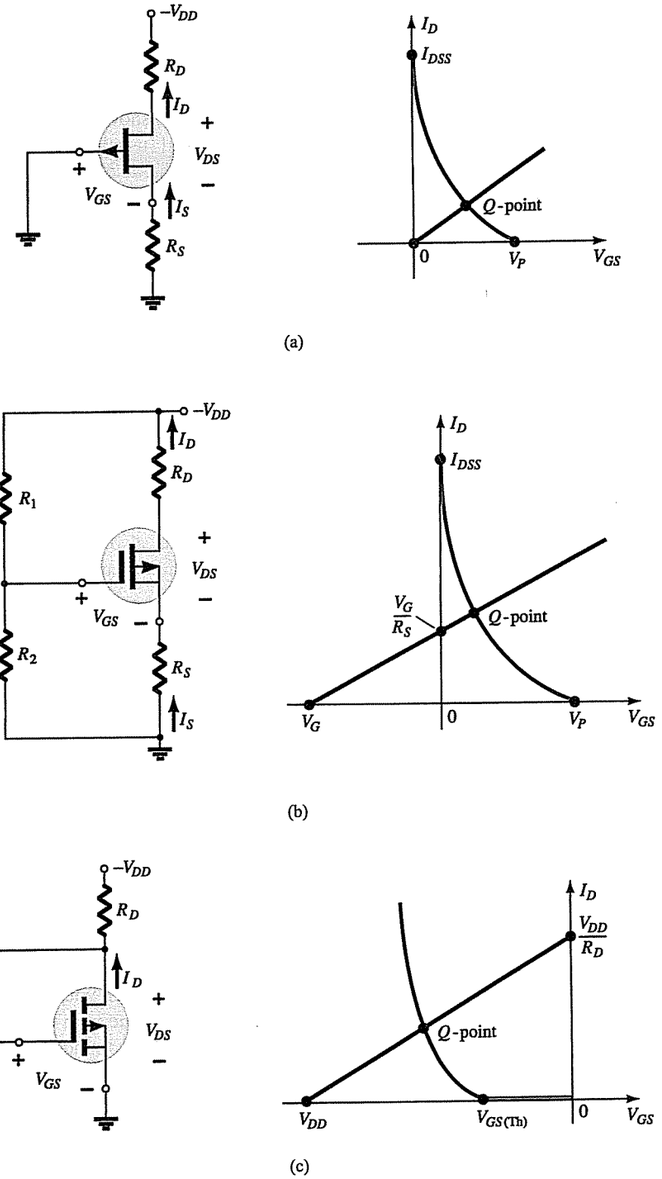


FIG. 7.56
p-Channel configurations. (a) JFET; (b) Depletion-type MOSFET; (c) Enhancement-type MOSFET.

PSpice

EXAMPLE 7.18 Determine I_{D_Q}, V_{GS_Q}, and V_{DS} for the *p*-channel JFET of Fig. 7.57.

Solution: We have

$$V_G = \frac{20\,\text{k}\Omega(-20\,\text{V})}{20\,\text{k}\Omega + 68\,\text{k}\Omega} = -4.55\,\text{V}$$

Applying Kirchhoff's voltage law gives

$$V_G - V_{GS} + I_D R_S = 0$$

and

$$V_{GS} = V_G + I_D R_S$$

Choosing $I_D = 0\,\text{mA}$ yields

$$V_{GS} = V_G = -4.55\,\text{V}$$

as appearing in Fig. 7.58.

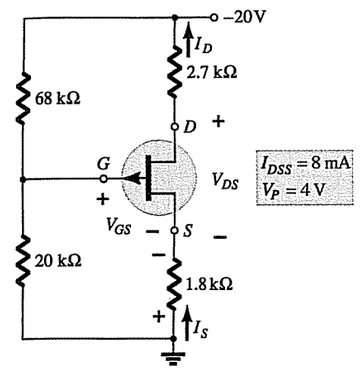


FIG. 7.57
Example 7.18.

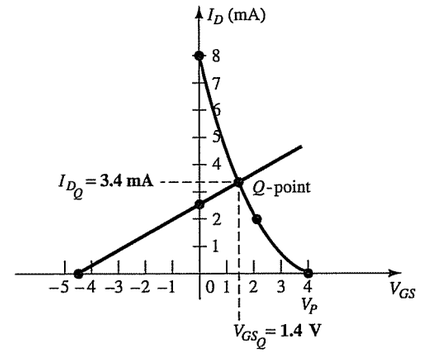


FIG. 7.58
Determining the Q-point for the JFET configuration of Fig. 7.57.

Choosing $V_{GS} = 0\,\text{V}$, we obtain

$$I_D = -\frac{V_G}{R_S} = -\frac{-4.55\,\text{V}}{1.8\,\text{k}\Omega} = 2.53\,\text{mA}$$

as also appearing in Fig. 7.58.

The resulting quiescent point from Fig. 7.58 is given by

$$I_{D_Q} = \mathbf{3.4\,mA}$$
$$V_{GS_Q} = \mathbf{1.4\,V}$$

For V_{DS}, Kirchhoff's voltage law results in

$$-I_D R_S + V_{DS} - I_D R_D + V_{DD} = 0$$

and

$$\begin{aligned} V_{DS} &= -V_{DD} + I_D(R_D + R_S) \\ &= -20\,\text{V} + (3.4\,\text{mA})(2.7\,\text{k}\Omega + 1.8\,\text{k}\Omega) \\ &= -20\,\text{V} + 15.3\,\text{V} \\ &= \mathbf{-4.7\,V} \end{aligned}$$

7.12 UNIVERSAL JFET BIAS CURVE

Since the dc solution of a FET configuration requires drawing the transfer curve for each analysis, a universal curve was developed that can be used for any level of I_{DSS} and V_P. The universal curve for an *n*-channel JFET or depletion-type MOSFET (for negative values of V_{GS_Q}) is provided in Fig. 7.59. Note that the horizontal axis is not that of V_{GS} but of a normalized level defined by $V_{GS}/|V_P|$, the $|V_P|$ indicating that only the magnitude of V_P is to be employed, not its sign. For the vertical axis, the scale is also a normalized level of I_D/I_{DSS}. The result is that when $I_D = I_{DSS}$, the ratio is 1, and when $V_{GS} = V_P$, the ratio $V_{GS}/|V_P|$ is -1. Note also that the scale for I_D/I_{DSS} is on the left rather than on the right as encountered for I_D in past exercises. The additional two scales on the right need an introduction. The vertical scale labeled *m* can in itself be used to find the solution to fixed-bias configurations. The other scale, labeled *M*, is employed along with the *m* scale to find the solution to voltage-divider configurations. The scaling for *m* and *M* come from a mathematical development involving the network equations and normalized scaling just introduced. The description to follow will not concentrate on why the *m* scale extends from 0 to 5 at $V_{GS}/|V_P| = -0.2$ and the *M* scale ranges from 0 to 1 at $V_{GS}/|V_P| = 0$, but rather on how to

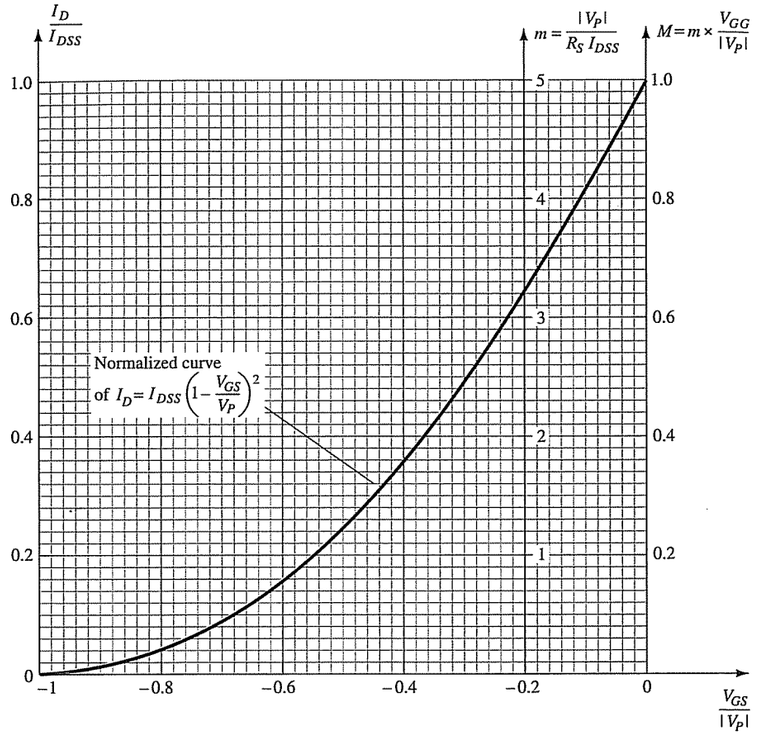


FIG. 7.59
Universal JFET bias curve.

use the resulting scales to obtain a solution for the configurations. The equations for m and M are the following, with V_G as defined by Eq. (7.15):

$$m = \frac{|V_P|}{I_{DSS}R_S} \tag{7.35}$$

$$M = m \times \frac{V_G}{|V_P|} \tag{7.36}$$

with

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

Keep in mind that the beauty of this approach is the elimination of the need to sketch the transfer curve for each analysis, that the superposition of the bias line is a great deal easier, and that the calculations are fewer. The use of the m and M axes is best described by examples employing the scales. Once the procedure is clearly understood, the analysis can be quite rapid, with a good measure of accuracy.

EXAMPLE 7.19 Determine the quiescent values of I_D and V_{GS} for the network of Fig. 7.60.

Solution: Calculating the value of m, we obtain

$$m = \frac{|V_P|}{I_{DSS}R_S} = \frac{|-3\text{ V}|}{(6\text{ mA})(1.6\text{ k}\Omega)} = 0.31$$

The self-bias line defined by R_S is plotted by drawing a straight line from the origin through a point defined by $m = 0.31$, as shown in Fig. 7.61.

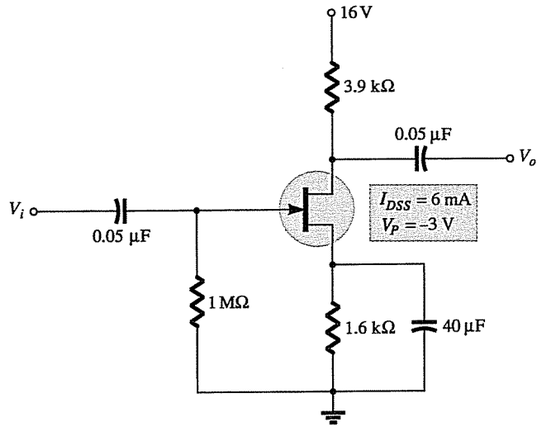


FIG. 7.60
Example 7.19.

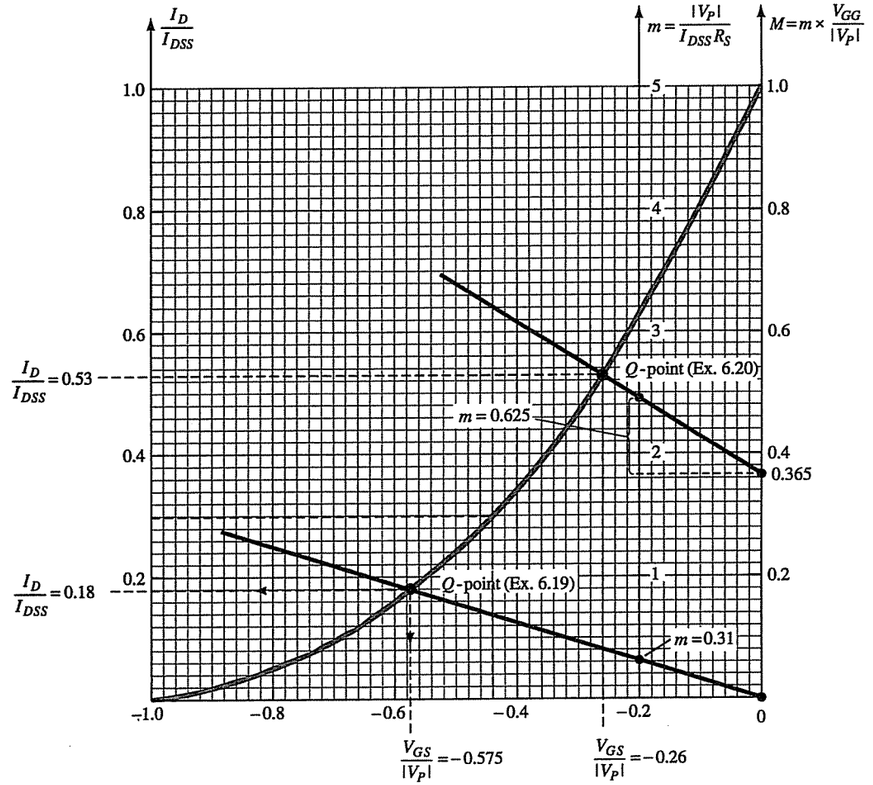


FIG. 7.61
Universal curve for Examples 7.19 and 7.20.

The resulting Q-point:

$$\frac{I_D}{I_{DSS}} = 0.18 \quad \text{and} \quad \frac{V_{GS}}{|V_P|} = -0.575$$

The quiescent values of I_D and V_{GS} can then be determined as follows:

$$I_{D_Q} = 0.18I_{DSS} = 0.18(6\text{ mA}) = \mathbf{1.08\text{ mA}}$$

and

$$V_{GS_Q} = -0.575|V_P| = -0.575(3\text{ V}) = \mathbf{-1.73\text{ V}}$$

EXAMPLE 7.20 Determine the quiescent values of I_D and V_{GS} for the network of Fig. 7.62.

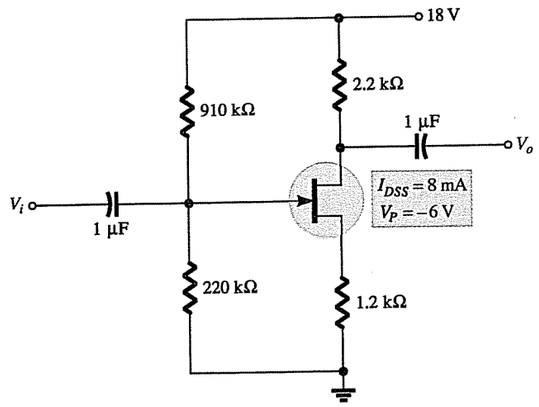


FIG. 7.62
Example 7.20.

Solution: Calculating m gives

$$m = \frac{|V_P|}{I_{DSS}R_S} = \frac{|-6\text{ V}|}{(8\text{ mA})(1.2\text{ k}\Omega)} = 0.625$$

Determining V_G yields

$$V_G = \frac{R_2V_{DD}}{R_1 + R_2} = \frac{(220\text{ k}\Omega)(18\text{ V})}{910\text{ k}\Omega + 220\text{ k}\Omega} = 3.5\text{ V}$$

Finding M, we have

$$M = m \times \frac{V_G}{|V_P|} = 0.625\left(\frac{3.5\text{ V}}{6\text{ V}}\right) = 0.365$$

Now that m and M are known, the bias line can be drawn on Fig. 7.61. In particular, note that even though the levels of I_{DSS} and V_P are different for the two networks, the same universal curve can be employed. First find M on the M axis as shown in Fig. 7.61. Then draw a horizontal line over to the m axis and, at the point of intersection, add the magnitude of m as shown in the figure. Using the resulting point on the m axis and the M intersection, draw the straight line to intersect with the transfer curve and define the Q-point. That is,

$$\frac{I_D}{I_{DSS}} = 0.53 \quad \text{and} \quad \frac{V_{GS}}{|V_P|} = -0.26$$

and

$$I_{D_Q} = 0.53I_{DSS} = 0.53(8\text{ mA}) = \mathbf{4.24\text{ mA}}$$

with

$$V_{GS_Q} = -0.26|V_P| = -0.26(6\text{ V}) = \mathbf{-1.56\text{ V}}$$

7.13 PRACTICAL APPLICATIONS

The applications described here take full advantage of the high input impedance of field-effect transistors, the isolation that exists between the gate and drain circuits, and the linear region of JFET characteristics that permit approximating the device by a resistive element between the drain and source terminals.

Voltage-Controlled Resistor (Noninverting Amplifier)

One of the most common applications of the JFET is as a variable resistor whose resistance value is controlled by the applied dc voltage at the gate terminal. In Fig. 7.63a, the linear region of a JFET transistor has been clearly indicated. Note that in this region the various curves all start at the origin and follow a fairly straight path as the drain-to-source voltage and drain current increase. Recall from your basic dc courses that **the plot of a fixed resistor is nothing more than a straight line with its origin at the intersection of the axes.**

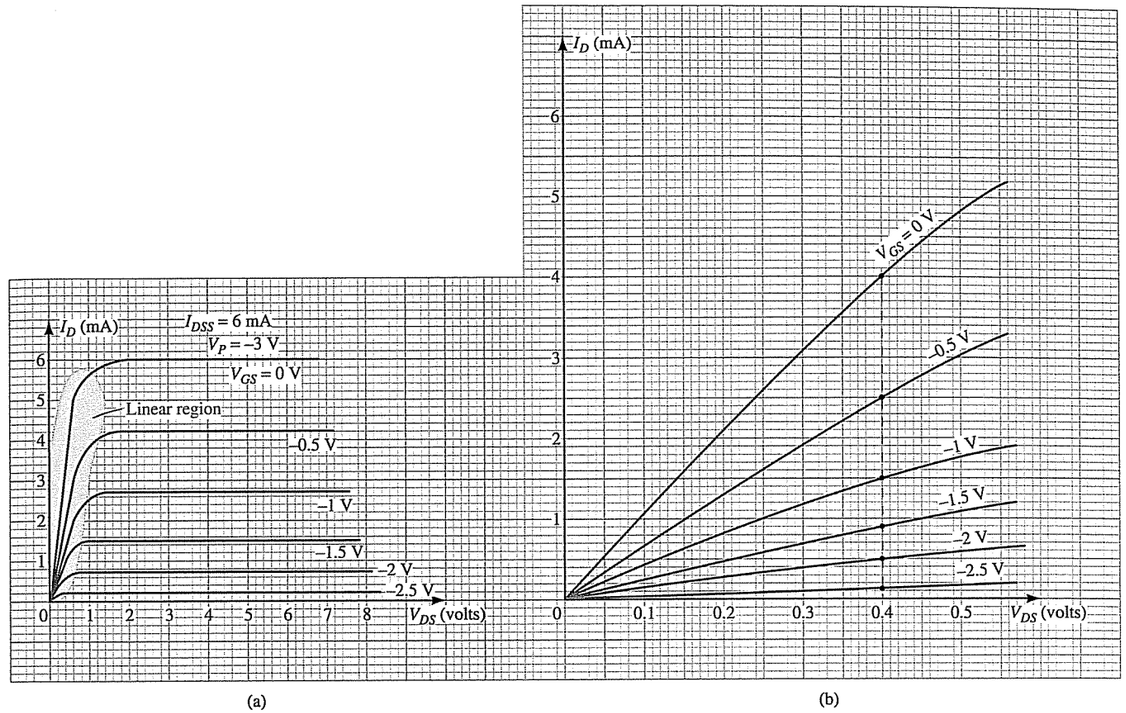


FIG. 7.63
JFET characteristics: (a) defining the linear region; (b) expanding the linear region.

In Fig. 7.63b, the linear region has been expanded to a maximum drain-to-source voltage of about 0.5 V. Note that even though the curves do have some curvature to them, they can easily be approximated by fairly straight lines, all having their origin at the intersection of the axes and a slope determined by the gate-to-source dc voltage. Recall from earlier discussions that **for an *I–V* plot where the current is the vertical axis and the voltage the horizontal axis, the steeper the slope, the less is the resistance; and the more horizontal the curve, the greater is the resistance**. The result is that a vertical line has 0 Ω resistance and a horizontal line has infinite resistance. At $V_{GS} = 0$ V, the slope is the steepest and the resistance the least. As the gate-to-source voltage becomes increasingly negative, the slope decreases until it is almost horizontal near the pinch-off voltage.

It is important to remember that this linear region is limited to levels of V_{DS} that are relatively small compared to the pinch-off voltage. In general, **the linear region of a JFET is defined by $V_{DS} \ll V_{DS_{max}}$ and $|V_{GS}| \ll |V_P|$.**

Using Ohm's law, let us calculate the resistance associated with each curve of Fig. 7.63b using the current that results at a drain-to-source voltage of 0.4 V.

$$V_{GS} = 0\text{ V}: \quad R_{DS} = \frac{V_{DS}}{I_{DS}} = \frac{0.4\text{ V}}{4\text{ mA}} = \mathbf{100\ \Omega}$$

$$V_{GS} = -0.5\text{ V}: \quad R_{DS} = \frac{V_{DS}}{I_{DS}} = \frac{0.4\text{ V}}{2.5\text{ mA}} = \mathbf{160\ \Omega}$$

$$V_{GS} = -1\text{ V}: \quad R_{DS} = \frac{V_{DS}}{I_{DS}} = \frac{0.4\text{ V}}{1.5\text{ mA}} = \mathbf{267\ \Omega}$$

$$V_{GS} = -1.5\text{ V}: \quad R_{DS} = \frac{V_{DS}}{I_{DS}} = \frac{0.4\text{ V}}{0.9\text{ mA}} = \mathbf{444\ \Omega}$$

$$V_{GS} = -2\text{ V}: \quad R_{DS} = \frac{V_{DS}}{I_{DS}} = \frac{0.4\text{ V}}{0.5\text{ mA}} = \mathbf{800\ \Omega}$$

$$V_{GS} = -2.5\text{ V}: \quad R_{DS} = \frac{V_{DS}}{I_{DS}} = \frac{0.4\text{ V}}{0.12\text{ mA}} = \mathbf{3.3\text{ k}\Omega}$$

In particular, note how **the drain-to-source resistance increases as the gate-to-source voltage approaches the pinch-off value.**

The results just obtained can be verified by Eq. (6.1) using the pinch-off voltage of -3 V and $R_o = 100\ \Omega$ at $V_{GS} = 0$ V. We have

$$R_{DS} = \frac{R_o}{\left(1 - \frac{V_{GS}}{V_P}\right)^2} = \frac{100\ \Omega}{\left(1 - \frac{V_{GS}}{-3\text{ V}}\right)^2}$$

$V_{GS} = -0.5$ V: $$R_{DS} = \frac{100\ \Omega}{\left(1 - \frac{-0.5\text{ V}}{-3\text{ V}}\right)^2} = \mathbf{144\ \Omega}$$ (versus 160 Ω above)

$V_{GS} = -1$ V: $$R_{DS} = \frac{100\ \Omega}{\left(1 - \frac{-1\text{ V}}{-3\text{ V}}\right)^2} = \mathbf{225\ \Omega}$$ (versus 267 Ω above)

$V_{GS} = -1.5$ V: $$R_{DS} = \frac{100\ \Omega}{\left(1 - \frac{-1.5\text{ V}}{-3\text{ V}}\right)^2} = \mathbf{400\ \Omega}$$ (versus 444 Ω above)

$V_{GS} = -2$ V: $$R_{DS} = \frac{100\ \Omega}{\left(1 - \frac{-2\text{ V}}{-3\text{ V}}\right)^2} = \mathbf{900\ \Omega}$$ (versus 800 Ω above)

$V_{GS} = -2.5$ V: $$R_{DS} = \frac{100\ \Omega}{\left(1 - \frac{-2.5\text{ V}}{-3\text{ V}}\right)^2} = \mathbf{3.6\ k\Omega}$$ (versus 3.3 kΩ above)

Although the results are not an exact match, for most applications Equation (6.1) provides an excellent approximation to the actual resistance level for R_{DS}.

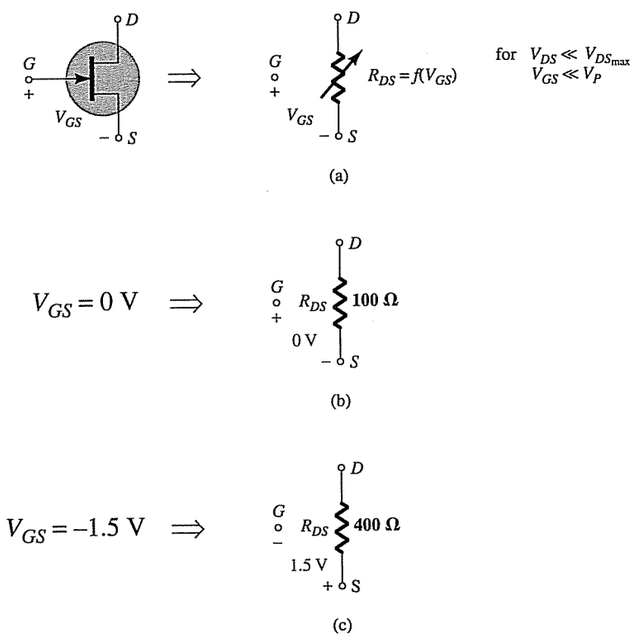


FIG. 7.64
JFET voltage-controlled drain resistance: (a) general equivalence; (b) with $V_{GS} = 0$ V; (c) with $V_{GS} = -1.5$ V.

Keep in mind that **the possible levels of V_{GS} between 0 V and pinch-off are infinite,** resulting in the full range of resistor values between 100 Ω and 3.3 kΩ. In general, therefore, the above discussion is summarized by Fig. 7.64a. For $V_{GS} = 0$ V, the equivalence of Fig. 7.64b would result; for $V_{GS} = -1.5$ V, the equivalence of Fig. 7.64c; and so on.

Let us now investigate the use of this voltage-controlled drain resistance in the noninverting amplifier of Fig. 7.65a;—**noninverting indicates that the input and output signals are in phase**. The op-amp of Fig. 7.65a is discussed in detail in Chapter 10, and the equation for the gain is derived in Section 10.4.

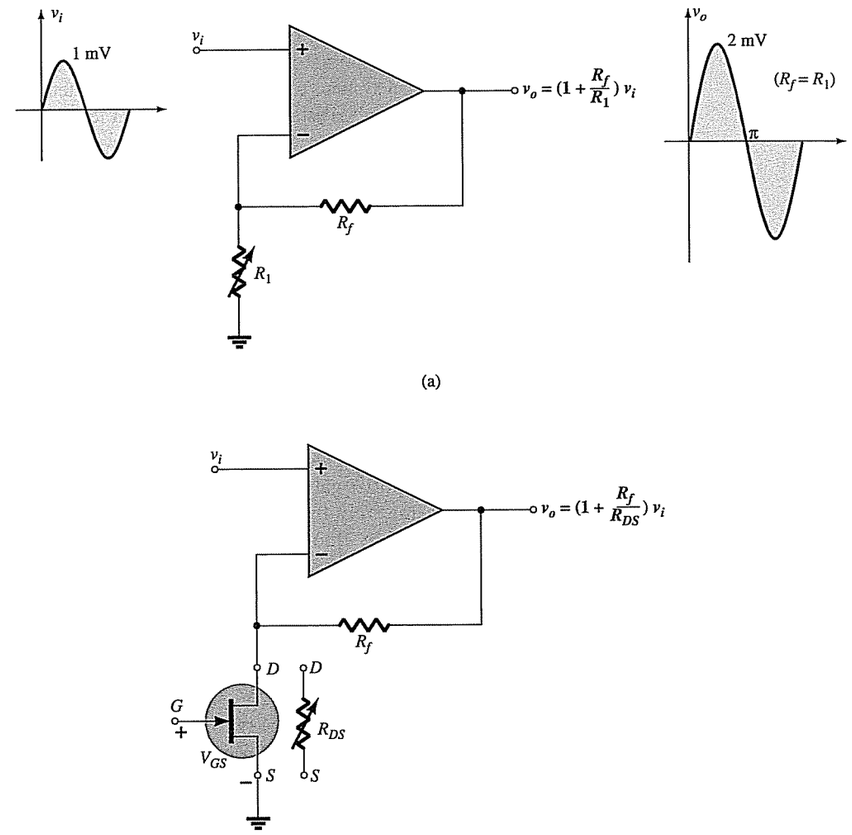


FIG. 7.65
(a) Noninverting op-amp configuration; (b) using the voltage-controlled drain-to-source resistance of a JFET in the noninverting amplifier.

If $R_f = R_1$, the resulting gain is 2, as shown by the in-phase sinusoidal signals of Fig. 7.65a. In Fig. 7.65b, the variable resistor has been replaced by an *n*-channel JFET. If $R_f = 3.3\ \text{k}\Omega$ and the transistor of Fig. 7.63 were employed, the gain could extend from $1 + 3.3\ \text{k}\Omega/3.3\ \text{k}\Omega = 2$ to $1 + 3.3\ \text{k}\Omega/100\ \Omega = 34$ for V_{GS} varying from -2.5 V to 0 V, respectively. In general, therefore, the gain of the amplifier can be set at any value between 2 and 34 by simply controlling the applied dc biasing voltage. The effect of this type of control can be extended to an extensive variety of applications. For instance, if the battery voltage of a radio should start to drop due to extended use, the dc level at the gate of the controlling JFET will drop, and the level of R_{DS} will decrease also. A drop in R_{DS} will result in an increase in gain for the same value of R_f, and the output volume of the radio can be maintained. A number of oscillators (networks designed to generate sinusoidal signals of specific frequencies) have a resistance factor in the equation for the frequency generated. If the

frequency generated should start to drift, a feedback network can be designed that changes the dc level at the gate of a JFET and therefore its drain resistance. If that drain resistance is part of the resistance factor in the frequency equation, the frequency generated can be stabilized or maintained.

One of the most important factors that affect the stability of a system is temperature variation. As a system heats up, the usual tendency is for the gain to increase, which in turn will usually cause additional heating and may eventually result in a condition referred to as "thermal runaway." Through proper design, a thermistor can be introduced that will affect the biasing level of a voltage-controlled variable JFET resistor. As the resistance of the thermistor drops with increase in heat, the biasing control of the JFET can be such that the drain resistance changes in the amplifier design to reduce the gain—establishing a balancing effect.

Before leaving the subject of thermal problems, note that some design specifications (often military type) require that systems that are overly sensitive to temperature variations be placed in a "chamber" or "oven" to establish a constant heat level. For instance, a 1-W resistor may be placed in an enclosed area with an oscillator network to establish a constant ambient heat level in the region. The design then centers on this heat level, which would be so high compared to the heat normally generated by the components that the variations in temperature levels of the elements could be ignored and a steady output frequency assured.

Other areas of application include any form of volume control, musical effects, meters, attenuators, filters, stability designs, and so on. One general advantage of this type of stability is that it avoids the need for expensive regulators (Chapter 15) in the overall design, although it should be understood that the purpose of this type of control mechanism is to "fine-tune" rather than to provide the primary source of stability.

For the noninverting amplifier, **one of the most important advantages associated with using a JFET for control is the fact that it is dc rather than ac control**. For most systems, dc control not only results in a reduced chance of adding unwanted noise to the system, but also lends itself well to remote control. For example, in Fig. 7.66a, a remote control panel controls the amplifier gain for the speaker by an ac line connected to the variable resistor. **The long line from the amplifier can easily pick up noise from the surrounding air as generated by fluorescent lights, local radio stations, operating equipment (even computers), motors, generators, and so on.** The result may be a 2-mV signal on the line with a 1-mV noise level—a terrible signal-to-noise ratio, which would only contribute to further deterioration of the signal coming in from the microphone due to the loop gain of the amplifier. In Fig. 7.66b, a dc line controls the gate voltage of the JFET and the variable resistance of the noninverting amplifier. Even though the dc line voltage on the line may be only -2 V, a ripple of 1 mV picked up by the long line will result in a very large signal-to-noise ratio, which could essentially be ignored in the distortion process. In other words, the noise on the dc line would simply move the dc operating point slightly on the device characteristics and would have almost no effect on the resulting drain resistance—isolation between the noise on the line and the amplifier response would be almost ideal.

Even though Figures 7.66a and 7.66b have a relatively long control line, the control line may only be 6″ long, as shown in the control panel of Fig. 7.66c, where all the elements of the amplifier are housed in the same container. Consider, however, **that just 1″ is enough to pick up RF noise**, so dc control is a favorable characteristic for almost any system. Furthermore, since the control resistance in Fig. 7.66a is usually quite large (hundreds of kilohms), whereas the dc voltage control resistors of the dc system of Fig. 7.66b are usually quite small (a few kilohms), the volume control resistor for the ac system will absorb a great deal more ac noise than the dc design. This phenomenon is a result of the fact that **RF noise signals in the air have a very high internal resistance, and therefore the larger the pickup resistance, the greater is the RF noise absorbed by the receiver**. Recall Thévenin's theorem, which states that for maximum power transfer, the load resistance should equal the internal resistance of the source.

As noted above, **dc control lends itself to computer and remote control systems** since they operate off specific fixed dc levels. For instance, when an infrared (IR) signal is sent out by a remote control to the receiver in a TV or VCR, the signal is passed through a decoder–counter sequence to define a particular dc voltage level on a staircase of voltage levels that can be fed into the gate of the JFET. For a volume control, that gate voltage may control the drain resistance of a noninverting amplifier controlling the volume of the system.

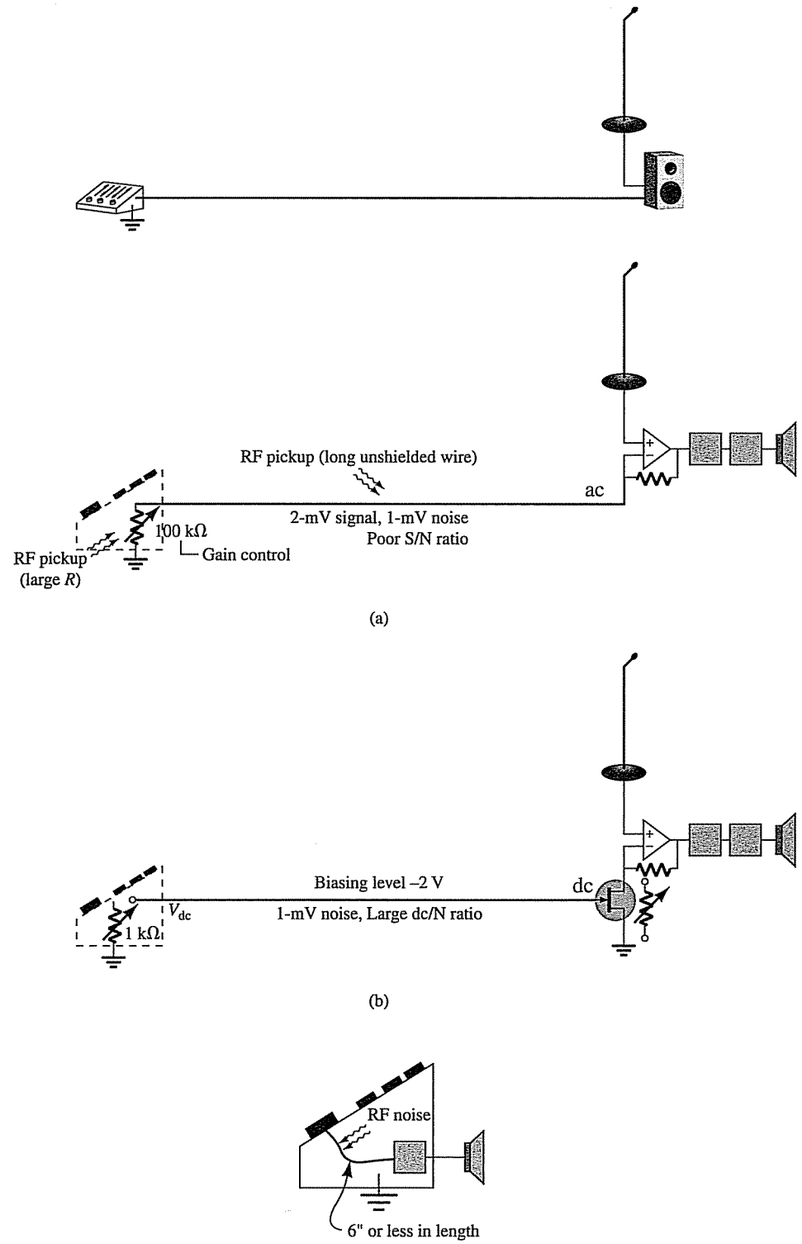
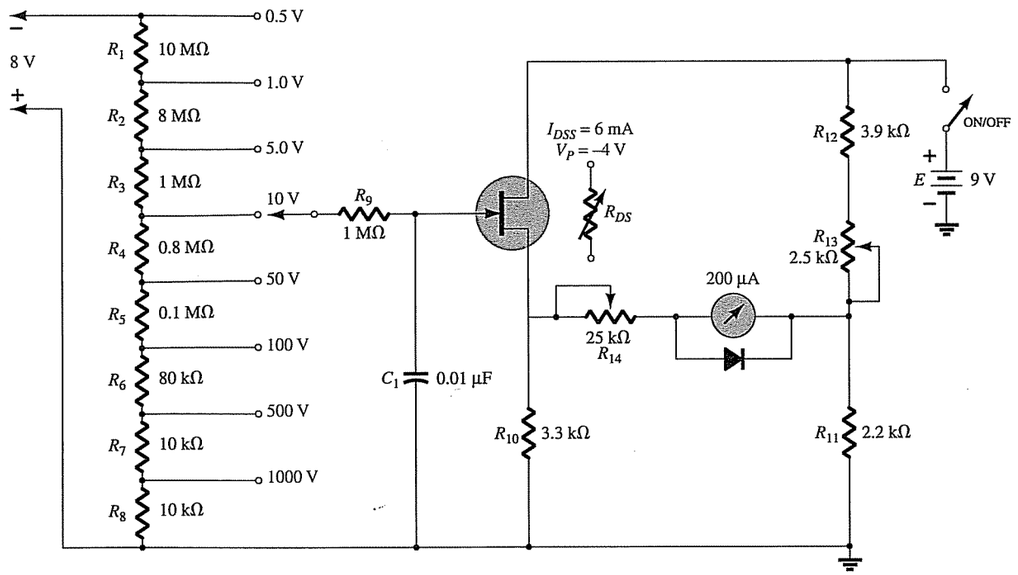


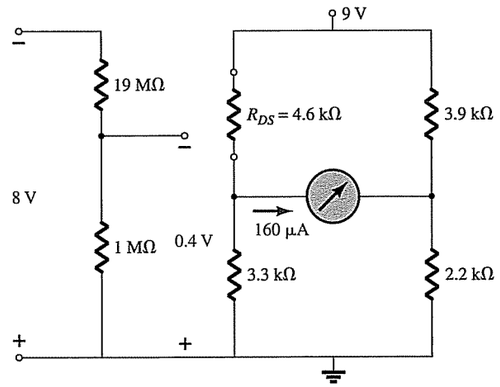
FIG. 7.66
Demonstrating the benefits of dc control: system with (a) ac control; (b) dc control; (c) RF noise pickup.

JFET Voltmeter

The voltage-controlled resistor effect just described will now be put to good use in the JFET voltmeter of Fig. 7.67a. The drain resistance of the JFET provides one arm of a bridge network that, when balanced, will result in zero current through the sensitive movement appearing in the equivalent diagram of Fig. 7.67b. Because of the need to properly bias the



(a)



(b)

FIG. 7.67

JFET voltmeter: (a) network; (b) reduced equivalent with an 8-V measurement. (Redrawn from International Rectifier Corporation.)

JFET, the user must be particularly careful to hook up the leads as shown to the 8 V being measured. A more sophisticated design would have a polarity switch that reverses the polarity if the meter pins or the reading is erroneous. For the 8 V being measured, the 10-V scale was chosen, resulting in a voltage-divider configuration as shown in Fig. 7.67b, which would result in −0.4 V from gate to source for the JFET. The resulting drain resistance of the JFET would then establish an unbalanced condition that would result in a current through the movement and an indication on the meter. Of course, for the reading to have any meaning, the meter would first have to be calibrated (movement set to zero under specific operating conditions), but this discussion is beyond the needs of this text.

For the special idealized situation of Fig. 7.67b with the balance resistors set on 0 Ω, a drain-to-source JFET resistance of about 4.6 kΩ would result in a meter current of about 160 μA, or 80% of full-scale reading (200 μA) as required for the 8 V being read on the 10-V scale. In addition, note that the gate-to-source voltage of −0.4 V is considerably less than the pinch-off voltage of −4 V and certainly much less than the maximum value of V_{DS} as required in the linear region of the JFET. The voltage-divider network of the input circuit

will ensure that the gate-to-source voltage does not exceed the boundaries that permit the variable resistance equivalence. In Fig. 7.67a, the capacitor is included to remove any surges that may develop when hooked up to the dc voltage to be measured and to short to ground any erroneous pickup noise at the source. The diode is included to protect the movement from excessive voltages (greater than 0.7 V). The variable resistors are included to zero the meter and to calibrate the meter using a known voltage source.

Before leaving the meter, note that **all meter movements have an "air-damp" mechanism designed to minimize the damage from surge currents and external turbulence**. When you shake a meter, you will find that the movement does not follow the shaking motion directly, but seems to lag the motion in a slower, lethargic manner. The reason is that air is being pushed out of the "air-damping container" by the motion of the pointer, slowing down the response of the balanced mechanism.

Timer Network

The high isolation between gate and drain circuits permits the design of a relatively simple timer such as shown in Fig. 7.68. The switch is a normally open (NO) switch, which, when closed, will short out the capacitor and cause its terminal voltage to quickly drop to 0 V. The switching network can handle the rapid discharge of voltage across the capacitor because the working voltages are relatively low and the discharge time is extremely short. Some would say it is a poor design, but in the practical world it is frequently used and not looked on as a terrible crime.

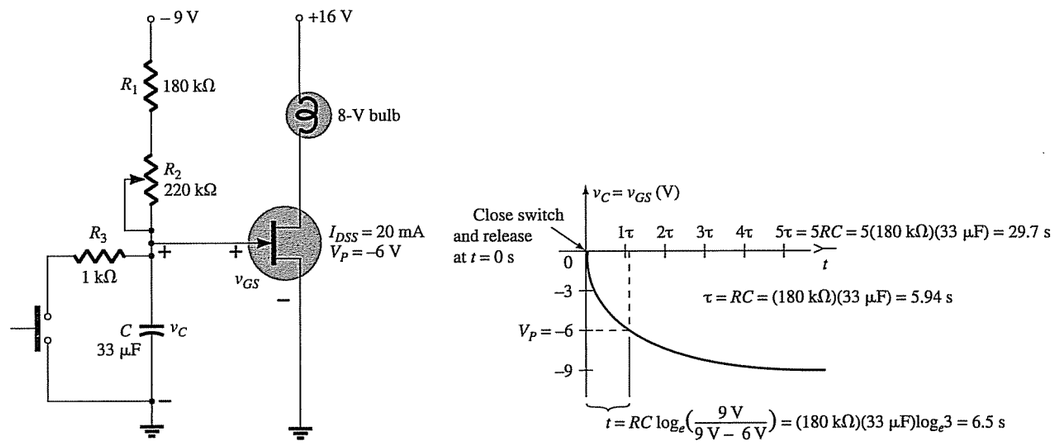


FIG. 7.68

JFET timer network.

When power is first applied, the capacitor will respond with its short-circuit equivalence since the **voltage across the capacitor cannot change instantaneously**. The result is that the gate-to-source voltage of the JFET will immediately be set to 0 V, the drain current I_D will equal I_{DSS}, and the bulb will turn on. However, with the switch in the normally open position, the capacitor will begin to charge to −9 V. **Because of the parallel high input impedance of the JFET, it has essentially no effect on the charging time constant of the capacitor**. Eventually, when the capacitor reaches the pinch-off level, the JFET and bulb will turn off. In general, therefore, when the system is first turned on, the bulb will light for a very short period of time and then turn off. It is now ready to perform its timing function.

When the switch is closed, it will short out the capacitor ($R_3 \ll R_1, R_2$) and will set the voltage at the gate to 0 V. The resulting drain current is I_{DSS}, and the bulb will burn brightly. When the switch is released, the capacitor will charge toward −9 V, and eventually when it reaches the pinch-off level, the JFET and bulb will turn off. The period during which the bulb is on will be determined by the time constant of the charging network, determined by $\tau = (R_1 + R_2)C$ and the level of the pinch-off voltage. The more negative the pinch-off level, the longer the bulb will be on. Resistor R_1 is included to be sure that there is some

resistance in the charging circuit when the power is turned on. Otherwise, a very heavy current could result that might damage the network. Resistor R_2 is a variable resistor, so the "on" time can be controlled. Resistor R_3 was added to limit the discharge current when the switch is closed. When the switch across the capacitor is closed, the discharge time of the capacitor will be only $5\tau = 5RC = 5(1\,\text{k}\Omega)(33\,\mu\text{F}) = 165\,\mu\text{s} = 0.165\,\text{ms} = 0.000165\,\text{s}$. In summary, therefore, when the switch is pressed and released, the bulb will come on brightly, and then, as time goes on, it will become dimmer until it shuts off after a period of time determined by the network time constant.

One of the most obvious applications of such a timing system is in a hallway or travel corridor where you want light for a short period of time so that you can pass safely but then want the system to turn off on its own. When you enter or leave a car, you may want a light on for a short period of time but don't want to worry about turning it off. There are endless possibilities for a timing network such as just described. Just consider the variety of other electrical or electronic systems that you would like to turn on for specific periods of time, and the list of uses grow exponentially.

One might ask why a BJT would not be a good alternative to the JFET for the same application. First, the input resistance of the BJT may be only a few kilohms. That would affect not only the time constant of the charging network, but also the maximum voltage to which the capacitor could charge. Just draw an equivalent network with the transistor replaced by a 1-kΩ resistor, and the above will immediately become clear. In addition, the control levels will have to be designed with a great deal more care since the BJT transistor turns on at about 0.7 V. The voltage swing from off to on is only 0.7 V rather than 4 V for the JFET configuration. One final note: You might have noticed the absence of a series resistor in the drain circuit for the situation when the bulb is first turned on and the resistance of the bulb is very low. The resulting current could be quite high until the bulb reaches its rated intensity. However, again, as described above for the switch across the capacitor, if the energy levels are small and the duration of stress minimal, such designs are often accepted. If there were any concern, adding a resistor of 0.1 to 1 Ω in series with the bulb would provide some security.

Fiber Optic Systems

The introduction of fiber optic technology has had a dramatic effect on the communications industry. **The information-carrying capacity of fiber optic cable is significantly greater** than that provided by conventional methods with individual pairs of wire. In addition, **the cable size is reduced, the cable is less expensive, crosstalk due to electromagnetic effects between current-carrying conductors is eliminated, and noise pickup due to external disturbances such as lightning are eliminated**.

The fiber optic industry is based on the fact that information can be transmitted on a beam of light. Although the speed of light through free space is 3×10^8 meters per second, or approximately 186,000 miles per second, its speed will be reduced by encounters with other media, causing reflection and refraction. When light information is passed through a fiber optic cable, it is expected to bounce off the walls of the cable. However, the angle at which the light is injected into the cable is critical, as is the actual design of the cable. In Fig. 7.69, the basic elements of a fiber optic cable are defined. The glass or plastic core of

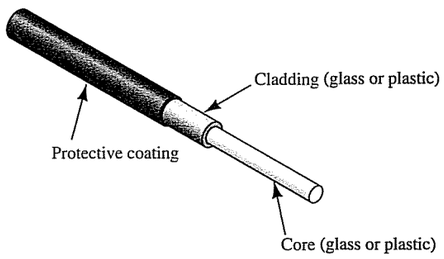


FIG. 7.69
Basic elements of a fiber optic cable.

the cable can be as small as 8 μm, which is close to 1/10 the diameter of a human hair. The core is surrounded by an outer layer called the *cladding*, which is also made of glass or plastic, but has a different refractive index to ensure that the light in the core that hits the outer surface of the core is reflected back into the core. A protective coating is then added to protect the two layers from outside environmental effects.

Most optical communication systems work in the infrared frequency range, which extends from 3×10^{11} Hz to 5×10^{14} Hz. This spectrum is just below the visible light spectrum, which extends from 5×10^{14} Hz to 7.7×10^{14} Hz. For most optical systems the frequency range of 1.87×10^{14} Hz to 3.75×10^{14} Hz is used. Because of the very high frequencies, each carrier can be modulated by hundreds or thousands of voice channels simultaneously. In addition, **very high speed computer transmission is a possibility, although one must be sure that the electronic components of the modulators can also operate successfully at the same frequency**. For distances over 30 nautical miles, repeaters (a combination receiver, amplifier, and transmitter) must be used, which require an additional electrical conductor in the cable that carries a current of about 1.5 A at 2500 V.

The basic components of an optical communication system are shown in Fig. 7.70. The input signal is applied to a light modulator whose sole purpose is to convert the input signal to one of corresponding levels of light intensity to be directed down the length of fiber optic cable. The information is then carried through the cable to the receiving station, where a light demodulator converts the varying light intensities back to voltage levels that match those of the original signal.

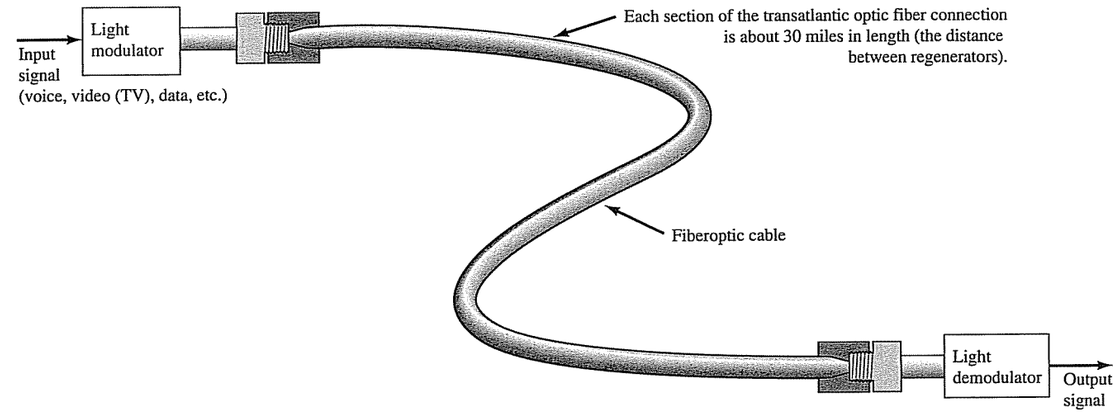


FIG. 7.70
Basic components of an optical communication system.

An electronic equivalent for the transmission of computer transistor-transistor-logic (TTL) information is provided in Fig. 7.71a. With the Enable control in the "on" or 1-state, the TTL information at the input to the AND gate can pass through to the gate of the JFET configuration. The design is such that the discrete levels of voltage associated with the TTL logic will turn the JFET on and off (perhaps 0 V and −5 V, respectively, for a JFET with $V_P = -4$ V). The resulting change in current levels will result in two distinct levels of light intensity from the LED (Section 1.16) in the drain circuit. That emitted light will then be directed through the cable to the receiving station, where a photodiode (Section 16.6) will react to the incident light and permit different levels of current to pass through as established by V and R. The current for photodiodes is a reverse current having the direction shown in Fig. 7.71a, but in the ac equivalent the photodiode and the resistor R are in parallel as shown in Fig. 7.71b, establishing the desired signal with the polarity shown at the gate of the JFET. Capacitor C is simply an open circuit to dc to isolate the biasing arrangement for the photodiode from the JFET and a short circuit as shown for the signal v_s. The incoming signal will then be amplified and will appear at the drain terminal of the output JFET.

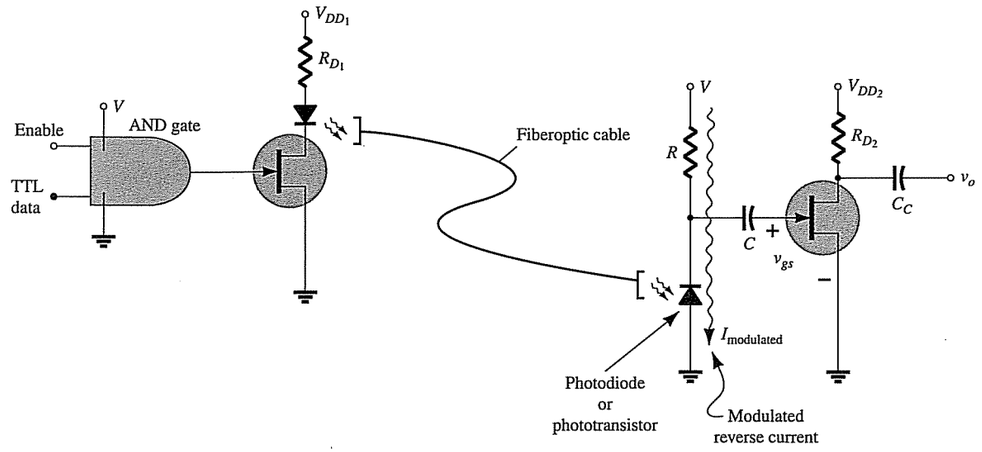


FIG. 7.71

TTL fiber optic communication channel: (a) JFET design; (b) passing on the signal generated across the photodiode.

As mentioned above, all the elements of the design, including the JFETs, LED, photodiode, capacitors, and so on, must be carefully chosen to ensure that they function properly at the high frequency of transmission. In fact, laser diodes are frequently used instead of LEDs in the modulator because they work at higher information rates and higher powers and have lower coupling and transmission losses. However, laser diodes are a great deal more expensive and more temperature sensitive, and they typically have a shorter lifetime than LEDs. For the demodulator side, the photodiodes are either of the pin photodiode or the avalanche photodiode variety. The *pin* abbreviation comes from the *p*-*i*ntrinsic-*n* construction process, and the term *avalanche* from the rapidly growing ionization process that develops during operation.

In general, the JFET is excellent for this application because of its high isolation at the input side and its ability to quickly "snap" from one state to the other due to the TTL input. At the output side the isolation blocks any effect of the demodulator sensing circuit from affecting the ac response, and it provides some gain for the signal before it is passed on to the next stage.

MOSFET Relay Driver

The MOSFET relay driver to be described in this section is an excellent example of how the FETs can be used to **drive high-current/high-voltage networks without drawing current or power from the driving circuit. The high input impedance of FETs essentially isolates the two parts of the network without the need for optical or electromagnetic linkages**. The network to be described can be used for a variety of applications, but our application will be limited to an alarm system activated when someone or something passes the plane of the transmitted light.

The IR (infrared—not visible) LED of Fig. 7.72 is directing its light through a directional funnel to hit the face of a photoconductive cell (Section 16.7) of the controlling

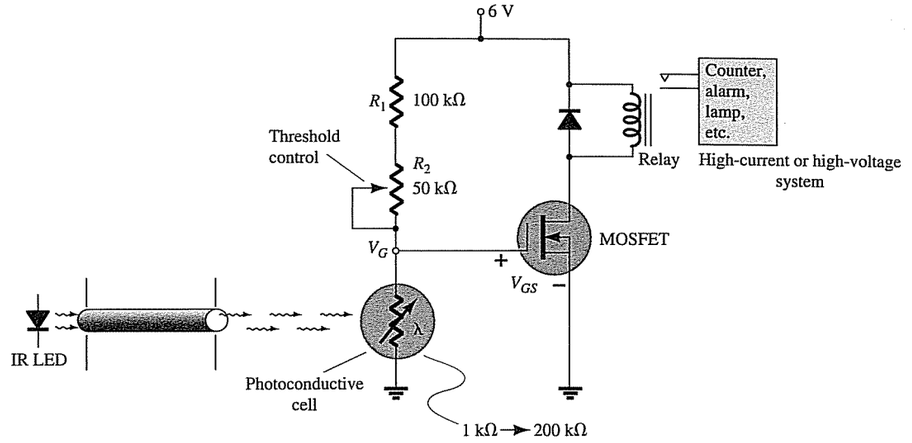


FIG. 7.72

MOSFET relay driver.

network. The photoconductive cell has a range of resistance from about 200 kΩ as its dark resistance level down to less than 1 kΩ at high illumination levels. Resistor R_1 is a variable resistance that can be used to set the threshold level of the depletion-type MOSFET. A medium-power MOSFET was employed because of the high level of drain current through the magnetizing coil. The diode is included as a protective device for reasons discussed in detail in Section 2.11.

When the system is on and the light consistently hitting the photoconductive cell, the resistance of the cell may drop to 10 kΩ. At this level an application of the voltage-divider rule will result in a voltage of about 0.54 V at the gate terminal (with the 50-kΩ potentiometer set to 0 kΩ). The MOSFET will be on, but not at a drain current level that will cause the relay to change state. When someone passes by, the light source will be cut off, and the resistance of the cell may quickly (in a few microseconds) rise to 100 kΩ. The voltage at the gate will then rise to 3 V, turning on the MOSFET and activating the relay and turning on the system under control. An alarm circuit has its own control design to ensure that it will not turn off when light returns to the photoconductive cell.

In essence, therefore, we have controlled a high-current network with a relatively small dc voltage level and a rather inexpensive design. The only obvious flaw in the design is the fact that the MOSFET will be on even when there is no intrusion. This can be remedied through the use of a more sophisticated design, but keep in mind that **MOSFETs are typically low-power-consumption devices**, so the power loss, even over time, is not that great.

7.14 SUMMARY

Important Conclusions and Concepts

1. A fixed-bias configuration has, as the label implies, a **fixed** dc voltage applied from gate to source to establish the operating point.
2. The **nonlinear** relationship between the gate-to-source voltage and the drain current of a JFET requires that a graphical or mathematical solution (involving the solution of two simultaneous equations) be used to determine the quiescent point of operation.
3. All voltages with a single subscript define a voltage from a specified point to **ground**.
4. The self-bias configuration is determined by an equation for V_{GS} that will *always* pass through the origin. Any other point determined by the biasing equation will establish a **straight** line to represent the biasing network.
5. For the voltage-divider biasing configuration, one can always assume that the gate current is 0 A to permit an **isolation** of the voltage-divider network from the output section. The resulting gate-to-ground voltage will always be **positive for an *n*-channel**

JFET and **negative for a *p*-channel JFET. Increasing values of R_S** result in **lower quiescent values of I_D** and more **negative values of V_{GS} for an *n*-channel JFET.**

6. The method of analysis applied to depletion-type MOSFETs is the same as applied to JFETs, with the only difference being a possible operating point with an I_D level **above** the I_{DSS} value.
7. The characteristics and method of analysis applied to enhancement-type MOSFETs are **entirely different** from those of JFETs and depletion-type MOSFETs. For values of V_{GS} less than the threshold value, the drain current is 0 A.
8. When analyzing networks with a variety of devices, first work with the region of the network that will provide a **voltage or current level** using the basic relationships associated with those devices. Then use that level and the appropriate equations to find other voltage or current levels of the network in the surrounding region of the system.
9. The design process often requires finding a resistance level to establish the desired voltage or current level. With this in mind, remember that a resistance level is defined by the **voltage across the resistor divided by the current** through the resistor. In the design process, both of these quantities are often available for a particular resistive element.
10. The ability to troubleshoot a network requires a **clear, firm understanding** of the terminal behavior of each of the devices in the network. That knowledge will provide an **estimate** of the working voltage levels of specific points of the network, which can be checked with a voltmeter. The ohmmeter section of a multimeter is particularly helpful in ensuring that there is a **true connection** between all the elements of the network.
11. The analysis of *p*-channel FETs is the same as that applied to *n*-channel FETs except for the fact that all the voltages will have the **opposite polarity** and the currents the **opposite direction.**

Equations

JFETs/depletion-type MOSFETs:

$$\text{Fixed-bias configuration:} \quad V_{GS} = -V_{GG} = V_G$$

$$\text{Self-bias configuration:} \quad V_{GS} = -I_D R_S$$

$$\text{Voltage-divider biasing:} \quad V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

$$V_{GS} = V_G - I_D R_S$$

Enhancement-type MOSFETs:

$$\text{Feedback biasing:} \quad V_{DS} = V_{GS}$$

$$V_{GS} = V_{DD} - I_D R_D$$

$$\text{Voltage-divider biasing:} \quad V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

$$V_{GS} = V_G - I_D R_S$$

7.15 COMPUTER ANALYSIS

PSpice Windows

JFET Voltage-Divider Configuration The results of Example 7.20 will now be verified using PSpice Windows. The network of Fig. 7.73 is constructed using computer methods described in the previous chapters. The J2N3819 JFET is obtained from the **EVAL** library, and **Edit-PSpice model** is used to set **Beta** to 0.222 mA/V^2 and **Vto** to -6 V. The **Beta** value is determined using Eq. (6.17) and the provided I_{DSS} and V_P. The results of the **Simulation** appear in Fig. 7.74 with the dc bias voltage and current levels. The resulting drain current is 4.231 mA, compared to the calculated level of 4.24 mA—an excellent match. The voltage V_{GS} is 3.504 V $-$ 5.077 V $= -1.573$ V versus the calculated level of -1.56 V in Example 7.20—another excellent match.

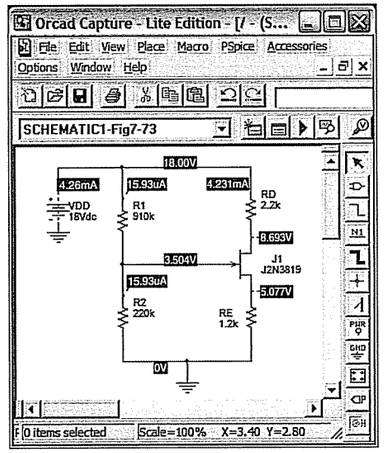


FIG. 7.73
JFET voltage-divider configuration with PSpice Windows results for current and voltage levels.

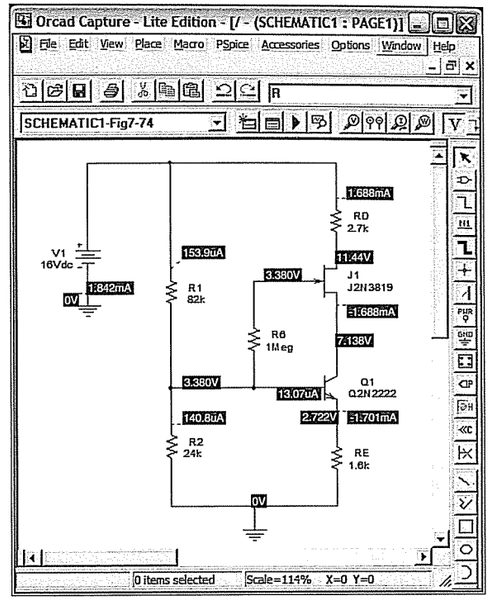


FIG. 7.74
Verifying the hand-calculated solution of Example 7.13 using PSpice Windows.

Combination Network Next, the result of Example 7.13 with both a transistor and JFET will be verified. For the transistor **Bf** is set to 180, whereas for the JFET, **Beta** is set to 0.333 mA/V^2 and **Vto** to -6 V as called for in the example. The results for all the dc levels appear in Fig. 7.75. Note again the excellent comparison with the calculator solution, with V_D at 11.44 V compared to 11.07 V, $V_S = V_C$ at 7.138 V compared to 7.32 V, and V_{GS} at -3.758 V compared to -3.7 V.

Enhancement MOSFET Next, the analysis procedure of Section 7.6 will be verified using the IRF150 enhancement-type *n*-channel MOSFET found in the **EVAL** library. First, the device characteristics will be obtained using a procedure similar to that used to obtain the transistor and JFET characteristics. Because the plot is of a single curve, there is no need for a nested or secondary sweep. In the **Simulation Settings** dialog box, choose **DC Sweep**, **Voltage Source** variable, and **Linear**. Note in Fig. 7.76 that the voltage V_{DD} is set at 9 V because that is about three times the threshold value (**Vto**) of 2.831 V. The gate-to-source voltage V_{GG} is swept from 0 V to 20 V. Therefore **Name** is **VGG**, **Start Value** is **0 V**, **End Value** is **20 V**, and the **Increment** is **0.01 V**. The **End Value** of 20 V is chosen to be sure there is distance between the rising curve and the end of the horizontal axis. After the simulation the sequence **Trace-Add Trace-ID(M1)** results in a curve similar to Fig. 7.77. The major difference is that the response has a drain current well beyond the limits of the device. The vertical rise can be limited to 80 A by selecting **Plot-Axis Settings-Y-Axis-User Defined** and entering **0 A** to **80 A**. An **OK**, and the graph of Fig. 7.76 results. The labels **ID** and **VGS** are added using the sequence **Plot-Label-Text**.

Now that we have the characteristics, we should build a network to establish an operating point in the middle of the operating region. Drawing the load line shown in Fig. 7.76 requires a source voltage V_{DD} of 20 V as shown in Fig. 7.77. The intersection with the vertical axis is at 50 A, which requires a drain resistance of 0.4 Ω, as appearing in Fig. 7.76. As shown on Fig. 7.76, the resulting drain current is near 31.5 A and the gate-to-source or drain-to-source voltage is 7.4 V. Once the network of Fig. 7.77 is constructed the **Simulation Settings** can be set at **Analysis type**: **Bias Point** followed by **OK** and then **Simulation** to obtain the results of Fig. 7.77. Note that the drain current of 31.49 A is very close to the 31.5 A of Fig. 7.76, and the gate-to-source of 7.404 V is very close to the 7.4 V

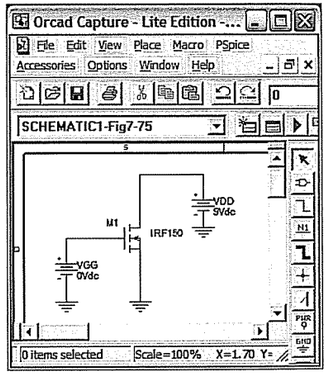


FIG. 7.75
Network used to obtain the characteristics of the IRF150 enhancement-type n-channel MOSFET.

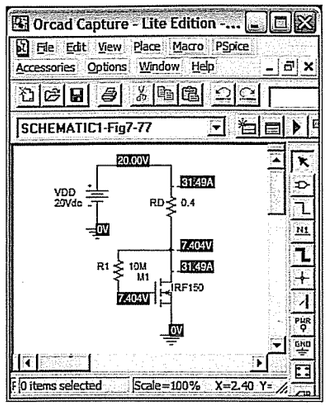


FIG. 7.77
Feedback-biasing arrangement using an IRF150 enhancement-type MOSFET.

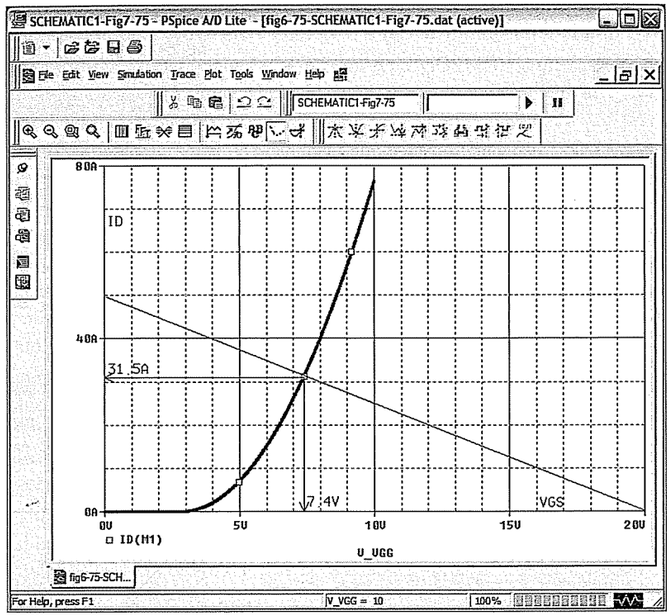


FIG. 7.76
Characteristics of the IRF500 MOSFET of Figure 7.75 with a load line defined by the network of Figure 7.77.

solution—a perfect match. When using **V** and **I** to display voltages and currents, respectively, keep in mind that some of the labels can be deleted by simply selecting them and choosing **Delete**.

Multisim

The results of Example 7.2 will now be verified using Multisim. The construction of the network of Fig. 7.78 is essentially the same as applied in the BJT chapters. The JFET is obtained by selecting **Transistor**, the fourth key down on the first vertical toolbar. A **Select a Component** dialog box will appear, in which **JFET_N** can be selected under the **Family** listing. A long **Component** list appears, in which **2N3821** is selected for this application. An **OK**, and it can be placed on the screen. After double-clicking the symbol on the screen, a **JFET_N** dialog box will appear in which **Value** can be selected, followed by **Edit Model**. An **Edit Model** dialog box will appear in which **Beta** and **Vto** can be set to **0.222 mA/V²** and **−6 V**, respectively. The value of **Beta** is determined using Eq. (6.17) and the parameters of the network as follows:

$$\text{Beta} = \frac{I_{DSS}}{|V_P|^2} = \frac{8\text{ mA}}{|-6\text{ V}|^2} = \frac{8\text{ mA}}{36\text{ V}^2} = 0.222\text{ mA/V}^2$$

Once the change is made, be sure to select **Change Part Model** before leaving the dialog box. The **JFET_N** dialog box will appear again, but an **OK**, and the changes will be made. The labels **IDSS = 8 mA** and **Vp = −6 V** are added using **Place-Text**. A blinking vertical bar will appear marking the place where the label can be entered. Once entered, it can easily be moved by simply clicking the area and dragging it to the desired position while holding the clicker down.

Using the **Indicator** option on the first vertical toolbar displays the drain and source voltages as shown in Fig. 7.78. In both cases the **VOLTMETER_V** option was chosen in the **Select a Component** dialog box.

Selecting **Simulate-Run** or moving the switch to the **1** position results in the display of Fig. 7.78. Note that V_{GS} at −2.602 V is an exact match with the hand-calculated solution of −2.6 V. Although the indicator is connected from source to ground, be aware that this is also the gate-to-source voltage because the voltage drop across the 1-MΩ resistor is

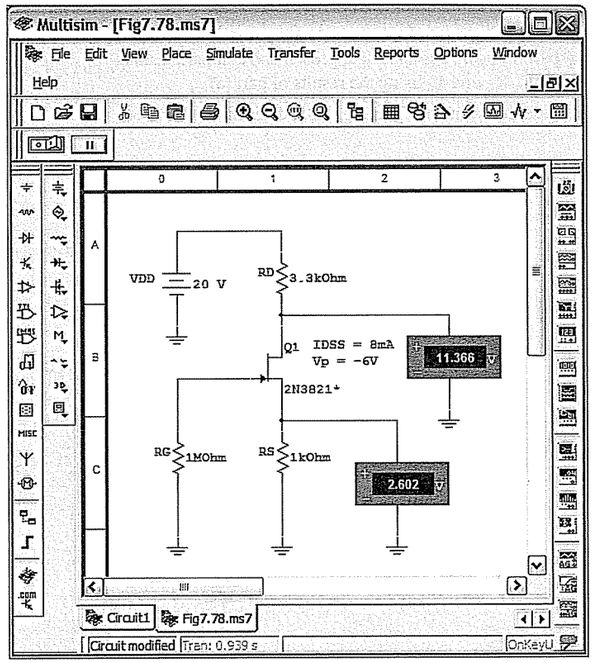


FIG. 7.78
Verifying the results of Example 7.2 using Multisim.

assumed to be 0 V. The level of 11.366 V at the drain is very close to the hand-calculated solution of 11.42 V—in all, a complete verification of the results of Example 7.2.

PROBLEMS

**Note:* Asterisks indicate more difficult problems.

7.2 Fixed-Bias Configuration

1. For the fixed-bias configuration of Fig. 7.79:
   a. Sketch the transfer characteristics of the device.
   b. Superimpose the network equation on the same graph.
   c. Determine I_{D_Q} and V_{DS_Q}.
   d. Using Shockley's equation, solve for I_{D_Q} and then find V_{DS_Q}. Compare with the solutions of part (c).

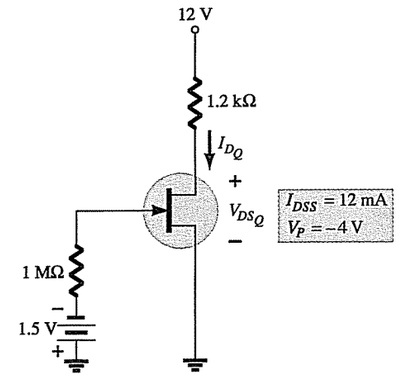


FIG. 7.79
Problems 1 and 35.

2. For the fixed-bias configuration of Fig. 7.80, determine:
   a. I_{D_Q} and V_{GS_Q} using a purely mathematical approach.
   b. Repeat part (a) using a graphical approach and compare results.
   c. Find V_{DS}, V_D, V_G, and V_S using the results of part (a).
3. Given the measured value of V_D in Fig. 7.81, determine:
   a. I_D.
   b. V_{DS}.
   c. V_{GG}.

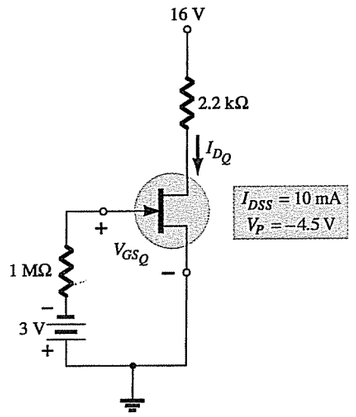


FIG. 7.80
Problem 2.

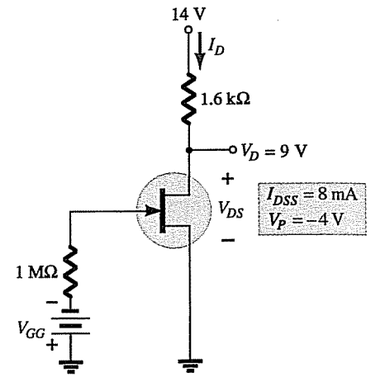


FIG. 7.81
Problem 3.

4. Determine V_D for the fixed-bias configuration of Fig. 7.82.
5. Determine V_D for the fixed-bias configuration of Fig. 7.83.

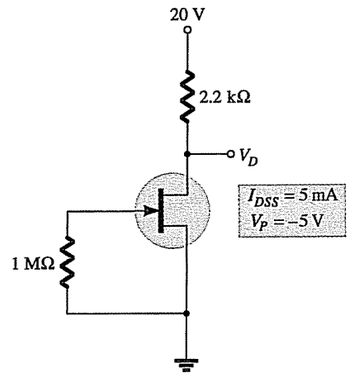


FIG. 7.82
Problem 4.

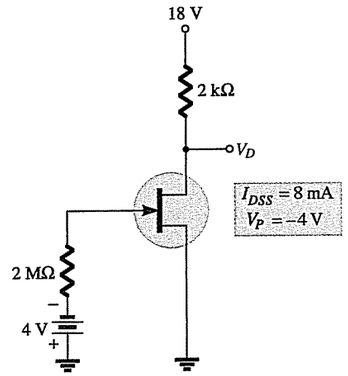


FIG. 7.83
Problem 5.

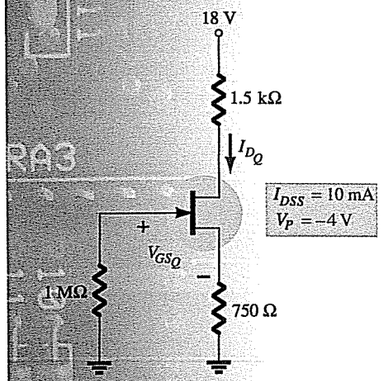


FIG. 7.84
Problems 6, 7, and 36.

7.3 Self-Bias Configuration

6. For the self-bias configuration of Fig. 7.84:
   a. Sketch the transfer curve for the device.
   b. Superimpose the network equation on the same graph.
   c. Determine I_{D_Q} and V_{GS_Q}.
   d. Calculate V_{DS}, V_D, V_G, and V_S.

*7. Determine I_{D_Q} for the network of Fig. 7.84 using a purely mathematical approach. That is, establish a quadratic equation for I_D and choose the solution compatible with the network characteristics. Compare to the solution obtained in Problem 6.

8. For the network of Fig. 7.85, determine:
   a. V_{GS_Q} and I_{D_Q}.
   b. V_{DS}, V_D, V_G, and V_S.
9. Given the measurement V_S = 1.7 V for the network of Fig. 7.86, determine:
   a. I_{D_Q}.
   b. V_{GS_Q}.
   c. I_{DSS}.
   d. V_D.
   e. V_{DS}.
*10. For the network of Fig. 7.87, determine:
   a. I_D.
   b. V_{DS}.
   c. V_D.
   d. V_S.
*11. Find V_S for the network of Fig. 7.88.

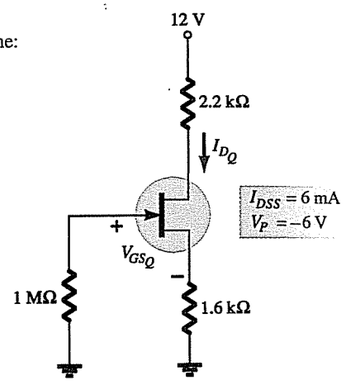


FIG. 7.85
Problem 8.

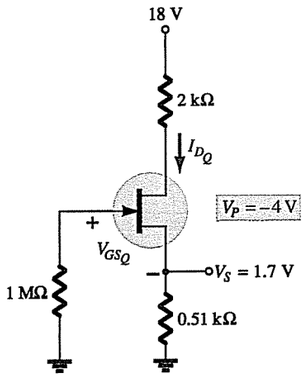


FIG. 7.86
Problem 9.

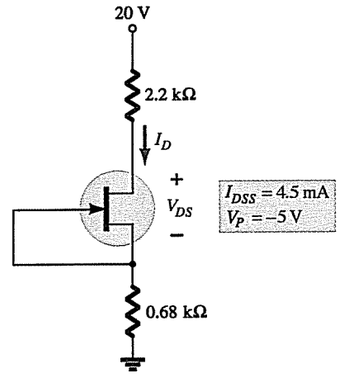


FIG. 7.87
Problem 10.

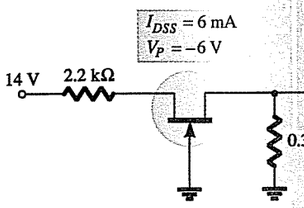


FIG. 7.88
Problem 11.

7.4 Voltage-Divider Biasing

12. For the network of Fig. 7.89, determine:
   a. V_G.
   b. I_{D_Q} and V_{GS_Q}.
   c. V_D and V_S.
   d. V_{DS_Q}.

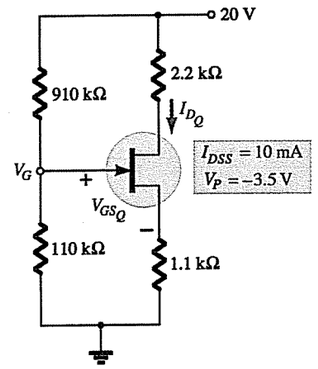


FIG. 7.89
Problems 12 and 13.

13. **a.** Repeat Problem 12 with $R_S = 0.51\ \text{k}\Omega$ (about 50% of the value of that of Problem 12). What is the effect of a smaller R_S on I_{D_Q} and V_{GS_Q}?
    b. What is the minimum possible value of R_S for the network of Fig. 7.89?
14. For the network of Fig. 7.90, $V_D = 9\ \text{V}$. Determine:
    a. I_D.
    b. V_S and V_{DS}.
    c. V_G and V_{GS}.
    d. V_P.
*15. For the network of Fig. 7.91, determine:
    a. I_{D_Q} and V_{GS_Q}.
    b. V_{DS} and V_S.
*16. Given $V_{DS} = 4\ \text{V}$ for the network of Fig. 7.92, determine:
    a. I_D.
    b. V_D and V_S.
    c. V_{GS}.

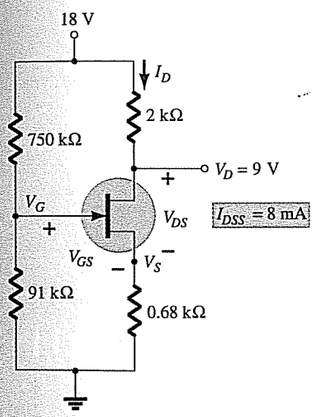


FIG. 7.90
Problem 14.

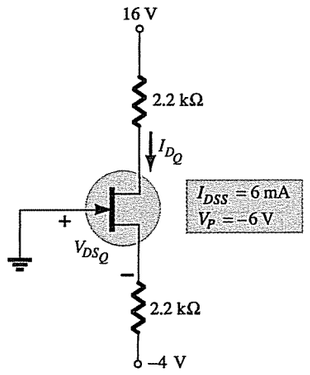


FIG. 7.91
Problems 15 and 37.

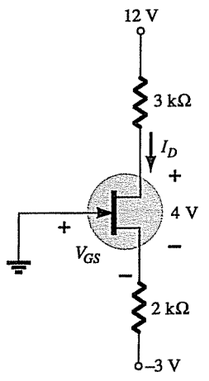


FIG. 7.92
Problem 16.

7.5 Depletion-Type MOSFETs

17. For the self-bias configuration of Fig. 7.93, determine:
    a. I_{D_Q} and V_{GS_Q}.
    b. V_{DS} and V_D.
*18. For the network of Fig. 7.94, determine:
    a. I_{D_Q} and V_{GS_Q}.
    b. V_{DS} and V_S.

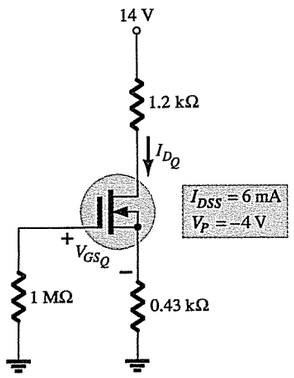


FIG. 7.93
Problem 17.

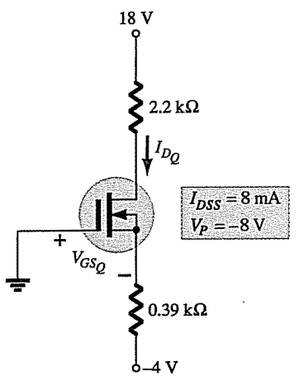


FIG. 7.94
Problem 18.

7.6 Enhancement-Type MOSFETs

19. For the network of Fig. 7.95, determine:
    a. I_{D_Q}.
    b. V_{GS_Q} and V_{DS_Q}.
    c. V_D and V_S.
    d. V_{DS}.
20. For the voltage-divider configuration of Fig. 7.96, determine:
    a. I_{D_Q} and V_{GS_Q}.
    b. V_D and V_S.

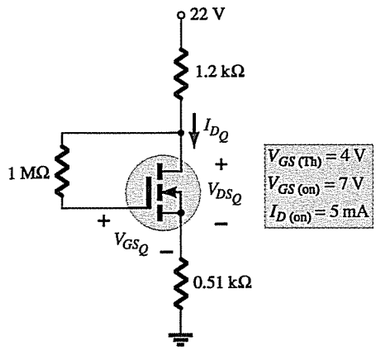


FIG. 7.95
Problem 19.

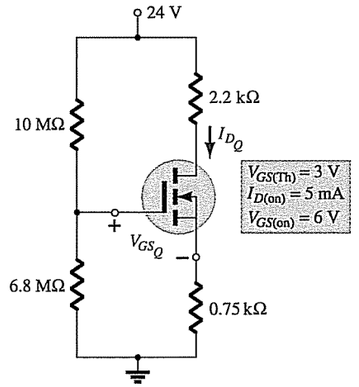


FIG. 7.96
Problem 20.

7.8 Combination Networks

*21. For the network of Fig. 7.97, determine:
    a. V_G.
    b. V_{GS_Q} and I_{D_Q}.
    c. I_E.
    d. I_B.
    e. V_D.
    f. V_C.

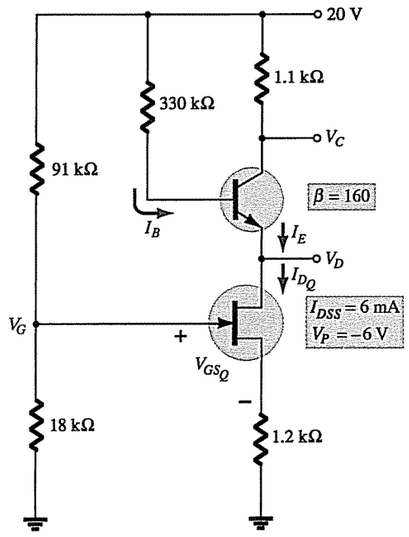


FIG. 7.97
Problem 21.

*22. For the combination network of Fig. 7.98, determine:
- a. V_B and V_G.
- b. V_E.
- c. I_E, I_C, and I_D.
- d. I_B.
- e. V_C, V_S, and V_D.
- f. V_{CE}.
- g. V_{DS}.

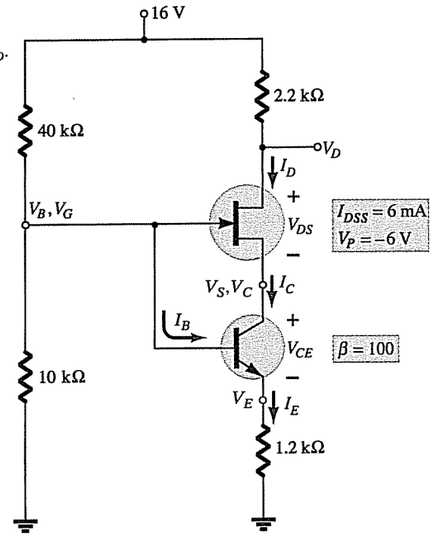


FIG. 7.98
Problem 22.

7.9 Design

*23. Design a self-bias network using a JFET transistor with $I_{DSS} = 8$ mA and $V_P = -6$ V to have a Q-point at $I_{D_Q} = 4$ mA using a supply of 14 V. Assume that $R_D = 3R_S$ and use standard values.

*24. Design a voltage-divider bias network using a depletion-type MOSFET with $I_{DSS} = 10$ mA and $V_P = -4$ V to have a Q-point at $I_{D_Q} = 2.5$ mA using a supply of 24 V. In addition, set $V_G = 4$ V and use $R_D = 2.5R_S$ with $R_1 = 22\,\text{M}\Omega$. Use standard values.

25. Design a network such as appears in Fig. 7.40 using an enhancement-type MOSFET with $V_{GS(\text{Th})} = 4$ V and $k = 0.5 \times 10^{-3}\,A/V^2$ to have a Q-point of $I_{D_Q} = 6$ mA. Use a supply of 16 V and standard values.

7.10 Troubleshooting

*26. What do the readings for each configuration of Fig. 7.99 suggest about the operation of the network?

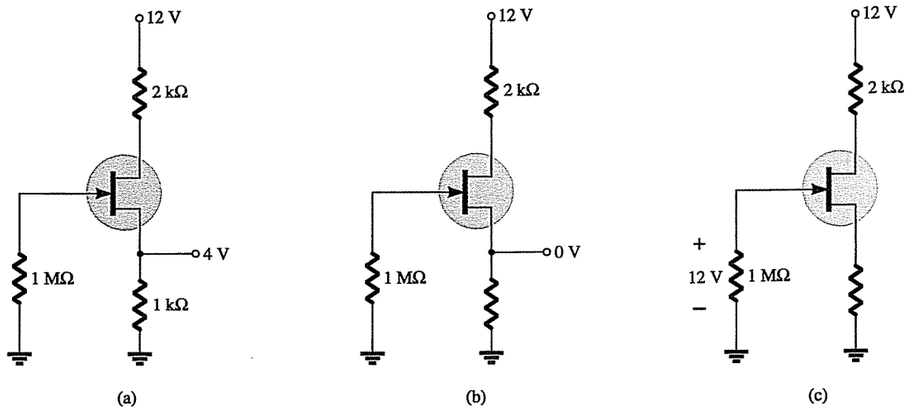


FIG. 7.99
Problem 26.

*27. Although the readings of Fig. 7.100 initially suggest that the network is behaving properly, determine a possible cause for the undesirable state of the network.

*28. The network of Fig. 7.101 is not operating properly. What is the specific cause for its failure?

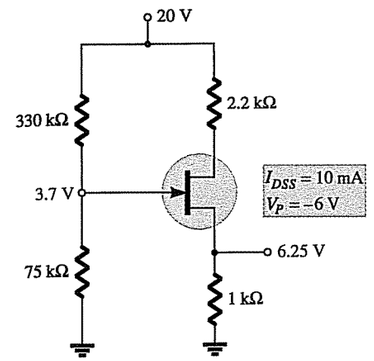


FIG. 7.100
Problem 27.

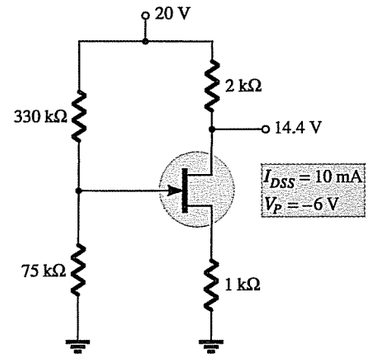


FIG. 7.101
Problem 28.

7.11 *p*-Channel FETs

29. For the network of Fig. 7.102, determine:
- a. I_{D_Q} and V_{GS_Q}.
- b. V_{DS}.
- c. V_D.

30. For the network of Fig. 7.103, determine:
- a. I_{D_Q} and V_{GS_Q}.
- b. V_{DS}.
- c. V_D.

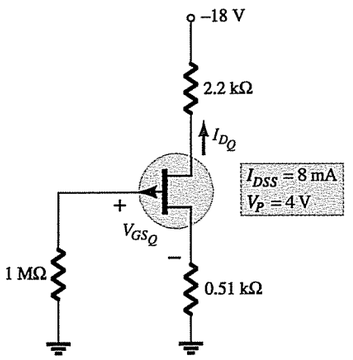


FIG. 7.102
Problem 29.

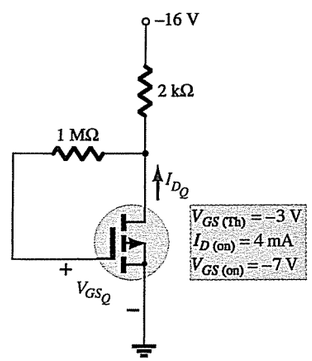


FIG. 7.103
Problem 30.

7.12 Universal JFET Bias Curve

31. Repeat Problem 1 using the universal JFET bias curve.
32. Repeat Problem 6 using the universal JFET bias curve.
33. Repeat Problem 12 using the universal JFET bias curve.
34. Repeat Problem 15 using the universal JFET bias curve.

7.15 Computer Analysis

35. Perform a PSpice Windows analysis of the network of Problem 1.
36. Perform a PSpice Windows analysis of the network of Problem 6.
37. Perform a Multisim analysis of the network of Problem 15.
38. Perform a Multisim analysis of the network of Problem 30.

8 FET Amplifiers

CHAPTER OUTLINE

8.1 Introduction
8.2 FET Small-Signal Model
8.3 JFET Fixed-Bias Configuration
8.4 JFET Self-Bias Configuration
8.5 JFET Voltage-Divider Configuration
8.6 JFET Source-Follower (Common-Drain) Configuration
8.7 JFET Common-Gate Configuration
8.8 Depletion-Type MOSFETs
8.9 Enhancement-Type MOSFETs
8.10 E-MOSFET Drain-Feedback Configuration
8.11 E-MOSFET Voltage-Divider Configuration
8.12 Designing FET Amplifier Networks
8.13 Summary Table
8.14 Effect of R_L and R_{sig}
8.15 Cascade Configuration
8.16 Troubleshooting
8.17 Practical Applications
8.18 Summary
8.19 Computer Analysis

8.1 INTRODUCTION

Field-effect transistor amplifiers provide an excellent voltage gain with the added feature of a high input impedance. They are also low-power-consumption configurations with good frequency range and minimal size and weight. JFETs, depletion MOSFETs, and MESFETs can be used to design amplifiers having similar voltage gains. The depletion MOSFET (MESFET) circuit, however, has a much higher input impedance than a similar JFET configuration.

Whereas a BJT device controls a large output (collector) current by means of a relatively small input (base) current, the FET device controls an output (drain) current by means of a small input (gate-voltage) voltage. In general, therefore, the BJT is a *current-controlled* device and the FET is a *voltage-controlled* device. In both cases, however, note that the output current is the controlled variable. Because of the high input characteristic of FETs, the ac equivalent model is somewhat simpler than that employed for BJTs. Whereas the BJT has an amplification factor, β (beta), the FET has a transconductance factor, g_m.

The FET can be used as a linear amplifier or as a digital device in logic circuits. In fact, the enhancement MOSFET is quite popular in digital circuitry, especially in CMOS circuits that require very low power consumption. FET devices are also widely used in high-frequency applications and in buffering (interfacing) applications. Table 8.1 in Section 8.13 provides a summary of FET small-signal amplifier circuits and related formulas.

Although the common-source configuration is the most popular one, providing an inverted, amplified signal, one also finds common-drain (source-follower) circuits providing unity gain with no inversion and common-gate circuits providing gain with no inversion. As with BJT amplifiers, the important circuit features described in this chapter include voltage gain, input impedance, and output impedance. Due to the very high input impedance, the input current is generally assumed to be 0 μA and the current gain is an undefined quantity. Whereas the voltage gain of an FET amplifier is generally less than that obtained using a BJT amplifier, the FET amplifier provides a much higher input impedance than that of a BJT configuration. Output impedance values are comparable for both BJT and FET circuits.

FET ac amplifier networks can also be analyzed using computer software. Using PSpice or Multisim, one can perform a dc analysis to obtain the circuit bias conditions and an ac analysis to determine the small-signal voltage gain. Using PSpice transistor models, one can analyze the circuit using specific transistor models. On the other hand, one can develop a program using a language such as C++ that can perform both the dc and ac analyses and provide the results in a very special format.

8.2 FET SMALL-SIGNAL MODEL

The ac analysis of an FET configuration requires that a small-signal ac model for the FET be developed. A major component of the ac model will reflect the fact that an ac voltage applied to the input gate-to-source terminals will control the level of current from drain to source.

The gate-to-source voltage controls the drain-to-source (channel) current of an FET.

Recall from Chapter 7 that a dc gate-to-source voltage controls the level of dc drain current through a relationship known as Shockley's equation: $I_D = I_{DSS}(1 - V_{GS}/V_P)^2$. The *change* in collector current that will result from a *change* in gate-to-source voltage can be determined using the transconductance factor g_m in the following manner:

$$\boxed{\Delta I_D = g_m \Delta V_{GS}} \tag{8.1}$$

The prefix *trans-* in the terminology applied to g_m reveals that it establishes a relationship between an output and an input quantity. The root word *conductance* was chosen because g_m is determined by a voltage-to-current ratio similar to the ratio that defines the conductance of a resistor, $G = 1/R = I/V$.

Solving for g_m in Eq. (8.1), we have

$$\boxed{g_m = \frac{\Delta I_D}{\Delta V_{GS}}} \tag{8.2}$$

Graphical Determination of g_m

If we now examine the transfer characteristics of Fig. 8.1, we find that g_m is actually the slope of the characteristics at the point of operation. That is,

$$\boxed{g_m = m = \frac{\Delta y}{\Delta x} = \frac{\Delta I_D}{\Delta V_{GS}}} \tag{8.3}$$

Following the curvature of the transfer characteristics, it is reasonably clear that the slope and, therefore, g_m increase as we progress from V_P to I_{DSS}. In other words, as V_{GS} approaches 0 V, the magnitude of g_m increases.

Equation (8.2) reveals that g_m can be determined at any Q-point on the transfer characteristics by simply choosing a finite increment in V_{GS} (or in I_D) about the Q-point and then finding the corresponding change in I_D (or V_{GS}, respectively). The resulting changes in each quantity are then substituted in Eq. (8.2) to determine g_m.

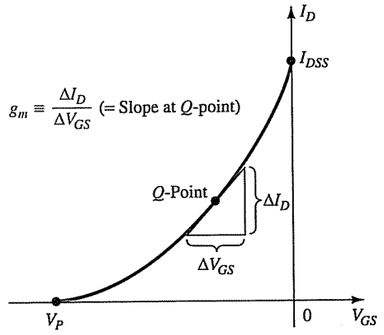


FIG. 8.1
Definition of g_m using transfer characteristic.

EXAMPLE 8.1 Determine the magnitude of g_m for a JFET with $I_{DSS} = 8$ mA and $V_P = -4$ V at the following dc bias points:

a. $V_{GS} = -0.5$ V.
b. $V_{GS} = -1.5$ V.
c. $V_{GS} = -2.5$ V.

Solution: The transfer characteristics are generated as Fig. 8.2 using the procedure defined in Chapter 7. Each operating point is then identified and a tangent line is drawn at each point to best reflect the slope of the transfer curve in this region. An appropriate increment is then chosen for V_{GS} to reflect a variation to either side of each Q-point. Equation (8.2) is then applied to determine g_m.

a. $g_m = \dfrac{\Delta I_D}{\Delta V_{GS}} \cong \dfrac{2.1\text{ mA}}{0.6\text{ V}} = \mathbf{3.5\text{ mS}}$

b. $g_m = \dfrac{\Delta I_D}{\Delta V_{GS}} \cong \dfrac{1.8\text{ mA}}{0.7\text{ V}} \cong \mathbf{2.57\text{ mS}}$

c. $g_m = \dfrac{\Delta I_D}{\Delta V_{GS}} = \dfrac{1.5\text{ mA}}{1.0\text{ V}} = \mathbf{1.5\text{ mS}}$

Note the decrease in g_m as V_{GS} approaches V_P.

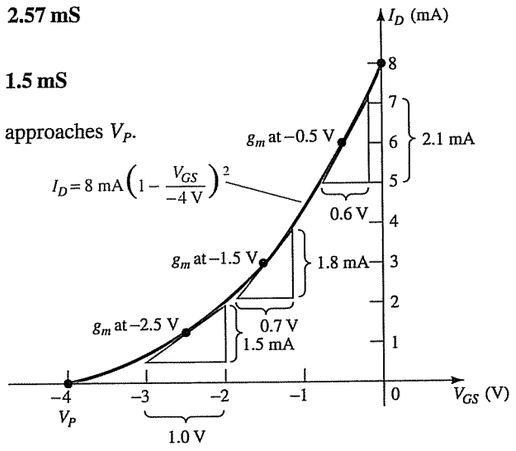


FIG. 8.2
Calculating g_m at various bias points.

Mathematical Definition of g_m

The graphical procedure just described is limited by the accuracy of the transfer plot and the care with which the changes in each quantity can be determined. Naturally, the larger the graph, the better is the accuracy, but this can then become a cumbersome problem. An alternative approach to determining g_m employs the approach used to find the ac resistance of a diode in Chapter 1, where it was stated that:

The derivative of a function at a point is equal to the slope of the tangent line drawn at that point.

If we therefore take the derivative of I_D with respect to V_{GS} (differential calculus) using Shockley's equation, we can derive an equation for g_m as follows:

$$g_m = \left.\frac{dI_D}{dV_{GS}}\right|_{Q\text{-pt.}} = \frac{d}{dV_{GS}}\left[I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2\right]$$
$$= I_{DSS}\frac{d}{dV_{GS}}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 2I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]\frac{d}{dV_{GS}}\left(1 - \frac{V_{GS}}{V_P}\right)$$
$$= 2I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]\left[\frac{d}{dV_{GS}}(1) - \frac{1}{V_P}\frac{dV_{GS}}{dV_{GS}}\right] = 2I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]\left[0 - \frac{1}{V_P}\right]$$

and

$$g_m = \frac{2I_{DSS}}{|V_P|}\left[1 - \frac{V_{GS}}{V_P}\right] \tag{8.4}$$

where $|V_P|$ denotes magnitude only, to ensure a positive value for g_m.

It was mentioned earlier that the slope of the transfer curve is a maximum at $V_{GS} = 0$ V. Plugging in $V_{GS} = 0$ V into Eq. (8.4) results in the following equation for the maximum value of g_m for a JFET in which I_{DSS} and V_P have been specified:

$$g_m = \frac{2I_{DSS}}{|V_P|}\left[1 - \frac{0}{V_P}\right]$$

and

$$\boxed{g_{m0} = \frac{2I_{DSS}}{|V_P|}} \tag{8.5}$$

where the added subscript 0 reminds us that it is the value of g_m when $V_{GS} = 0$ V. Equation (8.4) then becomes

$$\boxed{g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right]} \tag{8.6}$$

EXAMPLE 8.2 For the JFET having the transfer characteristics of Example 8.1:

a. Find the maximum value of g_m.
b. Find the value of g_m at each operating point of Example 8.1 using Eq. (8.6) and compare with the graphical results.

Solution:

a. $g_{m0} = \dfrac{2I_{DSS}}{|V_P|} = \dfrac{2(8\text{ mA})}{4\text{ V}} = \mathbf{4\text{ mS}}$ (maximum possible value of g_m)

b. At $V_{GS} = -0.5$ V,

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right] = 4\text{ mS}\left[1 - \frac{-0.5\text{ V}}{-4\text{ V}}\right] = \mathbf{3.5\text{ mS}}$$ (vs. 3.5 mS graphically)

At $V_{GS} = -1.5$ V,

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right] = 4\text{ mS}\left[1 - \frac{-1.5\text{ V}}{-4\text{ V}}\right] = \mathbf{2.5\text{ mS}}$$ (vs. 2.57 mS graphically)

At $V_{GS} = -2.5$ V,

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right] = 4\text{ mS}\left[1 - \frac{-2.5\text{ V}}{-4\text{ V}}\right] = \mathbf{1.5\text{ mS}}$$ (vs. 1.5 mS graphically)

The results of Example 8.2 are certainly sufficiently close to validate Eq. (8.4) through (8.6) for future use when g_m is required.

On specification sheets, g_m is provided as y_{fs}, where y indicates it is part of an admittance equivalent circuit. The f signifies *f*orward transfer parameter, and the s indicates that it is connected to the *s*ource terminal.

In equation form,

$$\boxed{g_m = y_{fs}} \tag{8.7}$$

For the JFET of Fig. 6.18, y_{fs} ranges from 1000 to 5000 μS, or 1 to 5 mS.

Plotting g_m versus V_{GS}

Since the factor $\left(1 - \frac{V_{GS}}{V_P}\right)$ of Eq. (8.6) is less than 1 for any value of V_{GS} other than 0 V, the magnitude of g_m will decrease as V_{GS} approaches V_P and the ratio $\frac{V_{GS}}{V_P}$ increases in magnitude. At $V_{GS} = V_P$, $g_m = g_{m0}(1 - 1) = 0$. Equation (8.6) defines a straight line with a minimum value of 0 and a maximum value of g_m, as shown by the plot of Fig. 8.3.

Figure 8.3 also shows that when V_{GS} is one-half the pinch-off value, g_m is one-half the maximum value.

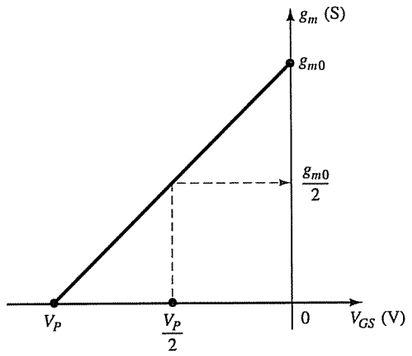


FIG. 8.3
Plot of g_m versus V_{GS}.

EXAMPLE 8.3 Plot g_m versus V_{GS} for the JFET of Examples 8.1 and 8.2.

Solution: Note Fig. 8.4.

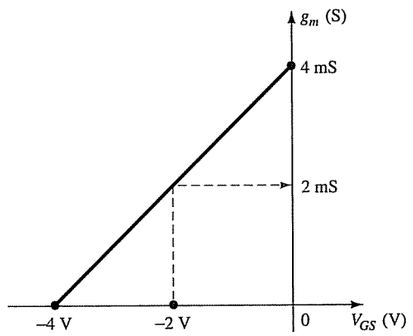


FIG. 8.4
Plot of g_m versus V_{GS} for a JFET with I_{DSS} = 8 mA and $V_P = -4$ V.

Effect of I_D on g_m

A mathematical relationship between g_m and the dc bias current I_D can be derived by noting that Shockley's equation can be written in the following form:

$$\boxed{1 - \frac{V_{GS}}{V_P} = \sqrt{\frac{I_D}{I_{DSS}}}} \tag{8.8}$$

Substituting Eq. (8.8) into Eq. (8.6) results in

$$\boxed{g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_P}\right) = g_{m0}\sqrt{\frac{I_D}{I_{DSS}}}} \tag{8.9}$$

Using Eq. (8.9) to determine g_m for a few specific values of I_D, we obtain the following results:

a. If $I_D = I_{DSS}$,

$$g_m = g_{m0}\sqrt{\frac{I_{DSS}}{I_{DSS}}} = \boldsymbol{g_{m0}}$$

b. If $I_D = I_{DSS}/2$,

$$g_m = g_{m0}\sqrt{\frac{I_{DSS}/2}{I_{DSS}}} = \mathbf{0.707}\boldsymbol{g_{m0}}$$

c. If $I_D = I_{DSS}/4$,

$$g_m = g_{m0}\sqrt{\frac{I_{DSS}/4}{I_{DSS}}} = \frac{g_{m0}}{2} = \mathbf{0.5}\boldsymbol{g_{m0}}$$

EXAMPLE 8.4 Plot g_m versus I_D for the JFET of Examples 8.1 through 8.3.

Solution: See Fig. 8.5.

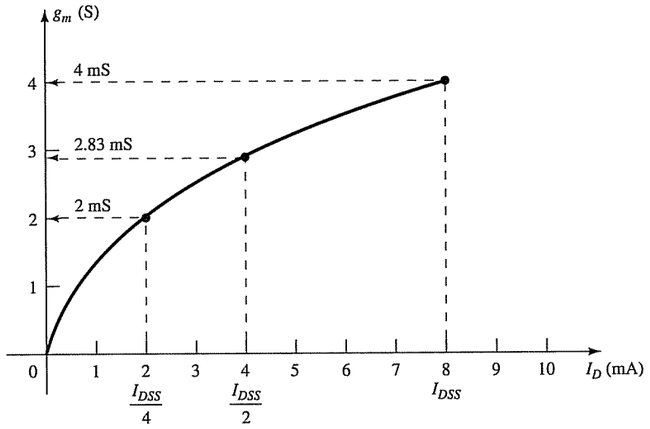


FIG. 8.5
Plot of g_m versus I_D for a JFET with I_{DSS} = 8 mA and $V_{GS} = -4$ V.

The plots of Examples 8.3 and 8.4 clearly reveal that the highest values of g_m are obtained when V_{GS} approaches 0 V and I_D approaches its maximum value of I_{DSS}.

FET Input Impedance Z_i

The input impedance of all commercially available FETs is sufficiently large to assume that the input terminals approximate an open circuit. In equation form,

$$Z_i\,(\text{FET}) = \infty\ \Omega \tag{8.10}$$

For a JFET a practical value of $10^9\ \Omega$ ($1000\ \text{M}\Omega$) is typical, whereas a value of $10^{12}\ \Omega$ to $10^{15}\ \Omega$ is typical for MOSFETs and MESFETs.

FET Output Impedance Z_o

The output impedance of FETs is similar in magnitude to that of conventional BJTs. On FET specification sheets, the output impedance will typically appear as y_{os} with the units of μS. The parameter y_{os} is a component of an *admittance equivalent circuit*, with the subscript o signifying an *o*utput network parameter and s the terminal (*s*ource) to which it is attached in the model. For the JFET of Fig. 6.18, y_{os} has a range of $10\ \mu$S to $50\ \mu$S or $20\ \text{k}\Omega$ ($R = 1/G = 1/50\ \mu\text{S}$) to $100\ \text{k}\Omega$ ($R = 1/G = 1/10\ \mu\text{S}$).

In equation form,

$$Z_o\,(\text{FET}) = r_d = \frac{1}{y_{os}} \tag{8.11}$$

The output impedance is defined on the characteristics of Fig. 8.6 as the slope of the horizontal characteristic curve at the point of operation. The more horizontal the curve, the greater is the output impedance. If it is perfectly horizontal, the ideal situation is on hand with the output impedance being infinite (an open circuit)—an often applied approximation.

In equation form,

$$r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}=\text{constant}} \tag{8.12}$$

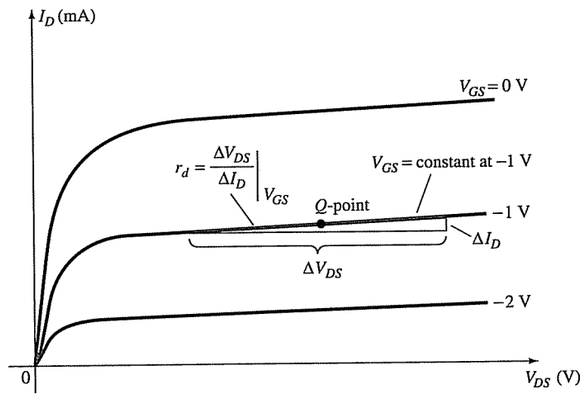


FIG. 8.6
Definition of r_d using FET drain characteristics.

Note the requirement when applying Eq. (8.12) that the voltage V_{GS} remain constant when r_d is determined. This is accomplished by drawing a straight line approximating the V_{GS} line at the point of operation. A ΔV_{DS} or ΔI_D is then chosen and the other quantity measured off for use in the equation.

EXAMPLE 8.5 Determine the output impedance for the FET of Fig. 8.7 for $V_{GS} = 0$ V and $V_{GS} = -2$ V at $V_{DS} = 8$ V.

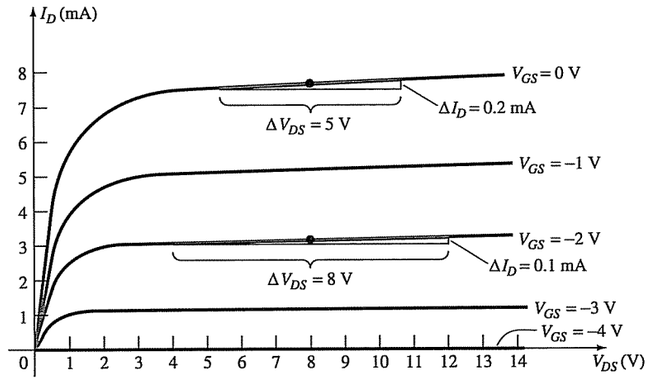


FIG. 8.7
Drain characteristics used to calculate r_d in Example 8.5.

Solution: For $V_{GS} = 0$ V, a tangent line is drawn and ΔV_{DS} is chosen as 5 V, resulting in a ΔI_D of 0.2 mA. Substituting into Eq. (8.12), we find

$$r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}=0\,\text{V}} = \frac{5\ \text{V}}{0.2\ \text{mA}} = \mathbf{25\ k\Omega}$$

For $V_{GS} = -2$ V, a tangent line is drawn and ΔV_{DS} is chosen as 8 V, resulting in a ΔI_D of 0.1 mA. Substituting into Eq. (8.12), we find

$$r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}=-2\,\text{V}} = \frac{8\ \text{V}}{0.1\ \text{mA}} = \mathbf{80\ k\Omega}$$

which shows that r_d does change from one operating region to another, with lower values typically occurring at lower levels of V_{GS} (closer to 0 V).

FET AC Equivalent Circuit

Now that the important parameters of an ac equivalent circuit have been introduced and discussed, a model for the FET transistor in the ac domain can be constructed. The control of I_d by V_{gs} is included as a current source $g_m V_{gs}$ connected from drain to source as shown in Fig. 8.8. The current source has its arrow pointing from drain to source to establish a 180° phase shift between output and input voltages as will occur in actual operation.

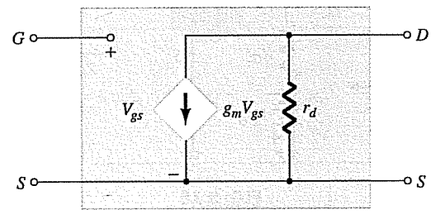


FIG. 8.8
FET ac equivalent circuit.

The input impedance is represented by the open circuit at the input terminals and the output impedance by the resistor r_d from drain to source. Note that the gate-to-source voltage is now represented by V_{gs} (lower-case subscripts) to distinguish it from dc levels. In addition, note that the source is common to both input and output circuits, whereas the gate and drain terminals are only in "touch" through the controlled current source $g_m V_{gs}$.

In situations where r_d is ignored (assumed sufficiently large in relation to other elements of the network to be approximated by an open circuit), the equivalent circuit is simply a current source whose magnitude is controlled by the signal V_{gs} and parameter g_m—clearly a voltage-controlled device.

EXAMPLE 8.6 Given $y_{fs} = 3.8\text{ mS}$ and $y_{os} = 20\ \mu\text{S}$, sketch the FET ac equivalent model.

Solution:

$$g_m = y_{fs} = 3.8\text{ mS} \quad \text{and} \quad r_d = \frac{1}{y_{os}} = \frac{1}{20\ \mu\text{S}} = 50\text{ k}\Omega$$

resulting in the ac equivalent model of Fig. 8.9.

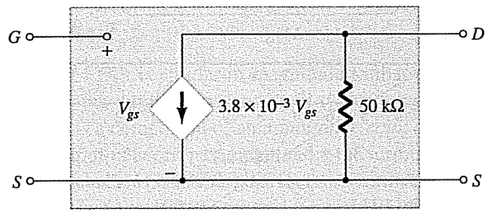


FIG. 8.9
FET ac equivalent model for Example 8.6.

8.3 JFET FIXED-BIAS CONFIGURATION

Now that the FET equivalent circuit has been defined, a number of fundamental FET small-signal configurations are investigated. The approach parallels the ac analysis of BJT amplifiers with a determination of the important parameters of Z_i, Z_o, and A_v for each configuration.

The *fixed-bias* configuration of Fig. 8.10 includes the coupling capacitors C_1 and C_2, which isolate the dc biasing arrangement from the applied signal and load; they act as short-circuit equivalents for the ac analysis.

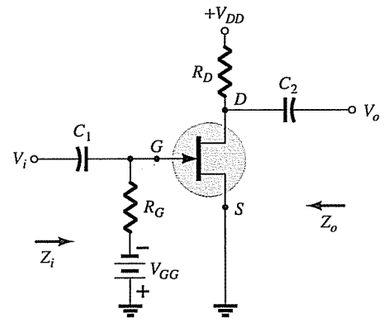


FIG. 8.10
JFET fixed-bias configuration.

Once the levels of g_m and r_d are determined from the dc biasing arrangement, specification sheet, or characteristics, the ac equivalent model can be substituted between the appropriate terminals as shown in Fig. 8.11. Note that both capacitors have the short-circuit equivalent because the reactance $X_C = 1/(2\pi fC)$ is sufficiently small compared to other impedance levels of the network, and the dc batteries V_{GG} and V_{DD} are set to 0 V by a short-circuit equivalent.

The network of Fig. 8.11 is then carefully redrawn as shown in Fig. 8.12. Note the defined polarity of V_{gs}, which defines the direction of $g_m V_{gs}$. If V_{gs} is negative, the direction of the current source reverses. The applied signal is represented by V_i and the output signal across R_D by V_o.

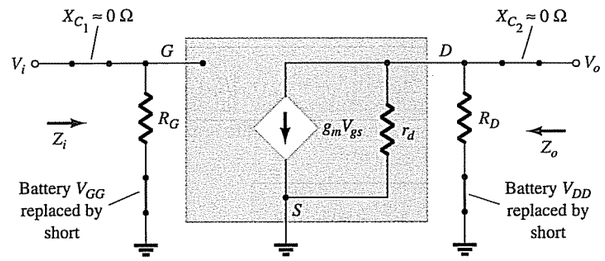


FIG. 8.11
Substituting the JFET ac equivalent circuit unit into the network of Fig. 8.10.

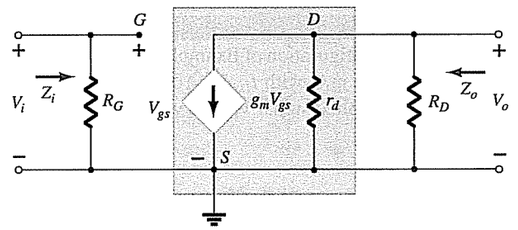


FIG. 8.12
Redrawn network of Fig. 8.11.

Z_i Figure 8.12 clearly reveals that

$$\boxed{Z_i = R_G} \tag{8.13}$$

because of the open-circuit equivalence at the input terminals of the JFET.

Z_o Setting $V_i = 0\text{ V}$ as required by the definition of Z_o will establish V_{gs} as 0 V also. The result is $g_m V_{gs} = 0\text{ mA}$, and the current source can be replaced by an open-circuit equivalent as shown in Fig. 8.13. The output impedance is

$$\boxed{Z_o = R_D \| r_d} \tag{8.14}$$

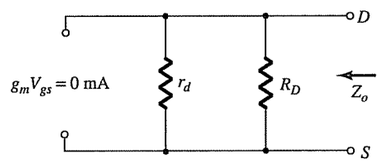


FIG. 8.13
Determining Z_o.

If the resistance r_d is sufficiently large (at least 10:1) compared to R_D, the approximation $r_d \| R_D \cong R_D$ can often be applied and

$$\boxed{Z_o \cong R_D}_{r_d \geq 10R_D} \tag{8.15}$$

A_v Solving for V_o in Fig. 8.12, we find

$$V_o = -g_m V_{gs}(r_d \| R_D)$$

but $$V_{gs} = V_i$$

and $$V_o = -g_m V_i(r_d \| R_D)$$

so that

$$A_v = \frac{V_o}{V_i} = -g_m(r_d \| R_D) \tag{8.16}$$

If $r_d \geq 10R_D$,

$$A_v = \frac{V_o}{V_i} = -g_m R_D \quad r_d \geq 10R_D \tag{8.17}$$

Phase Relationship The negative sign in the resulting equation for A_v clearly reveals a phase shift of 180° between input and output voltages.



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EXAMPLE 8.7 The fixed-bias configuration of Example 7.1 had an operating point defined by $V_{GS_Q} = -2$ V and $I_{D_Q} = 5.625$ mA, with $I_{DSS} = 10$ mA and $V_P = -8$ V. The network is redrawn as Fig. 8.14 with an applied signal V_i. The value of y_{os} is provided as 40 μS.

a. Determine g_m.
b. Find r_d.
c. Determine Z_i.
d. Calculate Z_o.
e. Determine the voltage gain A_v.
f. Determine A_v ignoring the effects of r_d.

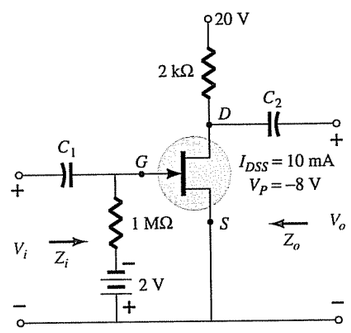


FIG. 8.14
JFET configuration for Example 8.7.

Solution:

a. $g_{m0} = \dfrac{2I_{DSS}}{|V_P|} = \dfrac{2(10\text{ mA})}{8\text{ V}} = 2.5\text{ mS}$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 2.5\text{ mS}\left(1 - \frac{(-2\text{ V})}{(-8\text{ V})}\right) = \mathbf{1.88\text{ mS}}$$

b. $r_d = \dfrac{1}{y_{os}} = \dfrac{1}{40\ \mu\text{S}} = \mathbf{25\text{ k}\Omega}$

c. $Z_i = R_G = \mathbf{1\text{ M}\Omega}$

d. $Z_o = R_D \| r_d = 2\text{ k}\Omega \| 25\text{ k}\Omega = \mathbf{1.85\text{ k}\Omega}$

e. $A_v = -g_m(R_D \| r_d) = -(1.88\text{ mS})(1.85\text{ k}\Omega)$
$= \mathbf{-3.48}$

f. $A_v = -g_m R_D = -(1.88\text{ mS})(2\text{ k}\Omega) = \mathbf{-3.76}$

As demonstrated in part (f), a ratio of 25 kΩ:2 kΩ = 12.5:1 between r_d and R_D results in a difference of 8% in the solution.

Bypassed R_S

The fixed-bias configuration has the distinct disadvantage of requiring two dc voltage sources. The *self-bias* configuration of Fig. 8.15 requires only one dc supply to establish the desired operating point.

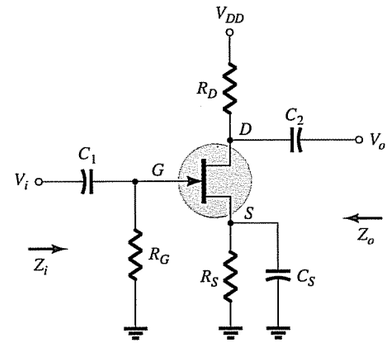


FIG. 8.15
Self-bias JFET configuration.

The capacitor C_S across the source resistance assumes its short-circuit equivalence for dc, allowing R_S to define the operating point. Under ac conditions, the capacitor assumes the short-circuit state and "short circuits" the effects of R_S. If left in the ac, gain will be reduced, as will be shown in the paragraphs to follow.

The JFET equivalent circuit is established in Fig. 8.16 and carefully redrawn in Fig. 8.17.

Since the resulting configuration is the same as appearing in Fig. 8.12, the resulting equations for Z_i, Z_o, and A_v will be the same.

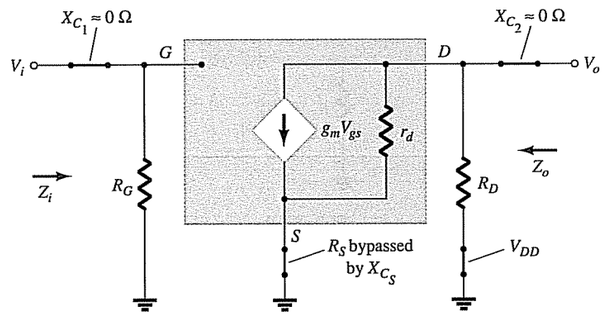


FIG. 8.16
Network of Fig. 8.15 following the substitution of the JFET ac equivalent circuit.

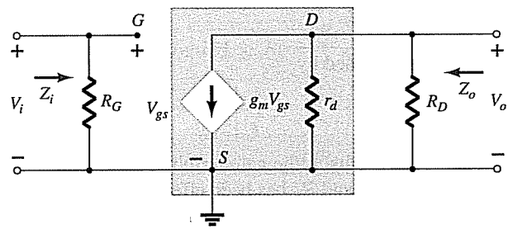


FIG. 8.17
Redrawn network of Fig. 8.16.

Z_i

$$Z_i = R_G \tag{8.18}$$

Z_o

$$Z_o = r_d \| R_D \tag{8.19}$$

If $r_d \geq 10R_D$,

$$Z_o \cong R_D \quad r_d \geq 10R_D \tag{8.20}$$

A_v

$$A_v = -g_m(r_d \| R_D) \tag{8.21}$$

If $r_d \geq 10R_D$,

$$A_v = -g_m R_D \quad r_d \geq 10R_D \tag{8.22}$$

Phase Relationship The negative sign in the solutions for A_v again indicates a phase shift of 180° between V_i and V_o.

Unbypassed R_S

If C_S is removed from Fig 8.15, the resistor R_S will be part of the ac equivalent circuit as shown in Fig. 8.18. In this case, there is no obvious way to reduce the network to lower its level of complexity. In determining the levels of Z_i, Z_o, and A_v, one must be very careful with notation and defined polarities and direction. Initially, the resistance r_d will be left out of the analysis to form a basis for comparison.

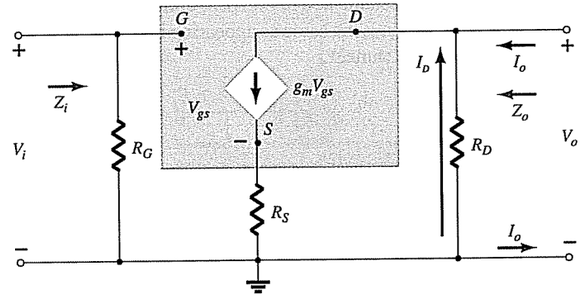


FIG. 8.18
Self-bias JFET configuration including the effects of R_S with $r_d = \infty\Omega$.

Z_i Due to the open-circuit condition between the gate and the output network, the input remains the following:

$$Z_i = R_G \tag{8.23}$$

Z_o The output impedance is defined by

$$Z_o = \left.\frac{V_o}{I_o}\right|_{V_i=0}$$

Setting $V_i = 0$ V in Fig. 8.18 results in the gate terminal being at ground potential (0 V). The voltage across R_G is then 0 V, and R_G has been effectively "shorted out" of the picture.

Applying Kirchhoff's current law results in

$$I_o + I_D = g_m V_{gs}$$

with

$$V_{gs} = -(I_o + I_D)R_S$$

so that

$$I_o + I_D = -g_m(I_o + I_D)R_S = -g_m I_o R_S - g_m I_D R_S$$

or

$$I_o[1 + g_m R_S] = -I_D[1 + g_m R_S]$$

and

$$I_o = -I_D \quad \text{(the controlled current source } g_m V_{gs} = 0 \text{ A for the applied conditions)}$$

Since

$$V_o = -I_D R_D$$

then

$$V_o = -(-I_o)R_D = I_o R_D$$

and

$$Z_o = \frac{V_o}{I_o} = R_D \quad r_d = \infty\,\Omega \tag{8.24}$$

If r_d is included in the network, the equivalent will appear as shown in Fig. 8.19.

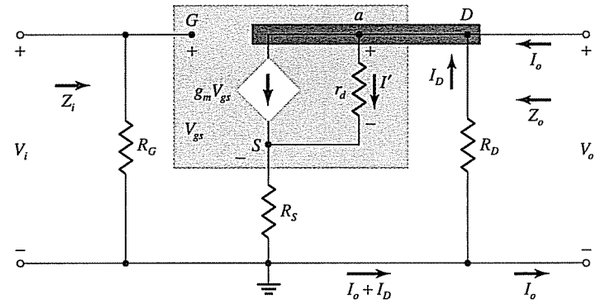


FIG. 8.19
Including the effects of r_d in the self-bias JFET configuration.

Since

$$Z_o = \left.\frac{V_o}{I_o}\right|_{V_i=0\text{ V}} = -\frac{I_D R_D}{I_o}$$

we should try to find an expression for I_o in terms of I_D.

Applying Kirchhoff's current law, we have

$$I_o = g_m V_{gs} + I_{r_d} - I_D$$

but

$$V_{r_d} = V_o + V_{gs}$$

and

$$I_o = g_m V_{gs} + \frac{V_o + V_{gs}}{r_d} - I_D$$

or

$$I_o = \left(g_m + \frac{1}{r_d}\right)V_{gs} - \frac{I_D R_D}{r_d} - I_D \text{ using } V_o = -I_D R_D$$

Now,

$$V_{gs} = -(I_D + I_o)R_S$$

so that

$$I_o = -\left(g_m + \frac{1}{r_d}\right)(I_D + I_o)R_S - \frac{I_D R_D}{r_d} - I_D$$

with the result that

$$I_o\left[1 + g_m R_S + \frac{R_S}{r_d}\right] = -I_D\left[1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d}\right]$$

or

$$I_o = \frac{-I_D\left[1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d}\right]}{1 + g_m R_S + \frac{R_S}{r_d}}$$

and

$$Z_o = \frac{V_o}{I_o} = \frac{-I_D R_D}{-I_D\left(1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d}\right)}{1 + g_m R_S + \frac{R_S}{r_d}}$$

and finally,

$$Z_o = \frac{\left[1 + g_m R_S + \frac{R_S}{r_d}\right]}{\left[1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d}\right]} R_D \qquad \textbf{(8.25a)}$$

For $r_d \geq 10R_D$,

$$\left(1 + g_m R_S + \frac{R_S}{r_d}\right) \gg \frac{R_D}{r_d} \quad \text{and} \quad 1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d} \cong 1 + g_m R_S + \frac{R_S}{r_d}$$

and

$$\boxed{Z_o = R_D}_{r_d \geq 10R_D} \qquad \textbf{(8.25b)}$$

***A*$_v$** For the network of Fig. 8.19, application of Kirchhoff's voltage law to the input circuit results in

$$V_i - V_{gs} - V_{R_S} = 0$$
$$V_{gs} = V_i - I_D R_S$$

The voltage across r_d using Kirchhoff's voltage law is

$$V_{r_d} = V_o - V_{R_S}$$

and

$$I' = \frac{V_{r_d}}{r_d} = \frac{V_o - V_{R_S}}{r_d}$$

so that application of Kirchhoff's current law results in

$$I_D = g_m V_{gs} + \frac{V_o - V_{R_S}}{r_d}$$

Substituting for V_{gs} from above and substituting for V_o and V_{R_S}, we have

$$I_D = g_m[V_i - I_D R_S] + \frac{(-I_D R_D) - (I_D R_S)}{r_d}$$

so that

$$I_D\left[1 + g_m R_S + \frac{R_D + R_S}{r_d}\right] = g_m V_i$$

or

$$I_D = \frac{g_m V_i}{1 + g_m R_S + \frac{R_D + R_S}{r_d}}$$

The output voltage is then

$$V_o = -I_D R_D = -\frac{g_m R_D V_i}{1 + g_m R_S + \frac{R_D + R_S}{r_d}}$$

and

$$\boxed{A_v = \frac{V_o}{V_i} = -\frac{g_m R_D}{1 + g_m R_S + \frac{R_D + R_S}{r_d}}} \qquad \textbf{(8.26)}$$

Again, if $r_d \geq 10(R_D + R_S)$,

$$\boxed{A_v = \frac{V_o}{V_i} = -\frac{g_m R_D}{1 + g_m R_S}}_{r_d \geq 10(R_D + R_S)} \qquad \textbf{(8.27)}$$

Phase Relationship The negative sign in Eq. (8.26) again reveals that a 180° phase shift will exist between V_i and V_o.

EXAMPLE 8.8 The self-bias configuration of Example 7.2 has an operating point defined by $V_{GS_Q} = -2.6$ V and $I_{D_Q} = 2.6$ mA, with $I_{DSS} = 8$ mA and $V_P = -6$ V. The network is redrawn as Fig. 8.20 with an applied signal V_i. The value of y_{os} is given as 20 μS.


PSpice

a. Determine g_m.
b. Find r_d.
c. Find Z_i.
d. Calculate Z_o with and without the effects of r_d. Compare the results.
e. Calculate A_v with and without the effects of r_d. Compare the results.

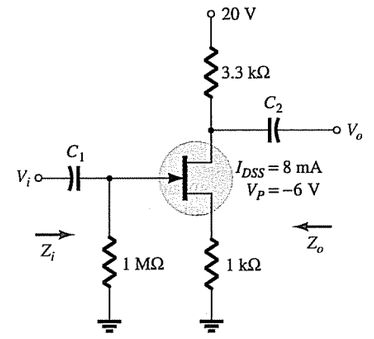


FIG. 8.20
Network for Example 8.8.

Solution:

a. $g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(8\text{ mA})}{6\text{ V}} = 2.67\text{ mS}$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 2.67\text{ mS}\left(1 - \frac{(-2.6\text{ V})}{(-6\text{ V})}\right) = \mathbf{1.51\text{ mS}}$$

b. $r_d = \frac{1}{y_{os}} = \frac{1}{20\,\mu\text{S}} = \mathbf{50\,k\Omega}$

c. $Z_i = R_G = \mathbf{1\,M\Omega}$

d. With r_d,

$$r_d = 50\,\text{k}\Omega > 10R_D = 33\,\text{k}\Omega$$

Therefore,

$$Z_o = R_D = \mathbf{3.3\,k\Omega}$$

If $r_d = \infty\Omega$,

$$Z_o = R_D = \mathbf{3.3\,k\Omega}$$

e. With r_d,

$$A_v = \frac{-g_m R_D}{1 + g_m R_S + \frac{R_D + R_S}{r_d}} = \frac{-(1.51\text{ mS})(3.3\,\text{k}\Omega)}{1 + (1.51\text{ mS})(1\,\text{k}\Omega) + \frac{3.3\,\text{k}\Omega + 1\,\text{k}\Omega}{50\,\text{k}\Omega}}$$
$$= \mathbf{-1.92}$$

Without r_d,

$$A_v = \frac{-g_m R_D}{1 + g_m R_S} = \frac{-(1.51\text{ mS})(3.3\,\text{k}\Omega)}{1 + (1.51\text{ mS})(1\,\text{k}\Omega)} = \mathbf{-1.98}$$

As above, the effect of r_d is minimal because the condition $r_d \geq 10(R_D + R_S)$ is satisfied.

Note also that the typical gain of a JFET amplifier is less than that generally encountered for BJTs of similar configurations. Keep in mind, however, that Z_i is magnitudes greater than the typical Z_i of a BJT, which will have a very positive effect on the overall gain of a system.

Mathcad

The complexity of some of the equations for the unbypassed source resistance suggests that it might be a good opportunity to employ Mathcad. In fact, the results of Example 8.8 will be verified using equations introduced in Chapter 7 and in this chapter. The analysis will proceed in a manner that permits a quick change in the parameter list so that any network of this configuration can be analyzed in short order. To this end, note that the first line of Fig. 8.21 is a list of all the elements of the network. In the future, the user simply has to change the parameter list, and Mathcad will quickly generate the new results without the user's having to enter all the equations again. The next line is a list of **Guess** values for the quantities to be calculated to help with the iteration process. As described in Chapter 7, **Given** must then be entered, followed by the equations that will generate the desired unknowns. Lastly, the **Find** statement in the format shown will direct the software to determine the quantities appearing within the brackets. As soon as the equal sign is selected, the results will appear in an order that matches the listing within the **Find** brackets. Note that the resulting drain current is 2.588 mA to match the 2.6 mA of Example 8.2, and V_{GS} is -2.588 V to match the -2.6 V of the same example. The resulting value of g_m is 1.517 mS to match the 1.51 mS of Example 8.8, and the overall gain is -1.923, which compares well with the calculated result of -1.98.

One of the most confusing elements of Mathcad can be which equal sign to use for which operation. All the parameters of the first two lines used the equal sign generated by **Shift:**, and all the boldface equal signs in the defining equations come from **Ctrl** =. Following the **Find** statement, the keyboard equal sign is employed.

There is no question that it takes some time to get used to entering complex equations such as appearing in Fig. 8.21, but be assured that the skills will develop quickly. As mentioned above, if any of the parameters such as **IDSS** and **VP** should change, all that has to be done is to retrieve the program from memory and change those two values; the new results for the four quantities will appear almost instantaneously—a real time-saver.

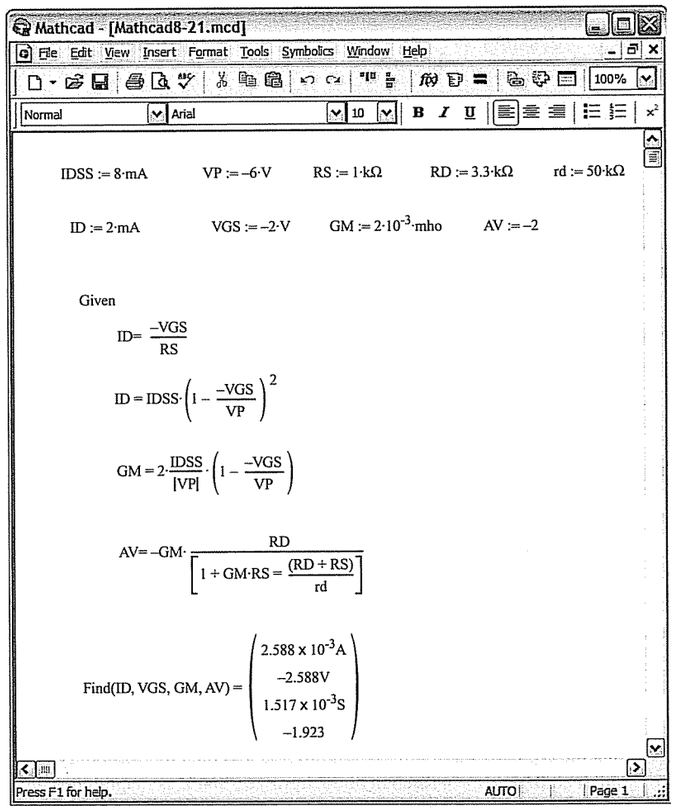


FIG. 8.21
Parameters and equations for Example 8.8 using Mathcad.

8.5 JFET VOLTAGE-DIVIDER CONFIGURATION

The popular voltage-divider configuration for BJTs can also be applied to JFETs as demonstrated in Fig. 8.22.

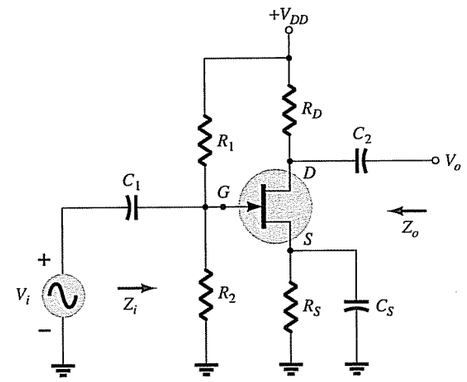


FIG. 8.22
JFET voltage-divider configuration.

Substituting the ac equivalent model for the JFET results in the configuration of Fig. 8.23. Replacing the dc supply V_{DD} by a short-circuit equivalent has grounded one end of R_1 and R_D. Since each network has a common ground, R_1 can be brought down in parallel with R_2 as shown in Fig. 8.24. R_D can also be brought down to ground, but in the output circuit across r_d. The resulting ac equivalent network now has the basic format of some of the networks already analyzed.

Z_i R_1 and R_2 are in parallel with the open-circuit equivalence of the JFET, resulting in

$$Z_i = R_1 \| R_2 \tag{8.28}$$

Z_o Setting $V_i = 0$ V sets V_{gs} and $g_m V_{gs}$ to zero, and

$$Z_o = r_d \| R_D \tag{8.29}$$

For $r_d \geq 10R_D$,

$$Z_o \cong R_D \quad r_d \geq 10R_D \tag{8.30}$$

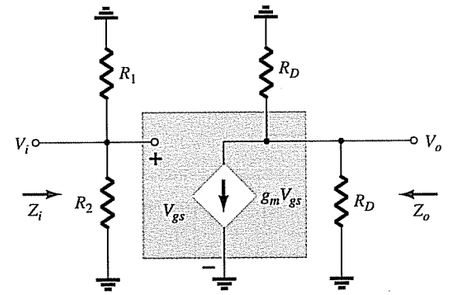


FIG. 8.23
Network of Fig. 8.22 under ac conditions.

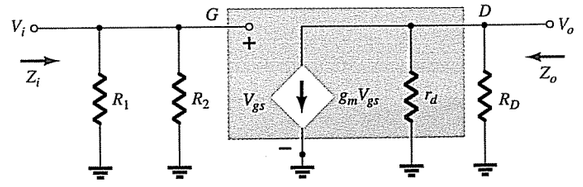


FIG. 8.24
Redrawn network of Fig. 8.23.

A_v

$$V_{gs} = V_i$$

and
$$V_o = -g_m V_{gs}(r_d \| R_D)$$

so that
$$A_v = \frac{V_o}{V_i} = \frac{-g_m V_{gs}(r_d \| R_D)}{V_{gs}}$$

and
$$\boxed{A_v = \frac{V_o}{V_i} = -g_m(r_d \| R_D)} \tag{8.31}$$

If $r_d \geq 10R_D$,
$$\boxed{A_v = \frac{V_o}{V_i} \cong -g_m R_D}_{r_d \geq 10R_D} \tag{8.32}$$

Note that the equations for Z_o and A_v are the same as obtained for the fixed-bias and self-bias (with bypassed R_S) configurations. The only difference is the equation for Z_i, which is now sensitive to the parallel combination of R_1 and R_2.

8.6 JFET SOURCE-FOLLOWER (COMMON-DRAIN) CONFIGURATION

The JFET equivalent of the BJT emitter-follower configuration is the source-follower configuration of Fig. 8.25. Note that the output is taken off the source terminal and, when the dc supply is replaced by its short-circuit equivalent, the drain is grounded (hence, the terminology common-drain).

Substituting the JFET equivalent circuit results in the configuration of Fig. 8.26. The controlled source and the internal output impedance of the JFET are tied to ground

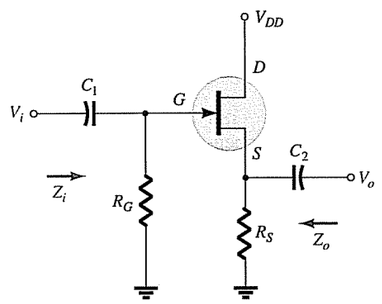


FIG. 8.25
JFET source-follower configuration.

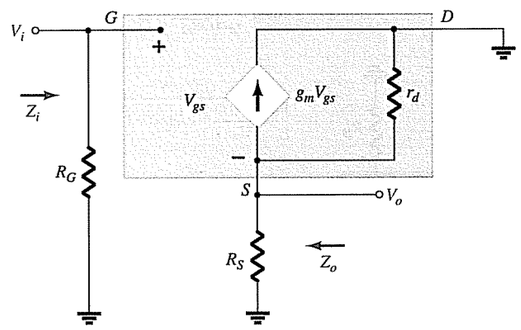


FIG. 8.26
Network of Fig. 8.25 following the substitution of the JFET ac equivalent model.

at one end and R_S on the other, with V_o across R_S. Since $g_m V_{gs}$, r_d, and R_S are connected to the same terminal and ground, they can all be placed in parallel as shown in Fig. 8.27. The current source reversed direction, but V_{gs} is still defined between the gate and source terminals.

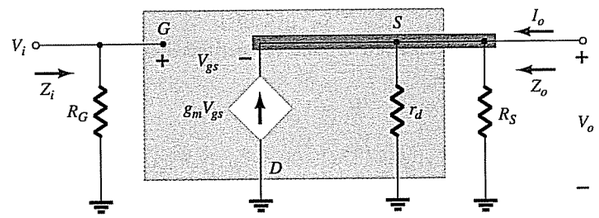


FIG. 8.27
Network of Fig. 8.26 redrawn.

Z_i Figure 8.27 clearly reveals that Z_i is defined by

$$\boxed{Z_i = R_G} \tag{8.33}$$

Z_o Setting $V_i = 0$ V results in the gate terminal being connected directly to the ground as shown in Fig. 8.28.

FIG. 8.28
Determining Z_o for the network of Fig. 8.25.

The fact that V_{gs} and V_o are across the same parallel network results in $V_o = -V_{gs}$.

Applying Kirchhoff's current law at node S, we obtain

$$I_o + g_m V_{gs} = I_{r_d} + I_{R_s}$$
$$= \frac{V_o}{r_d} + \frac{V_o}{R_S}$$

The result is
$$I_o = V_o\left[\frac{1}{r_d} + \frac{1}{R_S}\right] - g_m V_{gs}$$
$$= V_o\left[\frac{1}{r_d} + \frac{1}{R_S}\right] - g_m[-V_o]$$
$$= V_o\left[\frac{1}{r_d} + \frac{1}{R_S} + g_m\right]$$

and
$$Z_o = \frac{V_o}{I_o} = \frac{V_o}{V_o\left[\frac{1}{r_d} + \frac{1}{R_S} + g_m\right]} = \frac{1}{\frac{1}{r_d} + \frac{1}{R_S} + g_m} = \frac{1}{\frac{1}{r_d} + \frac{1}{R_S} + \frac{1}{1/g_m}}$$

which has the same format as the total resistance of three parallel resistors. Therefore,

$$\boxed{Z_o = r_d \| R_S \| 1/g_m} \tag{8.34}$$

For $r_d \geq 10\,R_S$,

$$\boxed{Z_o \cong R_S \| 1/g_m}_{\,r_d \geq 10R_S} \tag{8.35}$$

A_v The output voltage V_o is determined by

$$V_o = g_m V_{gs}(r_d \| R_S)$$

and applying Kirchhoff's voltage law around the perimeter of the network of Fig. 8.27 results in

$$V_i = V_{gs} + V_o$$

and

$$V_{gs} = V_i - V_o$$

so that

$$V_o = g_m(V_i - V_o)(r_d \| R_S)$$

or

$$V_o = g_m V_i(r_d \| R_S) - g_m V_o(r_d \| R_S)$$

and

$$V_o[1 + g_m(r_d \| R_S)] = g_m V_i(r_d \| R_S)$$

so that

$$\boxed{A_v = \frac{V_o}{V_i} = \frac{g_m(r_d \| R_S)}{1 + g_m(r_d \| R_S)}} \tag{8.36}$$

In the absence of r_d or if $r_d \geq 10\,R_S$,

$$\boxed{A_v = \frac{V_o}{V_i} \cong \frac{g_m R_S}{1 + g_m R_S}}_{\,r_d \geq 10R_S} \tag{8.37}$$

Since the denominator of Eq. (8.36) is larger than the numerator by a factor of one, the gain can never be equal to or greater than one (as encountered for the emitter-follower BJT network).

Phase Relationship Since A_v of Eq. (8.36) is a positive quantity, V_o and V_i are in phase for the JFET source-follower configuration.

PSpice

EXAMPLE 8.9 A dc analysis of the source-follower network of Fig. 8.29 results in $V_{GS_Q} = -2.86$ V and $I_{D_Q} = 4.56$ mA.

a. Determine g_m.
b. Find r_d.
c. Determine Z_i.
d. Calculate Z_o with and without r_d. Compare results.
e. Determine A_v with and without r_d. Compare results.

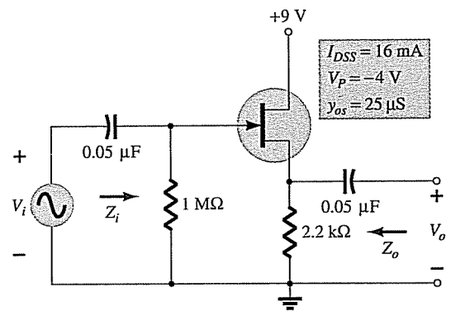


FIG. 8.29
Network to be analyzed in Example 8.9.

Solution:

a. $g_{m0} = \dfrac{2I_{DSS}}{|V_P|} = \dfrac{2(16\text{ mA})}{4\text{ V}} = 8\text{ mS}$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 8\text{ mS}\left(1 - \frac{(-2.86\text{ V})}{(-4\text{ V})}\right) = \mathbf{2.28\ mS}$$

b. $r_d = \dfrac{1}{y_{os}} = \dfrac{1}{25\,\mu\text{S}} = \mathbf{40\ k\Omega}$

c. $Z_i = R_G = \mathbf{1\ M\Omega}$

d. With r_d,

$$Z_o = r_d \| R_S \| 1/g_m = 40\text{ k}\Omega \| 2.2\text{ k}\Omega \| 1/2.28\text{ mS}$$
$$= 40\text{ k}\Omega \| 2.2\text{ k}\Omega \| 438.6\ \Omega$$
$$= \mathbf{362.52\ \Omega}$$

which shows that Z_o is often relatively small and determined primarily by $1/g_m$.
Without r_d,

$$Z_o = R_S \| 1/g_m = 2.2\text{ k}\Omega \| 438.6\ \Omega = \mathbf{365.69\ \Omega}$$

which shows that r_d typically has little effect on Z_o.

e. With r_d,

$$A_v = \frac{g_m(r_d \| R_S)}{1 + g_m(r_d \| R_S)} = \frac{(2.28\text{ mS})(40\text{ k}\Omega \| 2.2\text{ k}\Omega)}{1 + (2.28\text{ mS})(40\text{ k}\Omega \| 2.2\text{ k}\Omega)}$$
$$= \frac{(2.28\text{ mS})(2.09\text{ k}\Omega)}{1 + (2.28\text{ mS})(2.09\text{ k}\Omega)} = \frac{4.77}{1 + 4.77} = \mathbf{0.83}$$

which is less than 1, as predicted above.
Without r_d,

$$A_v = \frac{g_m R_S}{1 + g_m R_S} = \frac{(2.28\text{ mS})(2.2\text{ k}\Omega)}{1 + (2.28\text{ mS})(2.2\text{ k}\Omega)}$$
$$= \frac{5.02}{1 + 5.02} = \mathbf{0.83}$$

which shows that r_d usually has little effect on the gain of the configuration.

8.7 JFET COMMON-GATE CONFIGURATION

The last JFET configuration to be analyzed in detail is the common-gate configuration of Fig. 8.30, which parallels the common-base configuration employed with BJT transistors.

Substituting the JFET equivalent circuit results in Fig. 8.31. Note the continuing requirement that the controlled source $g_m V_{gs}$ be connected from drain to source with r_d in parallel. The isolation between input and output circuits has obviously been lost since the gate terminal is now connected to the common ground of the network. In addition, the resistor connected between input terminals is no longer R_G, but the resistor R_S connected from

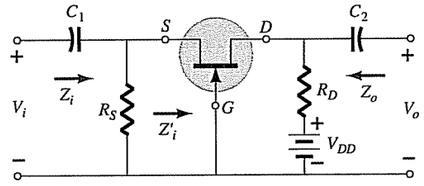


FIG. 8.30
JFET common-gate configuration.

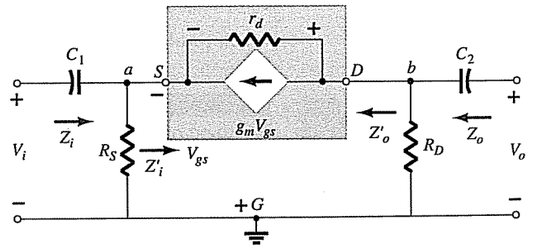


FIG. 8.31
Network of Fig. 8.30 following substitution of JFET ac equivalent model.

source to ground. Note also the location of the controlling voltage V_{gs} and the fact that it appears directly across the resistor R_S.

Z_i The resistor R_S is directly across the terminals defining Z_i. Let us therefore find the impedance Z_i' of Fig. 8.30, which will simply be in parallel with R_S when Z_i is defined.

The network of interest is redrawn as Fig. 8.32. The voltage $V' = -V_{gs}$. Applying Kirchhoff's voltage law around the output perimeter of the network results in

$$V' - V_{r_d} - V_{R_D} = 0$$

and

$$V_{r_d} = V' - V_{R_D} = V' - I'R_D$$

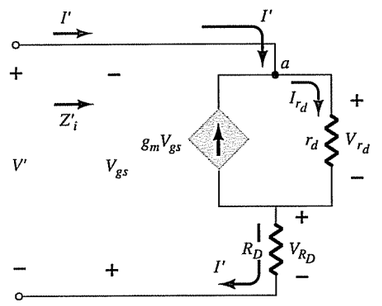


FIG. 8.32
Determining Z_i' for the network of Fig. 8.30.

Applying Kirchhoff's current law at node a results in

$$I' + g_mV_{gs} = I_{r_d}$$

and

$$I' = I_{r_d} - g_mV_{gs} = \frac{(V' - I'R_D)}{r_d} - g_mV_{gs}$$

or

$$I' = \frac{V'}{r_d} - \frac{I'R_D}{r_d} - g_m[-V']$$

so that

$$I'\left[1 + \frac{R_D}{r_d}\right] = V'\left[\frac{1}{r_d} + g_m\right]$$

and

$$\boxed{Z_i' = \frac{V'}{I'} = \frac{\left[1 + \frac{R_D}{r_d}\right]}{\left[g_m + \frac{1}{r_d}\right]}} \quad \textbf{(8.38)}$$

or

$$Z_i' = \frac{V'}{I'} = \frac{r_d + R_D}{1 + g_mr_d}$$

and

$$Z_i = R_S\|Z_i'$$

which results in

$$\boxed{Z_i = R_S\left\|\left[\frac{r_d + R_D}{1 + g_mr_d}\right]\right.} \quad \textbf{(8.39)}$$

If $r_d \geq 10R_D$, Eq. (8.38) permits the following approximation since $R_D/r_d \ll 1$ and $1/r_d \ll g_m$:

$$Z_i' = \frac{\left[1 + \frac{R_D}{r_d}\right]}{\left[g_m + \frac{1}{r_d}\right]} \cong \frac{1}{g_m}$$

and

$$\boxed{Z_i \cong R_S\|1/g_m}_{r_d \geq 10R_D} \quad \textbf{(8.40)}$$

Z_o Substituting $V_i = 0$ V in Fig. 8.31 will "short-out" the effects of R_S and set V_{gs} to 0 V. The result is $g_mV_{gs} = 0$, and r_d will be in parallel with R_D. Therefore,

$$\boxed{Z_o = R_D\|r_d} \quad \textbf{(8.41)}$$

For $r_d \geq 10R_D$,

$$\boxed{Z_o \cong R_D}_{r_d \geq 10R_D} \quad \textbf{(8.42)}$$

A_v Figure 8.31 reveals that

$$V_i = -V_{gs}$$

and

$$V_o = I_DR_D$$

The voltage across r_d is

$$V_{r_d} = V_o - V_i$$

and

$$I_{r_d} = \frac{V_o - V_i}{r_d}$$

Applying Kirchhoff's current law at node b in Fig. 8.31 results in

$$I_{r_d} + I_D + g_mV_{gs} = 0$$

and

$$I_D = -I_{r_d} - g_mV_{gs}$$

$$= -\left[\frac{V_o - V_i}{r_d}\right] - g_m[-V_i]$$

$$I_D = \frac{V_i - V_o}{r_d} + g_mV_i$$

so that

$$V_o = I_DR_D = \left[\frac{V_i - V_o}{r_d} + g_mV_i\right]R_D$$

$$= \frac{V_iR_D}{r_d} - \frac{V_oR_D}{r_d} + g_m$$

and

$$V_o\left[1 + \frac{R_D}{r_d}\right] = V_i\left[\frac{R_D}{r_d} + g_mR_D\right]$$

with

$$\boxed{A_v = \frac{V_o}{V_i} = \frac{\left[g_mR_D + \frac{R_D}{r_d}\right]}{\left[1 + \frac{R_D}{r_d}\right]}} \quad \textbf{(8.43)}$$

For $r_d \geq 10R_D$, the factor R_D/r_d of Eq. (8.43) can be dropped as a good approximation, and

$$\boxed{A_v \cong g_mR_D}_{r_d \geq 10R_D} \quad \textbf{(8.44)}$$

Phase Relationship The fact that A_v is a positive number will result in an *in-phase* relationship between V_o and V_i for the common-gate configuration.

EXAMPLE 8.10 Although the network of Fig. 8.33 may not initially appear to be of the common-gate variety, a close examination will reveal that it has all the characteristics of Fig. 8.30. If $V_{GS_Q} = -2.2$ V and $I_{D_Q} = 2.03$ mA:



a. Determine g_m.
b. Find r_d.
c. Calculate Z_i with and without r_d. Compare results.
d. Find Z_o with and without r_d. Compare results.
e. Determine V_o with and without r_d. Compare results.

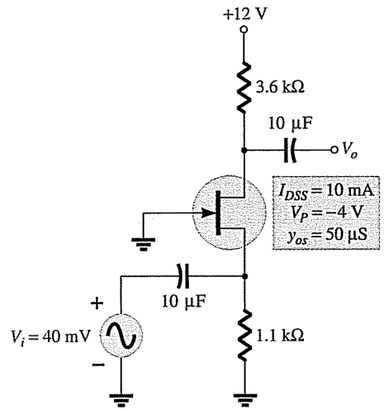


FIG. 8.33
Network for Example 8.10.

Solution:

a. $$g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(10\text{ mA})}{4\text{ V}} = 5\text{ mS}$$

$$g_m = g_{m0}\left(1 - \frac{V_{GSQ}}{V_P}\right) = 5\text{ mS}\left(1 - \frac{(-2.2\text{ V})}{(-4\text{ V})}\right) = \mathbf{2.25\text{ mS}}$$

b. $$r_d = \frac{1}{y_{os}} = \frac{1}{50\,\mu\text{S}} = \mathbf{20\text{ k}\Omega}$$

c. With r_d,

$$Z_i = R_S\|\left[\frac{r_d + R_D}{1 + g_m r_d}\right] = 1.1\text{ k}\Omega\|\left[\frac{20\text{ k}\Omega + 3.6\text{ k}\Omega}{1 + (2.25\text{ ms})(20\text{ k}\Omega)}\right]$$
$$= 1.1\text{ k}\Omega\|0.51\text{ k}\Omega = \mathbf{0.35\text{ k}\Omega}$$

Without r_d,

$$Z_i = R_S\|1/g_m = 1.1\text{ k}\Omega\|1/2.25\text{ ms} = 1.1\text{ k}\Omega\|0.44\text{ k}\Omega$$
$$= \mathbf{0.31\text{ k}\Omega}$$

Even though the condition $r_d \geq 10R_D$ is not satisfied with $r_d = 20\text{ k}\Omega$ and $10R_D = 36\text{ k}\Omega$, both equations result in essentially the same level of impedance. In this case, $1/g_m$ was the predominant factor.

d. With r_d,

$$Z_o = R_D\|r_d = 3.6\text{ k}\Omega\|20\text{ k}\Omega = \mathbf{3.05\text{ k}\Omega}$$

Without r_d,

$$Z_o = R_D = \mathbf{3.6\text{ k}\Omega}$$

Again the condition $r_d \geq 10R_D$ is *not* satisfied, but both results are reasonably close. R_D is certainly the predominant factor in this example.

e. With r_d,

$$A_v = \frac{\left[g_m R_D + \frac{R_D}{r_d}\right]}{\left[1 + \frac{R_D}{r_d}\right]} = \frac{\left[(2.25\text{ mS})(3.6\text{ k}\Omega) + \frac{3.6\text{ k}\Omega}{20\text{ k}\Omega}\right]}{\left[1 + \frac{3.6\text{ k}\Omega}{20\text{ k}\Omega}\right]}$$
$$= \frac{8.1 + 0.18}{1 + 0.18} = \mathbf{7.02}$$

and $$A_v = \frac{V_o}{V_i} \Rightarrow V_o = A_v V_i = (7.02)(40\text{ mV}) = \mathbf{280.8\text{ mV}}$$

Without r_d,

$$A_v = g_m R_D = (2.25\text{ mS})(3.6\text{ k}\Omega) = \mathbf{8.1}$$

with $$V_o = A_v V_i = (8.1)(40\text{ mV}) = \mathbf{324\text{ mV}}$$

In this case, the difference is a little more noticeable, but not dramatically so.

Example 8.10 demonstrates that even though the condition $r_d \geq 10R_D$ was not satisfied, the results for the parameters given were not significantly different using the exact and approximate equations. In fact, in most cases, the approximate equations can be used to find a reasonable idea of particular levels with a reduced amount of effort.

8.8 DEPLETION-TYPE MOSFETs

The fact that Shockley's equation is also applicable to depletion-type MOSFETs (D-MOSFETs) results in the same equation for g_m. In fact, the ac equivalent model for D-MOSFETs is exactly the same as that employed for JFETs, as shown in Fig. 8.34.

The only difference offered by D-MOSFETs is that V_{GS_Q} can be positive for *n*-channel devices and negative for *p*-channel units. The result is that g_m can be greater than g_{m0}, as demonstrated by the example to follow. The range of r_d is very similar to that encountered for JFETs.

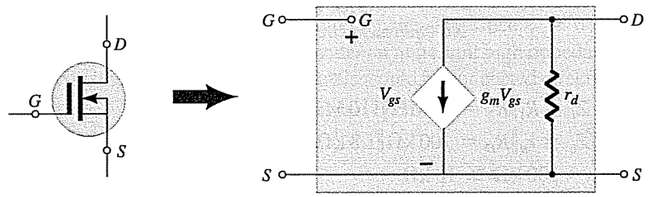


FIG. 8.34
D-MOSFET ac equivalent model.

EXAMPLE 8.11 The network of Fig. 8.35 was analyzed as Example 7.8, resulting in $V_{GS_Q} = 0.35$ V and $I_{D_Q} = 7.6$ mA.

a. Determine g_m and compare to g_{m0}.
b. Find r_d.
c. Sketch the ac equivalent network for Fig. 8.35.
d. Find Z_i.
e. Calculate Z_o.
f. Find A_v.

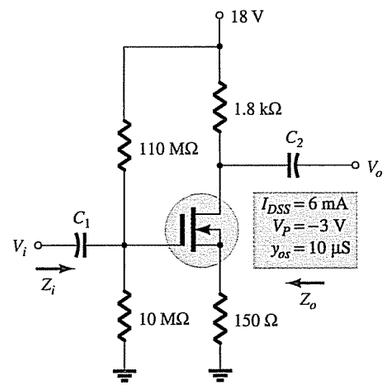


FIG. 8.35
Network for Example 8.11.

Solution:

a. $g_{m0} = \dfrac{2I_{DSS}}{|V_P|} = \dfrac{2(6\text{ mA})}{3\text{ V}} = 4\text{ mS}$

$$g_m = g_{m0}\left(1 - \frac{V_{GSQ}}{V_P}\right) = 4\text{ mS}\left(1 - \frac{(+0.35\text{ V})}{(-3\text{ V})}\right) = 4\text{ mS}(1 + 0.117) = \mathbf{4.47\text{ mS}}$$

b. $r_d = \dfrac{1}{y_{os}} = \dfrac{1}{10\,\mu\text{S}} = \mathbf{100\text{ k}\Omega}$

c. See Fig. 8.36. Note the similarities with the network of Fig. 8.24. Equations (8.28) through (8.32) are therefore applicable.

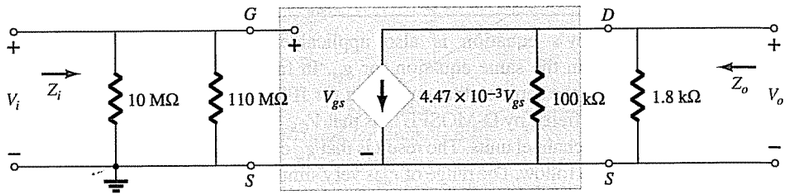


FIG. 8.36
AC equivalent circuit for Fig. 8.35.

d. Eq. (8.28): $Z_i = R_1 \| R_2 = 10\text{ M}\Omega \| 110\text{ M}\Omega = \mathbf{9.17\text{ M}\Omega}$

e. Eq. (8.29): $Z_o = r_d \| R_D = 100\text{ k}\Omega \| 1.8\text{ k}\Omega = \mathbf{1.77\text{ k}\Omega} \cong R_D = \mathbf{1.8\text{ k}\Omega}$

f. $r_d \geq 10R_D \rightarrow 100\text{ k}\Omega \geq 18\text{ k}\Omega$

Eq. (8.32): $A_v = -g_m R_D = -(4.47\text{ mS})(1.8\text{ k}\Omega) = \mathbf{8.05}$

8.9 ENHANCEMENT-TYPE MOSFETs

The enhancement-type MOSFET (E-MOSFET) can be either an *n*-channel (*n*MOS) or *p*-channel (*p*MOS) device, as shown in Fig. 8.37. The ac small-signal equivalent circuit of either device is shown in Fig. 8.37, revealing an open-circuit between gate and drain–source channel and a current source from drain to source having a magnitude dependent on the gate-to-source voltage. There is an output impedance from drain to source r_d, which is usually provided on specification sheets as an admittance y_{os}. The device transconductance g_m is provided on specification sheets as the forward transfer admittance y_{fs}.

In our analysis of JFETs, an equation for g_m was derived from Shockley's equation. For E-MOSFETs, the relationship between output current and controlling voltage is defined by

$$I_D = k(V_{GS} - V_{GS(\text{Th})})^2$$

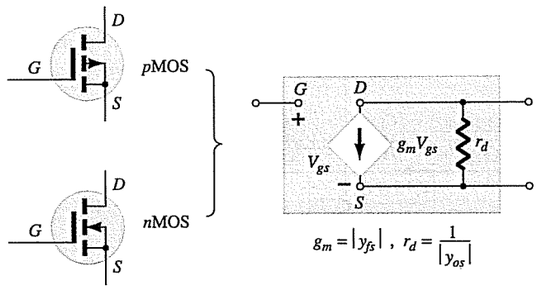


FIG. 8.37
Enhancement MOSFET ac small-signal model.

Since g_m is still defined by

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

we can take the derivative of the transfer equation to determine g_m as an operating point. That is,

$$g_m = \frac{dI_D}{dV_{GS}} = \frac{d}{dV_{GS}} k(V_{GS} - V_{GS(\text{Th})})^2 = k\frac{d}{dV_{GS}}(V_{GS} - V_{GS(\text{Th})})^2$$

$$= 2k(V_{GS} - V_{GS(\text{Th})})\frac{d}{dV_{GS}}(V_{GS} - V_{GS(\text{Th})}) = 2k(V_{GS} - V_{GS(\text{Th})})(1 - 0)$$

and

$$\boxed{g_m = 2k(V_{GSQ} - V_{GS(\text{Th})})} \qquad \textbf{(8.45)}$$

Recall that the constant k can be determined from a given typical operating point on a specification sheet. In every other respect, the ac analysis is the same as that employed for JFETs or D-MOSFETs. Be aware, however, that the characteristics of an E-MOSFET are such that the biasing arrangements are somewhat limited.

8.10 E-MOSFET DRAIN-FEEDBACK CONFIGURATION

The E-MOSFET drain-feedback configuration appears in Fig. 8.38. Recall from dc calculations that R_G could be replaced by a short-circuit equivalent since $I_G = 0$ A and therefore $V_{R_G} = 0$ V. However, for ac situations it provides an important high impedance between V_o and V_i. Otherwise, the input and output terminals would be connected directly and $V_o = V_i$.

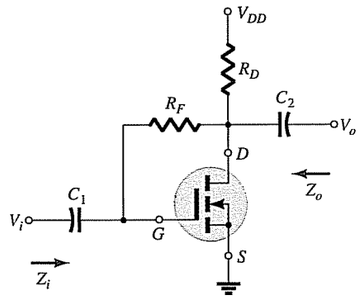


FIG. 8.38
E-MOSFET drain-feedback configuration.

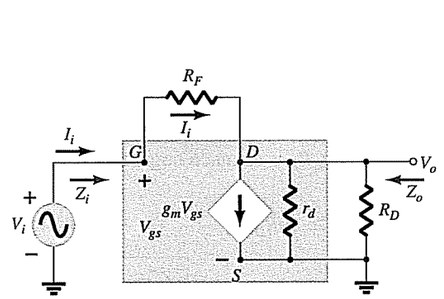


FIG. 8.39
AC equivalent of the network of Fig. 8.38.

Substituting the ac equivalent model for the device results in the network of Fig. 8.39. Note that R_F is not within the shaded area defining the equivalent model of the device, but does provide a direct connection between input and output circuits.

Z_i Applying Kirchhoff's current law to the output circuit (at node *D* in Fig. 8.39) results in

$$I_i = g_m V_{gs} + \frac{V_o}{r_d \| R_D}$$

and

$$V_{gs} = V_i$$

so that

$$I_i = g_m V_i + \frac{V_o}{r_d \| R_D}$$

or

$$I_i - g_m V_i = \frac{V_o}{r_d \| R_D}$$

Therefore,

$$V_o = (r_d \| R_D)(I_i - g_m V_i)$$

with

$$I_i = \frac{V_i - V_o}{R_F} = \frac{V_i - (r_d \| R_D)(I_i - g_m V_i)}{R_F}$$

and $$I_iR_F = V_i - (r_d\|R_D)I_i + (r_d\|R_D)g_mV_i$$

so that $$V_i[1 + g_m(r_d\|R_D)] = I_i[R_F + r_d\|R_D]$$

and finally, $$\boxed{Z_i = \frac{V_i}{I_i} = \frac{R_F + r_d\|R_D}{1 + g_m(r_d\|R_D)}} \quad \textbf{(8.46)}$$

Typically, $R_F \gg r_d\|R_D$, so that

$$Z_i \cong \frac{R_F}{1 + g_m(r_d\|R_D)}$$

For $r_d \geq 10R_D$,

$$\boxed{Z_i \cong \frac{R_F}{1 + g_mR_D}}_{R_F \gg r_d\|R_D,\, r_d \geq 10R_D} \quad \textbf{(8.47)}$$

Z_o Substituting $V_i = 0$ V results in $V_{gs} = 0$ V and $g_mV_{gs} = 0$, with a short-circuit path from gate to ground as shown in Fig. 8.40. R_F, r_d, and R_D are then in parallel and

$$\boxed{Z_o = R_F\|r_d\|R_D} \quad \textbf{(8.48)}$$

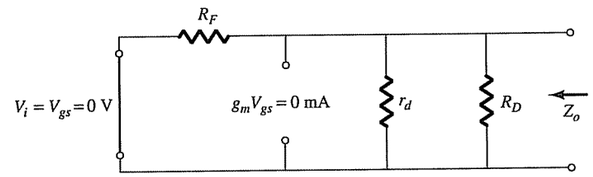


FIG. 8.40
Determining Z_o for the network of Fig. 8.38.

Normally, R_F is so much larger than $r_d\|R_D$ that

$$Z_o \cong r_d\|R_D$$

and with $r_d \geq 10R_D$,

$$\boxed{Z_o \cong R_D}_{R_F \gg r_d\|R_D,\, r_d \geq 10R_D} \quad \textbf{(8.49)}$$

A_v Applying Kirchhoff's current law at node D of Fig. 8.39 results in

$$I_i = g_mV_{gs} + \frac{V_o}{r_d\|R_D}$$

but $$V_{gs} = V_i \quad \text{and} \quad I_i = \frac{V_i - V_o}{R_F}$$

so that $$\frac{V_i - V_o}{R_F} = g_mV_i + \frac{V_o}{r_d\|R_D}$$

and $$\frac{V_i}{R_F} - \frac{V_o}{R_F} = g_mV_i + \frac{V_o}{r_d\|R_D}$$

so that $$V_o\left[\frac{1}{r_d\|R_D} + \frac{1}{R_F}\right] = V_i\left[\frac{1}{R_F} - g_m\right]$$

and $$A_v = \frac{V_o}{V_i} = \frac{\left[\frac{1}{R_F} - g_m\right]}{\left[\frac{1}{r_d\|R_D} + \frac{1}{R_F}\right]}$$

but $$\frac{1}{r_d\|R_D} + \frac{1}{R_F} = \frac{1}{R_F\|r_d\|R_D}$$

and $$g_m \gg \frac{1}{R_F}$$

so that $$\boxed{A_v = -g_m(R_F\|r_d\|R_D)} \quad \textbf{(8.50)}$$

Since R_F is usually $\gg r_d\|R_D$ and if $r_d \geq 10R_D$,

$$\boxed{A_v \cong -g_mR_D}_{R_F \gg r_d\|R_D,\, r_d \geq 10R_D} \quad \textbf{(8.51)}$$

Phase Relationship The negative sign for A_v reveals that V_o and V_i are out of phase by 180°.



EXAMPLE 8.12 The E-MOSFET of Fig. 8.41 was analyzed in Example 7.11, with the result that $k = 0.24 \times 10^{-3}$ A/V^2, $V_{GS_Q} = 6.4$ V, and $I_{D_Q} = 2.75$ mA.

a. Determine g_m.
b. Find r_d.
c. Calculate Z_i with and without r_d. Compare results.
d. Find Z_o with and without r_d. Compare results.
e. Find A_v with and without r_d. Compare results.

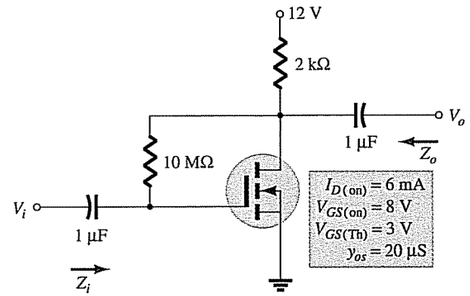


FIG. 8.41
Drain-feedback amplifier from Example 8.11.

Solution:

a. $g_m = 2k(V_{GS_Q} - V_{GS(Th)}) = 2(0.24 \times 10^{-3}\text{ A/V}^2)(6.4\text{ V} - 3\text{ V})$
$= \mathbf{1.63\text{ mS}}$

b. $r_d = \frac{1}{y_{os}} = \frac{1}{20\,\mu\text{S}} = \mathbf{50\text{ k}\Omega}$

c. With r_d,

$$Z_i = \frac{R_F + r_d\|R_D}{1 + g_m(r_d\|R_D)} = \frac{10\text{ M}\Omega + 50\text{ k}\Omega\|2\text{ k}\Omega}{1 + (1.63\text{ mS})(50\text{ k}\Omega\|2\text{ k}\Omega)}$$
$$= \frac{10\text{ M}\Omega + 1.92\text{ k}\Omega}{1 + 3.13} = \mathbf{2.42\text{ M}\Omega}$$

Without r_d,

$$Z_i \cong \frac{R_F}{1 + g_mR_D} = \frac{10\text{ M}\Omega}{1 + (1.63\text{ mS})(2\text{ k}\Omega)} = \mathbf{2.53\text{ M}\Omega}$$

which shows that since the condition $r_d \geq 10R_D = 50\text{ k}\Omega \geq 40\text{ k}\Omega$ is satisfied, the results for Z_o with or without r_d will be quite close.

d. With r_d,

$$Z_o = R_F\|r_d\|R_D = 10\text{ M}\Omega\|50\text{ k}\Omega\|2\text{ k}\Omega = 49.75\text{ k}\Omega\|2\text{ k}\Omega$$
$$= \mathbf{1.92\text{ k}\Omega}$$

Without r_d,

$$Z_o \cong R_D = 2\,\text{k}\Omega$$

again providing very close results.

e. With r_d,

$$\begin{aligned} A_v &= -g_m(R_F \| r_d \| R_D) \\ &= -(1.63\,\text{mS})(10\,\text{M}\Omega \| 50\,\text{k}\Omega \| 2\,\text{k}\Omega) \\ &= -(1.63\,\text{mS})(1.92\,\text{k}\Omega) \\ &= \mathbf{-3.21} \end{aligned}$$

Without r_d,

$$\begin{aligned} A_v &= -g_m R_D = -(1.63\,\text{mS})(2\,\text{k}\Omega) \\ &= \mathbf{-3.26} \end{aligned}$$

which is very close to the above result.

8.11 E-MOSFET VOLTAGE-DIVIDER CONFIGURATION

The last E-MOSFET configuration to be examined in detail is the voltage-divider network of Fig. 8.42. The format is exactly the same as appearing in a number of earlier discussions.

Substituting the ac equivalent network for the E-MOSFET results in the configuration of Fig. 8.43, which is exactly the same as Fig. 8.24. The result is that Eqs. (8.28) through (8.32) are applicable, as listed below for the E-MOSFET.

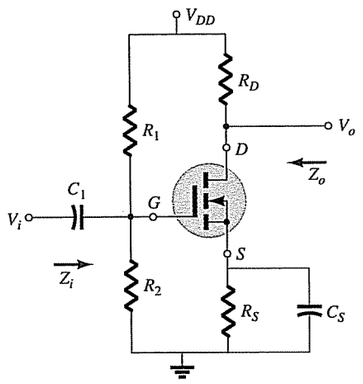


FIG. 8.42
E-MOSFET voltage-divider configuration.

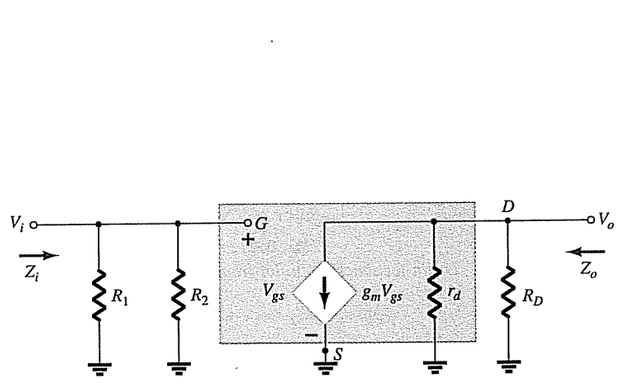


FIG. 8.43
AC equivalent network for the configuration of Fig. 8.42.

Z_i

$$Z_i = R_1 \| R_2 \tag{8.52}$$

Z_o

$$Z_o = r_d \| R_D \tag{8.53}$$

For $r_d \geq 10R_D$,

$$Z_o \cong R_d \quad _{r_d \geq 10R_D} \tag{8.54}$$

A_v

$$A_v = \frac{V_o}{V_i} = -g_m(r_d \| R_D) \tag{8.55}$$

and if $r_d \geq 10R_D$,

$$A_v = \frac{V_o}{V_i} \cong -g_m R_D \tag{8.56}$$

8.12 DESIGNING FET AMPLIFIER NETWORKS

Design problems at this stage are limited to obtaining a desired dc bias condition or ac voltage gain. In most cases, the various equations developed are used "in reverse" to define the parameters necessary to obtain the desired gain, input impedance, or output impedance. To avoid unnecessary complexity during the initial stages of the design, the approximate equations are often employed because some variation will occur when calculated resistors are replaced by standard values. Once the initial design is completed, the results can be tested and refinements made using the complete equations.

Throughout the design procedure be aware that although superposition permits a separate analysis and design of the network from a dc and an ac viewpoint, a parameter chosen in the dc environment will often play an important role in the ac response. In particular, recall that the resistance R_G could be replaced by a short-circuit equivalent in the feedback configuration because $I_G \cong 0$ A for dc conditions, but for the ac analysis, it presents an important high-impedance path between V_o and V_i. In addition, recall that g_m is larger for operating points closer to the I_D axis ($V_{GS} = 0$ V), requiring that R_S be relatively small. In the unbypassed R_S network, a small R_S will also contribute to a higher gain, but for the source-follower, the gain is reduced from its maximum value of 1. In total, simply keep in mind that network parameters can affect the dc and ac levels in different ways. Often a balance must be made between a particular operating point and its effect on the ac response.

In most situations, the available dc supply voltage is known, the FET to be employed has been determined, and the capacitors to be employed at the chosen frequency are defined. It is then necessary to determine the resistive elements necessary to establish the desired gain or impedance level. The next three examples determine the required parameters for a specific gain.

EXAMPLE 8.13 Design the fixed-bias network of Fig. 8.44 to have an ac gain of 10. That is, determine the value of R_D.

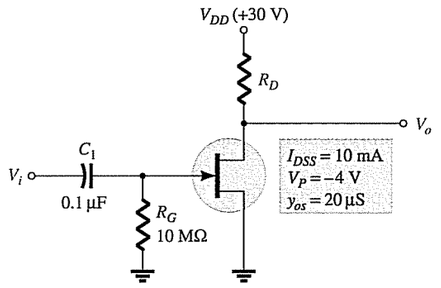


FIG. 8.44
Circuit for desired voltage gain in Example 8.13.

Solution: Since $V_{GS_Q} = 0$ V, the level of g_m is g_{m0}. The gain is therefore determined by

$$A_v = -g_m(R_D \| r_d) = -g_{m0}(R_D \| r_d)$$

with

$$g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(10\,\text{mA})}{4\,\text{V}} = 5\,\text{mS}$$

The result is

$$-10 = -5\,\text{mS}(R_D \| r_d)$$

and

$$R_D \| r_d = \frac{10}{5\,\text{mS}} = 2\,\text{k}\Omega$$

From the device specifications,

$$r_d = \frac{1}{y_{os}} = \frac{1}{20 \times 10^{-6}\,\text{S}} = 50\,\text{k}\Omega$$

Substituting, we find

$$R_D \| r_d = R_D \| 50\,\text{k}\Omega = 2\,\text{k}\Omega$$

and

$$\frac{R_D(50\,\text{k}\Omega)}{R_D + 50\,\text{k}\Omega} = 2\,\text{k}\Omega$$

or

$$50R_D = 2(R_D + 50\,\text{k}\Omega) = 2R_D + 100\,\text{k}\Omega$$

with

$$48R_D = 100\,\text{k}\Omega$$

and

$$R_D = \frac{100\,\text{k}\Omega}{48} \cong 2.08\,\text{k}\Omega$$

The closest standard value is **2 kΩ** (Appendix D), which would be employed for this design.

The resulting level of V_{DS_Q} is then determined as follows:

$$V_{DS_Q} = V_{DD} - I_{D_Q}R_D = 30\,\text{V} - (10\,\text{mA})(2\,\text{k}\Omega) = \mathbf{10\,V}$$

The levels of Z_i and Z_o are set by the levels of R_G and R_D, respectively. That is,

$$Z_i = R_G = \mathbf{10\,M\Omega}$$

$$Z_o = R_D \| r_d = 2\,\text{k}\Omega \| 50\,\text{k}\Omega = \mathbf{1.92\,k\Omega} \cong R_D = 2\,\text{k}\Omega$$

EXAMPLE 8.14 Choose the values of R_D and R_S for the network of Fig. 8.45 that will result in a gain of 8 using a relatively high level of g_m for this device defined at $V_{GS_Q} = \frac{1}{4}V_P$.

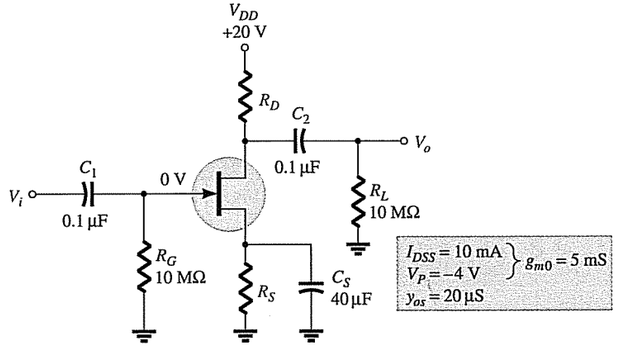


FIG. 8.45
Network for desired voltage gain in Example 8.14.

Solution: The operating point is defined by

$$V_{GS_Q} = \frac{1}{4}V_P = \frac{1}{4}(-4\,\text{V}) = -1\,\text{V}$$

and

$$I_D = I_{DSS}\left(1 - \frac{V_{GS_Q}}{V_P}\right)^2 = 10\,\text{mA}\left(1 - \frac{(-1\,\text{V})}{(-4\,\text{V})}\right)^2 = 5.625\,\text{mA}$$

Determining g_m, we obtain

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right)$$

$$= 5\,\text{mS}\left(1 - \frac{(-1\,\text{V})}{(-4\,\text{V})}\right) = 3.75\,\text{mS}$$

The magnitude of the ac voltage gain is determined by

$$|A_v| = g_m(R_D \| r_d)$$

Substituting known values results in

$$8 = (3.75\,\text{mS})(R_D \| r_d)$$

so that

$$R_D \| r_d = \frac{8}{3.75\,\text{mS}} = 2.13\,\text{k}\Omega$$

The level of r_d is defined by

$$r_d = \frac{1}{y_{os}} = \frac{1}{20\,\mu\text{S}} = 50\,\text{k}\Omega$$

and

$$R_D \| 50\,\text{k}\Omega = 2.13\,\text{k}\Omega$$

with the result that

$$R_D = \mathbf{2.2\,k\Omega}$$

which is a standard value.

The level of R_S is determined by the dc operating conditions as follows:

$$V_{GS_Q} = -I_D R_S$$

$$-1\,\text{V} = -(5.625\,\text{mA})R_S$$

and

$$R_S = \frac{1\,\text{V}}{5.625\,\text{mA}} = 177.8\,\Omega$$

The closest standard value is **180 Ω**. In this example, R_S does not appear in the ac design because of the shorting effect of C_S.

In the next example, R_S is unbypassed and the design becomes a bit more complicated.

EXAMPLE 8.15 Determine R_D and R_S for the network of Fig. 8.45 to establish a gain of 8 if the bypass capacitor C_S is removed.

Solution: V_{GS_Q} and I_{D_Q} are still −1 V and 5.625 mA, respectively, and since the equation $V_{GS} = -I_D R_S$ has not changed, R_S continues to equal the standard value of **180 Ω** obtained in Example 8.14.

The gain of an unbypassed self-bias configuration is

$$A_v = -\frac{g_m R_D}{1 + g_m R_S}$$

For the moment it is assumed that $r_d \geq 10(R_D + R_S)$. Using the full equation for A_v at this stage of the design would simply complicate the process unnecessarily.

Substituting (for the specified magnitude of 8 for the gain), we obtain

$$|8| = \left|\frac{-(3.75\,\text{mS})R_D}{1 + (3.75\,\text{mS})(180\,\Omega)}\right| = \frac{(3.75\,\text{mS})R_D}{1 + 0.675}$$

and

$$8(1 + 0.675) = (3.75\,\text{mS})R_D$$

so that

$$R_D = \frac{13.4}{3.75\,\text{mS}} = 3.573\,\text{k}\Omega$$

with the closest standard value at **3.6 kΩ**.

We can now test the condition

$$r_d \geq 10(R_D + R_S)$$

We have

$$50\,\text{k}\Omega \geq 10(3.6\,\text{k}\Omega + 0.18\,\text{k}\Omega) = 10(3.78\,\text{k}\Omega)$$

and

$$50\,\text{k}\Omega \geq 37.8\,\text{k}\Omega$$

which is satisfied—the solution stands!

8.13 SUMMARY TABLE

To provide a quick comparison between configurations and offer a listing that can be helpful for a variety of reasons, Table 8.1 was developed. The exact and approximate equation for each important parameter are provided with a typical range of values for each. Although

TABLE 8.1

Z_i, Z_o, and A_v for various FET configurations

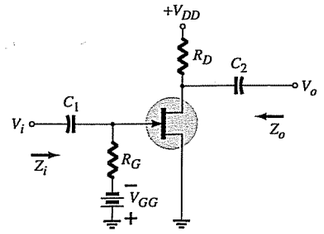
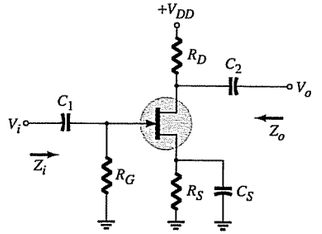
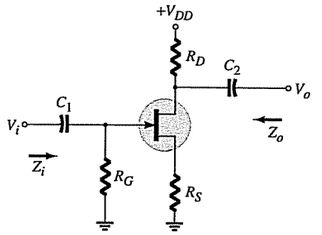
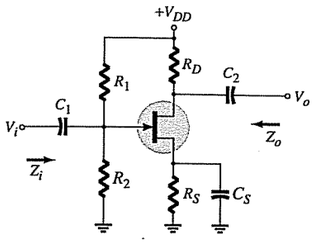
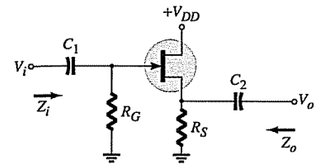
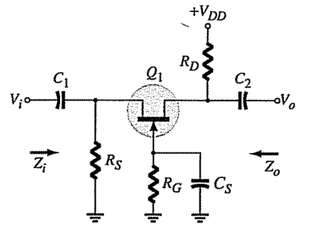
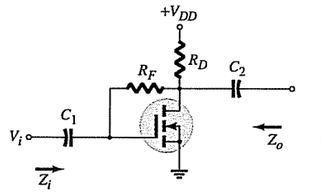
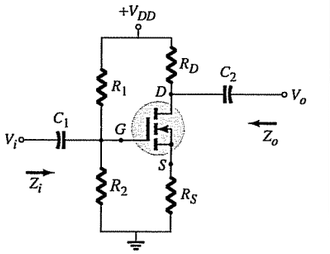
Configuration	Z_i	Z_o	$A_v = \frac{V_o}{V_i}$
Fixed-bias [JFET or D-MOSFET] 	High (10 MΩ) $= R_G$	Medium (2 kΩ) $= R_D \| r_d$ $\cong R_D$ $(r_d \geq 10R_D)$	Medium (−10) $= -g_m(r_d \| R_D)$ $\cong -g_m R_D$ $(r_d \geq 10R_D)$
Self-bias bypassed R_S [JFET or D-MOSFET] 	High (10 MΩ) $= R_G$	Medium (2 kΩ) $= R_D \| r_d$ $\cong R_D$ $(r_d \geq 10R_D)$	Medium (−10) $= -g_m(r_d \| R_D)$ $\cong -g_m R_D$ $(r_d \geq 10R_D)$
Self-bias unbypassed R_S [JFET or D-MOSFET] 	High (10 MΩ) $= R_G$	$= \dfrac{\left[1 + g_m R_S + \frac{R_S}{r_d}\right] R_D}{\left[1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d}\right]}$ $= R_D$ $r_d \geq 10R_D$ or $r_d = \infty\,\Omega$	Low (−2) $= \dfrac{g_m R_D}{1 + g_m R_S + \frac{R_D + R_S}{r_d}}$ $\cong -\dfrac{g_m R_D}{1 + g_m R_S}$ $[r_d \geq 10(R_D + R_S)]$
Voltage-divider bias [JFET or D-MOSFET] 	High (10 MΩ) $= R_1 \| R_2$	Medium (2 kΩ) $= R_D \| r_d$ $\cong R_D$ $(r_d \geq 10R_D)$	Medium (−10) $= -g_m(r_d \| R_D)$ $\cong -g_m R_D$ $(r_d \geq 10R_D)$

TABLE 8.1

(Continued)

Configuration	Z_i	Z_o	$A_v = \frac{V_o}{V_i}$
Source-follower [JFET or D-MOSFET] 	High (10 MΩ) $= R_G$	Low (100 kΩ) $= r_d \| R_S \| 1/g_m$ $\cong R_S \| 1 \| g_m$ $(r_d \geq 10R_S)$	Low (<1) $= \dfrac{g_m(r_d \| R_S)}{1 + g_m(r_d \| R_S)}$ $\cong \dfrac{g_m R_S}{1 + g_m R_S}$ $(r_d \geq 10R_S)$
Common-gate [JFET or D-MOSFET] 	Low (1 kΩ) $= R_S \left\| \left[\dfrac{r_d + R_D}{1 + g_m r_d} \right] \right.$ $\cong R_S \left\| \dfrac{1}{g_m} \right.$ $(r_d \geq 10R_D)$	Medium (2 kΩ) $= R_D \| r_d$ $\cong R_D$ $(r_d \geq 10R_D)$	Medium (+10) $= \dfrac{g_m R_D + \frac{R_D}{r_d}}{1 + \frac{R_D}{r_d}}$ $\cong g_m R_D$ $(r_d \geq 10R_D)$
Drain-feedback bias E-MOSFET 	Medium (1 MΩ) $= \dfrac{R_F + r_d \| R_D}{1 + g_m(r_d \| R_D)}$ $\cong \dfrac{R_F}{1 + g_m R_D}$ $(r_d \geq 10R_D)$	Medium (2 kΩ) $= R_F \| r_d \| R_D$ $\cong R_D$ $(R_F, r_d \geq 10R_D)$	Medium (−10) $= -g_m(R_F \| r_d \| R_D)$ $\cong -g_m R_D$ $(R_F, r_d \geq 10R_D)$
Voltage-divider bias E-MOSFET 	Medium (1 MΩ) $= R_1 \| R_2$	Medium (2 kΩ) $= R_D \| r_d$ $\cong R_D$ $(R_d \geq 10R_D)$	Medium (−10) $= -g_m(r_d \| R_D)$ $\cong -g_m R_D$ $(r_d \geq 10R_D)$

all the possible configurations are not present, the majority of the most frequently encountered are included. In fact, any configuration not listed will probably be some variation of those appearing in the table, so at the very least, the listing will provide some insight as to what expected levels should be and which path will probably generate the desired equations. The format chosen was designed to permit a duplication of the entire table on the front and back of one $8\frac{1}{2}$ by 11 inch page.

8.14 EFFECT OF R_L AND R_{sig}

This section will parallel Sections 5.16 and 5.17 of the BJT small-signal ac analysis chapter dealing with the effect of the source resistance and load resistance on the ac gain of an amplifier. There are again two approaches to the analysis. One can simply substitute the ac model for the FET of interest and perform a detailed analysis similar to the unloaded situation, or apply the two-port equations introduced in Section 5.17.

All of the two-port equations developed for the BJT transistor apply to FET networks also because the quantities of interest are defined at the input and output terminals and not the components of the system.

A few of the most important equations are repeated below to provide an easy reference for the analysis of this chapter and to refresh your memory about the conclusions:

$$A_v = \frac{R_L}{R_L + R_o} A_{v_{NL}} \tag{8.57}$$

$$A_i = -A_v \frac{Z_i}{R_L} \tag{8.58}$$

$$A_{v_s} = \frac{V_o}{V_S} = \frac{V_i}{V_S} \cdot \frac{V_o}{V_i} = \left(\frac{R_i}{R_i + R_{sig}}\right)\left(\frac{R_L}{R_L + R_o}\right) A_{v_{NL}} \tag{8.59}$$

Some of the important conclusions about the gain of BJT transistor configurations are also applicable to FET networks. They include the following facts:

The greatest gain of an amplifier is the no-load gain.

The loaded gain is always less than the no-load gain.

A source impedance will always reduce the overall gain below the no-load or loaded level.

In general, therefore,

$$A_{v_{NL}} > A_v > A_{v_s} \tag{8.60}$$

Recall from Chapter 5 that some BJT configurations are such that the output impedance is sensitive to the source impedance or the input impedance is sensitive to the applied load. For FET networks, however:

Due to the high impedance between the gate terminal and the channel, one can generally assume that the input impedance is unaffected by the load resistor and the output impedance is unaffected by the source resistance.

One must always be aware, however, that there are special situations where the above may not be totally true. Take, for instance, the feedback configuration that results in a direct connection between input and output networks. Although the feedback resistor is usually many times that of the source resistance, permitting the approximation that the source resistance is essentially 0 Ω, it does present a situation where the source resistance could possibly affect the output resistance or the load resistance could affect the input impedance. In general, however, due to the high isolation provided between the gate and the drain or source terminals, the general equations for the loaded gain are less complex than those encountered for BJT transistors. Recall that the base current provided a direct link between input and output circuits of any BJT transistor configuration.

To demonstrate each approach, let us examine the self-bias configuration of Fig. 8.46 with a bypassed source resistance. Substituting the ac equivalent model for the JFET results in the configuration of Fig. 8.47.

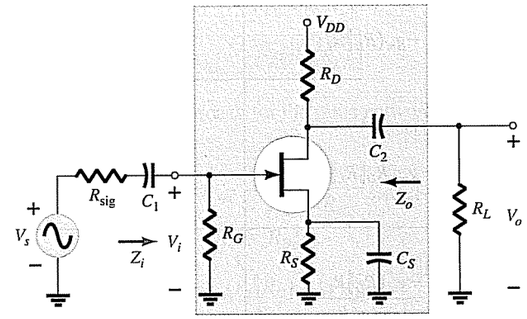


FIG. 8.46
JFET amplifier with R_{sig} and R_L.

Note that the load resistance appears in parallel with the drain resistance and the source resistance R_{sig} appears in series with the gate resistance R. For the overall voltage gain the result is a modified form of Eq. (8.21):

$$A_v = \frac{V_o}{V_i} = -g_m(r_d \| R_D \| R_L) \tag{8.61}$$

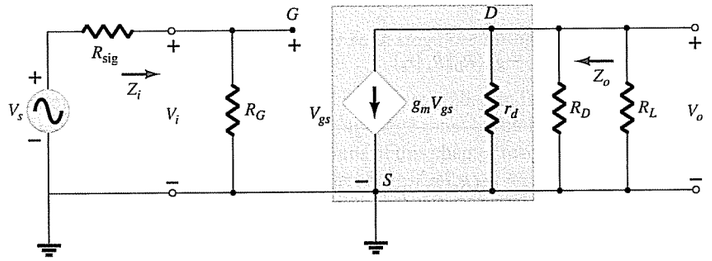


FIG. 8.47
Network of Fig. 8.46 following the substitution of the ac equivalent circuit for the JFET.

The output impedance is the same as obtained for the unloaded situation without a source resistance:

$$Z_o = r_d \| R_D \tag{8.62}$$

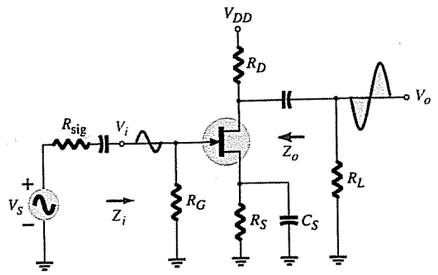
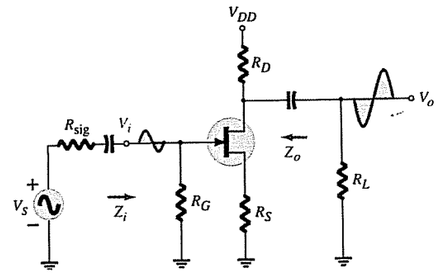
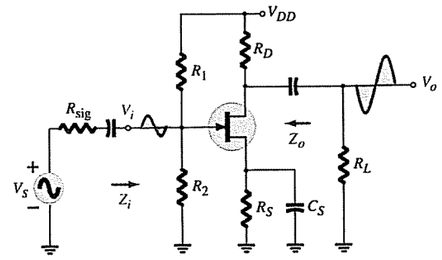
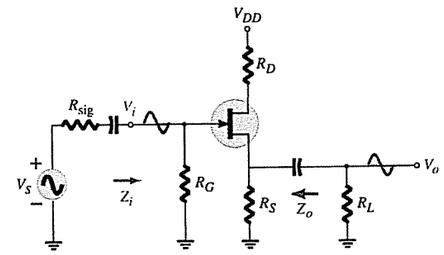
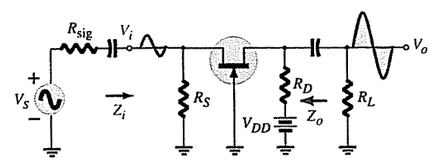
The input impedance remains as

$$Z_i = R_G \tag{8.63}$$

For the overall gain A_{v_S},

$$V_i = \frac{R_G V_S}{R_G + R_{sig}}$$

TABLE 8.2

Configuration	$A_v = V_o/V_i$	Z_i	Z_o
	$-g_m(R_D\|\|R_L)$ Including r_d: $-g_m(R_D\|\|R_L\|\|r_d)$	R_G R_G	R_D $R_D\|\|r_d$
	$\dfrac{-g_m(R_D\|\|R_L)}{1+g_mR_S}$ Including r_d: $\dfrac{-g_m(R_D\|\|R_L)}{1+g_mR_S+\dfrac{R_D+R_S}{r_d}}$	R_G R_G	$\dfrac{R_D}{1+g_mR_S}$ $\cong \dfrac{R_D}{1+g_mR_S}$
	$-g_m(R_D\|\|R_L)$ Including r_d: $-g_m(R_D\|\|R_L\|\|r_d)$	$R_1\|\|R_2$ $R_1\|\|R_2$	R_D $R_D\|\|r_d$;
	$\dfrac{g_m(R_S\|\|R_L)}{1+g_m(R_S\|\|R_L)}$ Including r_d: $=\dfrac{g_mr_d(R_S\|\|R_L)}{r_d+R_D+g_mr_d(R_S\|\|R_L)}$	R_G R_G	$R_S\|\|1/g_m$ $\dfrac{R_S}{1+\dfrac{g_mr_dR_S}{r_d+R_D}}$
	$g_m(R_D\|\|R_L)$ Including r_d: $\cong g_m(R_D\|\|R_L)$	$\dfrac{R_S}{1+g_mR_S}$ $Z_i=\dfrac{R_S}{1+\dfrac{g_mr_dR_S}{r_d+R_D\|\|R_L}}$	R_D $R_D\|\|r_d$

and

$$\boxed{A_{v_s}=\frac{V_o}{V_s}=\frac{V_i}{V_s}\cdot\frac{V_o}{V_i}=\left[\frac{R_G}{R_G+R_{\text{sig}}}\right][-g_m(r_d\|R_D\|R_L)]} \tag{8.64}$$

which for most applications where $R_G \gg R_{\text{sig}}$ and $R_D\|R_L \ll r_d$ results in

$$\boxed{A_{v_s}\cong -g_m(R_D\|R_L)} \tag{8.65}$$

If we now turn to the two-port approach for the same network, the equation for the overall gain becomes

$$A_v=\frac{R_L}{R_L+R_o}A_{v_{\text{NL}}}=\frac{R_L}{R_L+R_o}[-g_m(r_d\|R_D)]$$

but

$$R_o=R_D\|r_d,$$

so that

$$A_v=\frac{R_L}{R_L+R_D\|r_d}[-g_m(r_d\|R_D]=-g_m\frac{(r_d\|R_D)(R_L)}{(r_d+R_D)+R_L}$$

and

$$A_v=-g_m(r_d\|R_D\|R_L)$$

matching the previous result.

The above derivation was included to demonstrate that the same result will be obtained using either approach. If numerical values for R_i, R_o, and $A_{v_{\text{NL}}}$ were available, it would simply be a matter of substituting the values into the Eq. (8.57).

Continuing in the same manner for the most common configurations results in the equations of Table 8.2.

8.15 CASCADE CONFIGURATION

The cascade configuration introduced in Chapter 5 for BJTs can also be used with JFETs or MOSFETs, as shown for JFETs in Fig. 8.48. Recall that the output of one stage appears as the input for the following stage. The input impedance for the second stage is the load impedance for the first stage.

The total gain is the product of the gain of each stage including the loading effects of the following stage.

Too often, the no-load gain is employed and the overall gain is an unrealistic result. For each stage the loading effect of the following stage must be included in the gain calculations. Using the results of the previous sections of this chapter results in the following equation for the overall gain of the configuration of Fig. 8.48:

$$A_v=A_{v_1}A_{v_2}=(-g_{m_1}R_{D_1})(-g_{m_2}R_{D_2})=g_{m_1}g_{m_2}R_{D_1}R_{D_2} \tag{8.66}$$

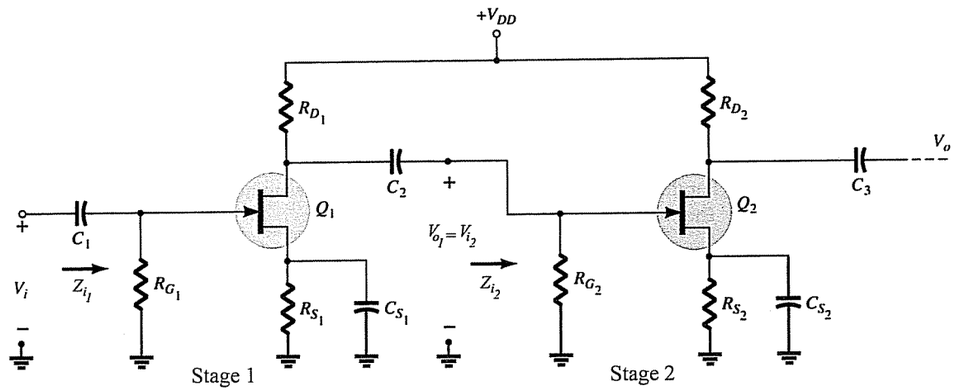


FIG. 8.48
Cascaded FET amplifier.

The input impedance of the cascade amplifier is that of stage 1,

$$Z_i = R_{G_1} \tag{8.67}$$

and the output impedance is that of stage 2,

$$Z_o = R_{D_2} \tag{8.57}$$

The main function of cascading stages is the larger overall gain achieved. Since dc bias and ac calculations for a cascade amplifier follow those derived for the individual stages, an example will demonstrate the various calculations to determine dc bias and ac operation.

PSpice

EXAMPLE 8.16 Calculate the dc bias, voltage gain, input impedance, output impedance, and resulting output voltage for the cascade amplifier shown in Fig. 8.49. Calculate the load voltage if a 10-kΩ load is connected across the output.

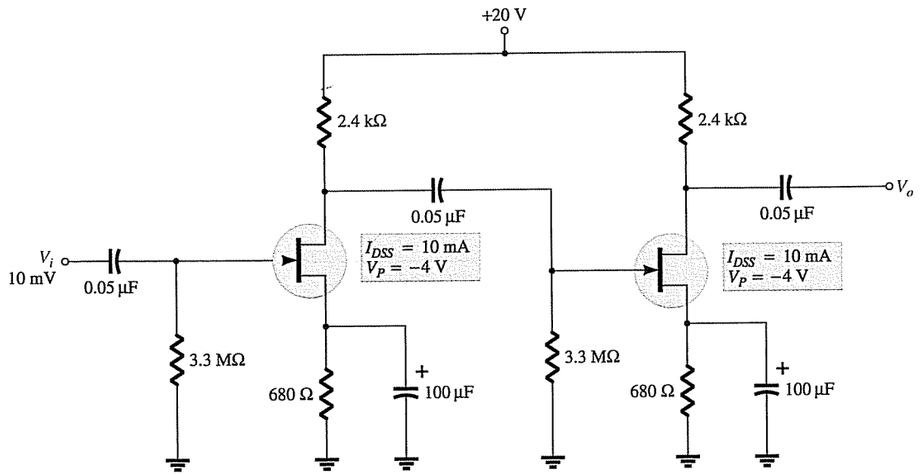


FIG. 8.49
Cascade amplifier circuit for Example 8.16.

Solution: Both amplifier stages have the same dc bias. Using dc bias techniques from Chapter 7 results in

$$V_{GS_Q} = -1.9\text{ V}, \qquad I_{D_Q} = 2.8\text{ mA} \qquad g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(10\text{ mA})}{|-4\text{ V}|} = 5\text{ mS}$$

and at the dc bias point,

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = (5\text{ mS})\left(1 - \frac{-1.9\text{ V}}{-4\text{ V}}\right) = \mathbf{2.6\text{ mS}}$$

Since the second stage is unloaded

$$A_{v_2} = -g_m R_D = -(2.6\text{ mS})(2.4\text{ k}\Omega) = \mathbf{-6.24}$$

For the first stage $2.4\text{ k}\Omega \| 3.3\text{ M}\Omega \cong 2.4\text{ k}\Omega$ resulting in the same gain.
The cascade amplifier voltage gain is

$$\text{Eq. (8.66):} \quad A_v = A_{v_1}A_{v_2} = (-6.2)(-6.2) = 38.4$$

The output voltage is then

$$V_o = A_v V_i = (38.4)(10\text{ mV}) = \mathbf{384\text{ mV}}$$

The cascade amplifier input impedance is

$$Z_i = R_G = \mathbf{3.3\text{ M}\Omega}$$

The cascade amplifier output impedance (assuming that $r_d = \infty\,\Omega$) is

$$Z_o = R_D = \mathbf{2.4\text{ k}\Omega}$$

The output voltage across a 10-kΩ load is then

$$V_L = \frac{R_L}{Z_o + R_L}V_o = \frac{10\text{ k}\Omega}{2.4\text{ k}\Omega + 10\text{ k}\Omega}(384\text{ mV}) = \mathbf{310\text{ mV}}$$

A combination of FET and BJT stages can also be used to provide high voltage gain and high input impedance, as demonstrated by the next example.

PSpice

EXAMPLE 8.17 For the cascade amplifier of Fig. 8.50, use the dc bias calculated in Examples 5.18 and 8.16 to calculate input impedance, output impedance, voltage gain, and resulting output voltage.

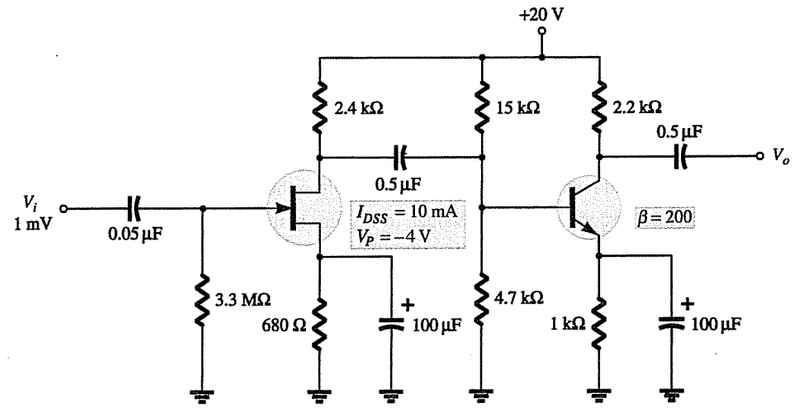


FIG. 8.50
Cascaded JFET-BJT amplifier for Example 8.17.

Solution: Since R_i (stage 2) $= 15\text{ k}\Omega \| 4.7\text{ k}\Omega \| 200(6.5\ \Omega) = 953.6\ \Omega$, the gain of stage 1 (when loaded by stage 2) is

$$\begin{aligned} A_{v_1} &= -g_m[R_D \| R_i\text{ (stage 2)}] \\ &= -2.6\text{ mS}(2.4\text{ k}\Omega \| 953.6\ \Omega) = -1.77 \end{aligned}$$

From Example 5.18, the voltage gain of stage 2 is $A_{v_2} = -338.46$. The overall voltage gain is then

$$A_v = A_{v_1}A_{v_2} = (-1.77)(-338.46) = \mathbf{599.1}$$

The output voltage is then

$$V_o = A_v V_i = (599.1)(1\text{ mV}) \approx \mathbf{0.6\text{ V}}$$

The input impedance of the amplifier is that of stage 1,

$$Z_i = \mathbf{3.3\text{ M}\Omega}$$

and the output impedance is that of stage 2,

$$Z_o = R_D = \mathbf{2.2\text{ k}\Omega}$$

8.16 TROUBLESHOOTING

As mentioned before, troubleshooting a circuit is a combination of knowing the theory and having experience using meters and an oscilloscope to check the operation of the circuit. A good troubleshooter has a "nose" for finding the trouble in a circuit—this ability to "see" what is happening being greatly developed through building, testing, and repairing many

different circuits. For an FET small-signal amplifier, one could go about troubleshooting a circuit by performing a number of basic steps:

1. Look at the circuit board to see if any obvious problems can be seen: an area charred by excess heating of a component; a component that feels or seems too hot to touch; what appears to be a poor solder joint; any connection that appears to have come loose.
2. Use a dc meter: make some measurements as marked in a repair manual containing the circuit schematic diagram and a listing of test dc voltages.
3. Apply a test ac signal: measure the ac voltages starting at the input and work along toward the output.
4. If the problem is identified at a particular stage, the ac signal at various points should be checked using an oscilloscope to see the waveform, its polarity, amplitude, and frequency, as well as any unusual waveform "glitches" that may be present. In particular, observe that the signal is present for the full signal cycle.

Possible Symptoms and Actions

If there is no output ac voltage:

1. Check whether the supply voltage is present.
2. Check whether the output voltage at V_D is between 0 V and V_{DD}.
3. Check whether there is any input ac signal at the gate terminal.
4. Check the ac voltage at each side of the coupling capacitor terminals.

When building and testing an FET amplifier circuit in the laboratory:

1. Check the color code of resistor values to be sure that they are correct. Even better, measure the resistor values because components used repeatedly may get overheated when used incorrectly, causing the nominal value to change.
2. Check that all dc voltages are present at the component terminals. Be sure that all ground connections are made common.
3. Measure the ac input signal to be sure the expected value is provided to the circuit.

8.17 PRACTICAL APPLICATIONS

Three-Channel Audio Mixer

The basic components of a three-channel JFET audio mixer are shown in Fig. 8.51. The three input signals can come from different sources such as a microphone, a musical instrument, background sound generators, and so on. All signals can be applied to the same

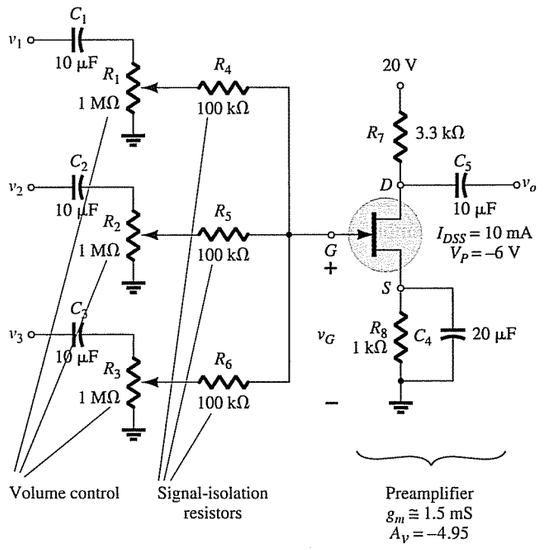


FIG. 8.51
Basic components of a three-channel JFET audio mixer.

gate terminal because the input impedance of the JFET is so high that it can be approximated by an open circuit. **In general, the input impedance is 1000 MΩ ($10^9\Omega$) or better for JFETs and 100 million MΩ ($10^{14}\Omega$) or better for MOSFETs.** If BJTs were employed instead of JFETs, the lower input impedance would require a transistor amplifier for each channel or at least an emitter-follower as the first stage to provide a higher input impedance.

The 10-μF capacitors are there to prevent any dc biasing levels on the input signal from appearing at the gate of the JFET, and the 1-MΩ potentiometers are the volume controls for each channel. The need for the 100-kΩ resistors for each channel is less obvious. Their purpose is to ensure that one channel does not load down the other channels and severely reduce or distort the signal at the gate. For instance, in Fig. 8.52a, one channel has a high-impedance (10-kΩ) microphone, whereas another channel has a low-impedance (0.5-kΩ) guitar amplifier. Channel 3 is left open, and the 100-kΩ isolation resistors have been removed for the moment. Replacing the capacitors by their short-circuit equivalent for the frequency range of interest and ignoring the effects of the parallel 1-MΩ potentiometers (set at their maximum value) result in the equivalent circuit of Fig. 8.52b at the gate of the JFET amplifier. Using the superposition theorem, we determine the voltage at the gate of the JFET by

$$v_G = \frac{0.5\,\text{k}\Omega(v_{\text{mic}})}{10.5\,\text{k}\Omega} + \frac{10\,\text{k}\Omega(v_{\text{guitar}})}{10.5\,\text{k}\Omega}$$
$$= 0.047v_{\text{mic}} + 0.95v_{\text{guitar}} \cong v_{\text{guitar}}$$

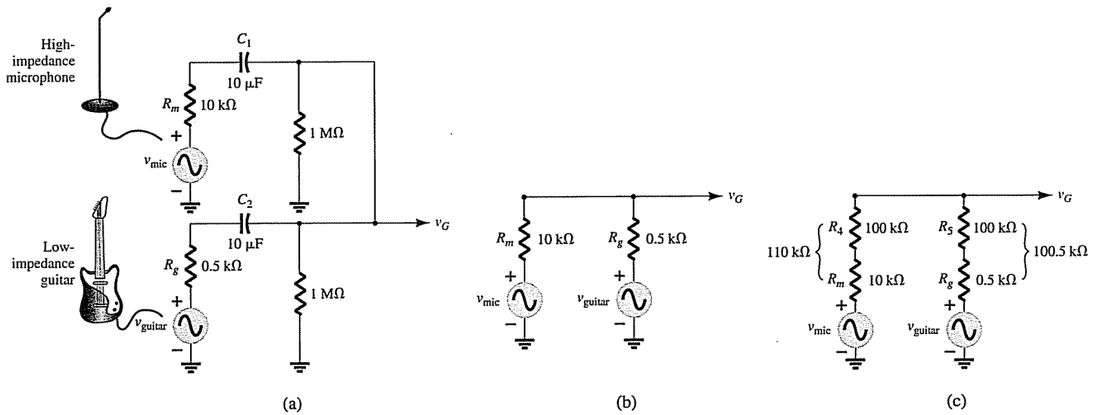


FIG. 8.52
(a) Application of a high- and a low-impedance source to the mixer of Fig. 8.51; (b) reduced equivalent without the 100-kΩ isolation resistors; (c) reduced equivalent with the 100-kΩ resistors.

clearly showing that the guitar has swamped the signal of the microphone. The only response of the amplifier of Fig. 8.52 will be to the guitar. Now, with the 100-kΩ resistors in place, the situation of Fig. 8.52c results. Using the superposition theorem again, we obtain the following equation for the voltage at the gate:

$$v_G = \frac{101\,\text{k}\Omega(v_{\text{mic}})}{211\,\text{k}\Omega} + \frac{110\,\text{k}\Omega(v_{\text{guitar}})}{211\,\text{k}\Omega}$$
$$\cong 0.48v_{\text{mic}} + 0.52v_{\text{guitar}}$$

showing an even balance in the signals at the gate of the JFET. **In general, therefore, the 100-kΩ resistors compensate for any difference in signal impedance to ensure that one does not load down the other and develop a mixed level of signals at the amplifier. Technically, they are often called "signal isolation resistors."**

An interesting consequence of a situation such as described in Fig. 8.52b is depicted in Fig. 8.53, where a guitar of low impedance has a signal level of about 150 mV, whereas the microphone, having a larger internal impedance, has a signal strength of only 50 mV. As pointed out above, the major part of the signal at the "feed" point (v_G) is that of the guitar. The resulting direction of current and power flow is unquestionably from the guitar to the

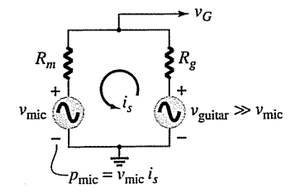
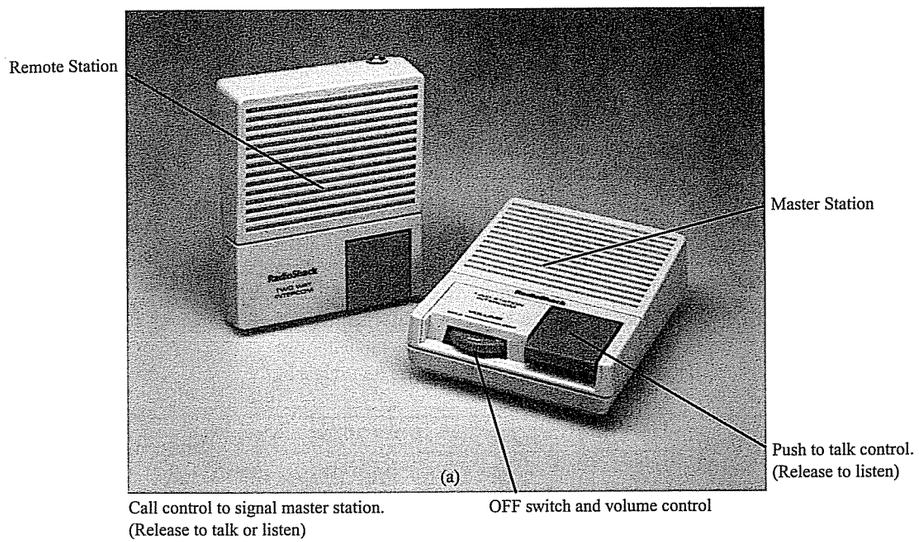


FIG. 8.53
Demonstrating that for parallel signals, the channel with the least internal impedance and most power controls the situation.

microphone. Furthermore, **since the basic construction of a microphone and a speaker is quite similar, the microphone may be forced to act like a speaker and broadcast the guitar signal**. New acoustic bands often face this problem as they learn the rudiments of good amplifier basics. **In general, for parallel signals, the channel with the least internal impedance controls the situation**.

For some it may come as quite a surprise that a microphone can actually behave like a speaker. However, the classical example of the use of one voice cone to act as a microphone and a speaker is in the typical intercom system such as appearing in Fig. 8.54a. The 16-Ω, 0.5-W speaker of Fig. 8.54b can be used as a microphone or a speaker, depending on the position of the activation switch. It is important to note, however, as in the microphone–guitar example above, that most speakers are designed to handle reasonable power levels, but most microphones are designed to simply accept the voice-activated input, and they cannot handle the power levels normally associated with speakers. Just compare the size of each



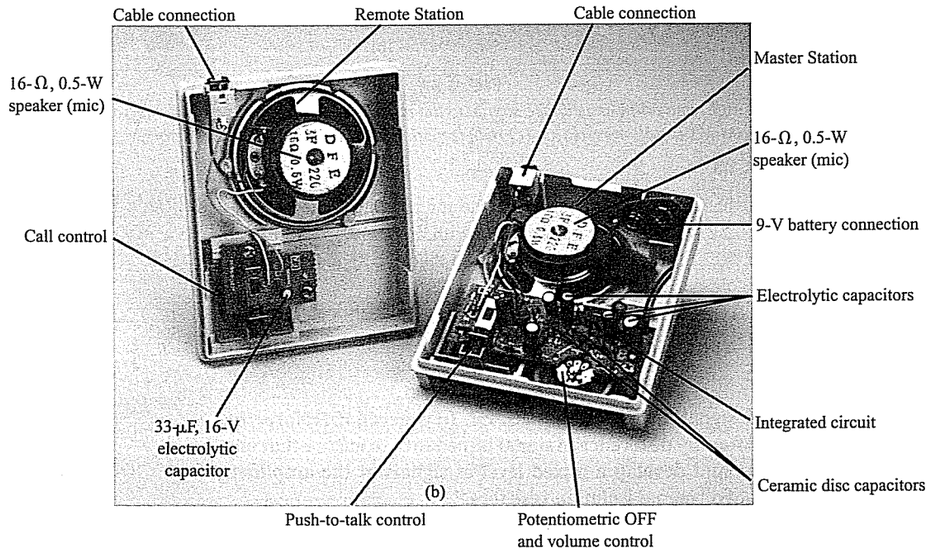


FIG. 8.54

Battery-powered (9-V), two-station intercom: (a) external appearance; (b) internal construction.

in any audio system. In general, a situation such as described above, where the guitar signal is heard over the microphone, will ultimately damage the microphone. For an intercom system the speaker is designed to handle both types of excitation without difficulty.

In Fig. 8.51, the gain of the self-biased JFET is determined by $-g_m R_D$, which for this situation is

$$-g_m R_D = -(1.5\ \text{mS})(3.3\,\text{k}\Omega) = \mathbf{-4.95}$$

Silent Switching

Any electronic system that incorporates mechanical switching such as shown in Fig. 8.55 is prone to developing noise on the line that will reduce the signal-to-noise ratio. When the switch of Fig. 8.55 is opened and closed, one often gets an annoying "pfft, pfft" sound as part of the output signal. In addition, the longer wires normally associated with mechanical switches will require that the switch be as close to the amplifier as possible to reduce the noise pickup on the line.

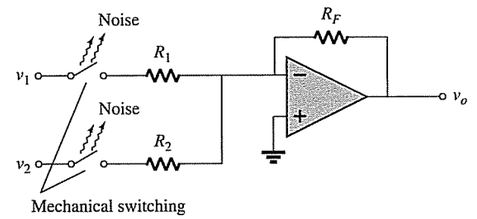
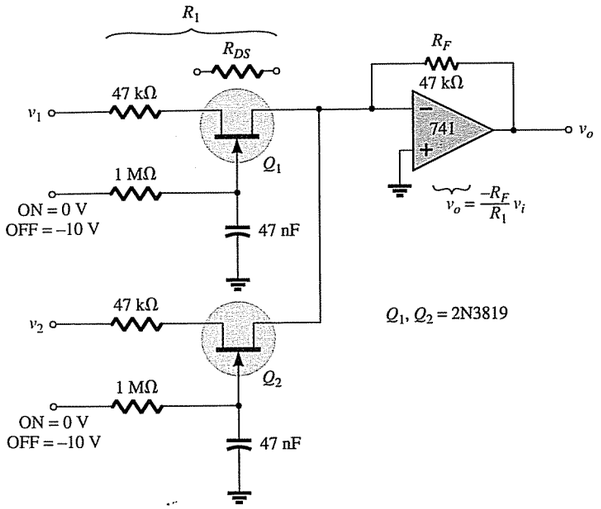


FIG. 8.55

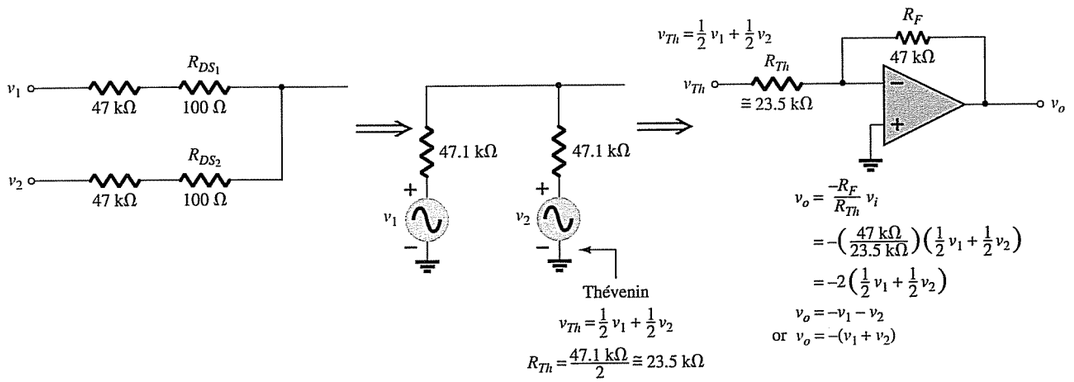
Noise development due to mechanical switching.

One effective method to essentially eliminate this source of noise is to use electronic switching such as shown in Fig. 8.56a for a two-channel mixing network. Recall from Chapter 7 that the drain to source of a JFET for low values of V_{DS} can be looked on as a resistance whose value is determined by the applied gate-to-source voltage as described in detail in Section 7.13. In addition, recall that the resistance is the least at $V_{GS} = 0$ V and the highest near pinch-off. In Fig. 8.56a, the signals to be mixed are applied to the drain side of each JFET, and the dc control is connected directly to the gate terminal of each JFET. With 0 V at each control terminal, both JFETs are heavily "on," and the resistance from D_1 to S_1 and from D_2 to S_2 is relatively small, say, 100 Ω for this discussion. Although 100 Ω is not the 0 Ω assumed with an ideal switch, it is so small compared to the series 47-kΩ resistor that it can often be ignored. Both switches are therefore in the "on" position, and both input signals can make their way to the input of the inverting amplifier (to be introduced in Chapter 10) as shown in Fig. 8.56b. In particular, note that the chosen resistor values result in an output signal that is simply an inversion of the sum of the two signals. The amplifier stage to follow will then raise the summation to audio levels.

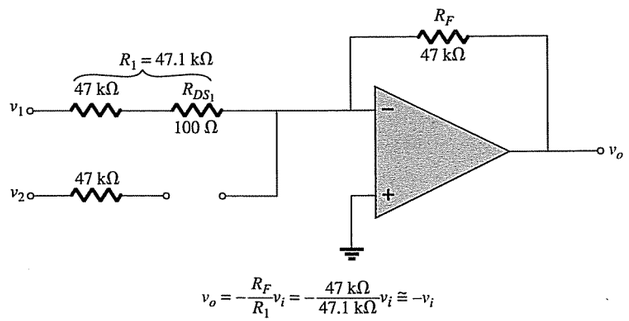
Both electronic switches can be put in the "off" state by applying a voltage that is more negative than the pinch-off level as indicated by the 10 V in Fig. 8.56a. The level of "off" resistance can approach 10,000 MΩ, which certainly can be approximated by an open circuit for most applications. Since both channels are isolated, one can be "on" while the other is "off." The speed of operation of a JFET switch is controlled by the substrate (those due to the device construction) and stray capacitance levels and the low "on" resistance of the JFET. **Maximum speeds for JFETs are about 100 MHz, with 10 MHz being more typical**. However, this speed is critically reduced by the input resistance and capacitance of the design. In Fig. 8.56a, the 1-MΩ resistor and the 47-nF capacitors have a time constant of $\tau = RC = 47\ \text{ms} = 0.047$ s for the dc charging network that is controlling the voltage at the gate. If we assume two time constants to charge to the pinch-off level, the total time is 0.094 s, or a switching speed of 1/0.094 s ≅ 10.6 per second. Compared to the typical switching speed of the JFET at 10 million times in 1 s, this number is extremely small. Keep in mind, however, that the application is the important consideration, and for a typical mixer, switching is not going to occur at speeds greater than 10.6 per second unless we have some radical input signals. One might ask why it is necessary to have the RC time constant



(a)



(b)



(c)

FIG. 8.56

Silent switching audio network: (a) JFET configuration; (b) with both signals present; (c) with one signal on.

at the gate at all. Why not let the applied dc level at the gate simply control the state of the JFET? In general, the *RC* time constant ensures that the control signal is not a spurious one generated by noise or "ringing" due to the sharply rising and falling applied pulses at the gate. By using a charging network, we ensure that the dc level must be present for a period of time before the pinch-off level is reached. Any spike on the line will not be present long enough to charge the capacitor and switch the state of the JFET.

It is important to realize **that the JFET switch is a bilateral switch**. That is, signals in the "on" state can pass through the drain–source region in either direction. This, of course, is the way ordinary mechanical switches work, which makes it that much easier to replace mechanical switch designs with electronic switches. Remember that the diode is not a bilateral switch because it can conduct current at low voltages in only one direction.

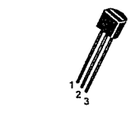
It should be noted that **because the state of the JFETs can be controlled by a dc level, the design of Fig. 8.56a lends itself to remote and computer control** for the same reasons described in Chapter 7 when dc control was discussed.

The data sheet for a low-cost JFET analog switch is provided in Fig. 8.57. Note, in particular, that the pinch-off voltage is typically about −10 V at a drain-to-source voltage of

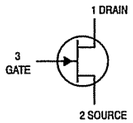
ON Semiconductor™

JFET Switching
N–Channel — Depletion

2N5555



CASE 29–11, STYLE 5
TO–92 (TO–226AA)



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DS}	25	Vdc
Drain–Gate Voltage	V_{DG}	25	Vdc
Gate–Source Voltage	V_{GS}	25	Vdc
Forward Gate Current	I_{GF}	10	mAdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	350 2.8	mW mW/°C
Junction Temperature Range	T_J	–65 to +150	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Gate–Source Breakdown Voltage (I_G = 10 μAdc, V_{DS} = 0)	$V_{(BR)GSS}$	25	—	Vdc
Gate Reverse Current (V_{GS} = 15 Vdc, V_{DS} = 0)	I_{GSS}	—	1.0	nAdc
Drain Cutoff Current (V_{DS} = 12 Vdc, V_{GS} = –10 V) (V_{DS} = 12 Vdc, V_{GS} = –10 V, T_A = 100°C)	$I_{D(off)}$	— —	10 2.0	nAdc μAdc
ON CHARACTERISTICS				
Zero–Gate–Voltage Drain Current[1] (V_{DS} = 15 Vdc, V_{GS} = 0)	I_{DSS}	15	—	mAdc
Gate–Source Forward Voltage ($I_{G(f)}$ = 1.0 mAdc, V_{DS} = 0)	$V_{GS(f)}$	—	1.0	Vdc
Drain–Source On–Voltage (I_D = 7.0 mAdc, V_{GS} = 0)	$V_{DS(on)}$	—	1.5	Vdc
Static Drain–Source On Resistance (I_D = 0.1 mAdc, V_{GS} = 0)	$r_{DS(on)}$	—	150	Ohms

1. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 3.0%.

Characteristic		Symbol	Min	Max	Unit
SMALL–SIGNAL CHARACTERISTICS					
Small–Signal Drain–Source "ON" Resistance (V_{GS} = 0, I_D = 0, f = 1.0 kHz)		$r_{ds(on)}$	—	150	Ohms
Input Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{iss}	—	5.0	pF
Reverse Transfer Capacitance (V_{DS} = 0, V_{GS} = 10 Vdc, f = 1.0 MHz)		C_{rss}	—	1.2	pF
SWITCHING CHARACTERISTICS					
Turn–On Delay Time	(V_{DD} = 10 Vdc, $I_{D(on)}$ = 7.0 mAdc, $V_{GS(on)}$ = 0, $V_{GS(off)}$ = –10 Vdc)	$t_{d(on)}$	—	5.0	ns
Rise Time		t_r	—	5.0	ns
Turn–Off Delay Time	(V_{DD} = 10 Vdc, $I_{D(on)}$ = 7.0 mAdc, $V_{GS(on)}$ = 0, $V_{GS(off)}$ = –10 Vdc)	$t_{d(off)}$	—	15	ns
Fall Time		t_f	—	10	ns

FIG. 8.57

Specification sheet for a low-cost analog JFET current switch.

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12 V. In addition, a current level of 10 nA is used to define the pinch-off level. The level of I_{DSS} is 15 mA, whereas the drain-to-source resistance is quite low at 150 Ω with $V_{GS} = 0$ V. The turn-on time is quite small at 10 ns ($t_d + t_r$), whereas the turn-off time is 25 ns.

Phase-Shift Networks

Using the voltage-controlled drain-to-source resistance characteristic of a JFET, we can control the phase angle of a signal using the configurations of Fig. 8.58. The network of Fig. 8.58a is a phase-advance network, which adds an angle to the applied signal, whereas the network of Fig. 8.58b is a phase-retard configuration, which creates a negative phase shift.

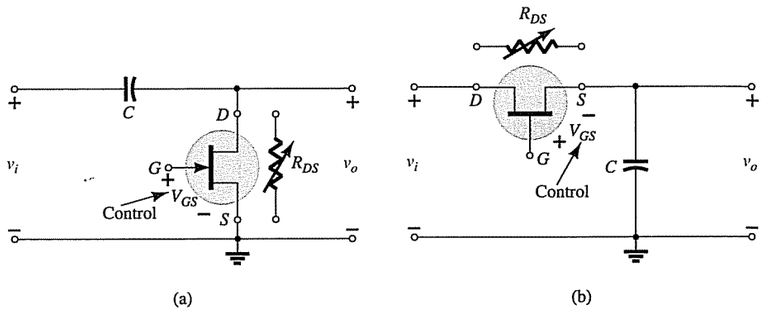


FIG. 8.58
Phase-shift networks: (a) advance; (b) retard.

For example, let us consider the effect of R_{DS} on an input signal having a frequency such as 10 kHz if we apply it to the network of Fig. 8.58a. For discussion, let us assume that the drain-to-source resistance is 2 kΩ due to an applied gate-to-source voltage of −3 V. Drawing the equivalent network results in the general configuration of Fig. 8.59. Solving for the output voltage results in

$$\mathbf{V}_o = \frac{R_{DS}\angle 0^\circ\, V_i\angle 0^\circ}{R_{DS} - jX_C} = \frac{R_{DS}V_i\angle 0^\circ}{\sqrt{R_{DS}^2 + X_C^2}\angle -\tan^{-1}\dfrac{X_C}{R_{DS}}}$$

$$= \frac{R_{DS}V_i}{\sqrt{R_{DS}^2 + X_C^2}}\angle \tan^{-1}\frac{X_C}{R_{DS}} = \left(\frac{R_{DS}}{\sqrt{R_{DS}^2 + X_C^2}}\right)V_i\angle \tan^{-1}\frac{X_C}{R_{DS}}$$

so that

$$\mathbf{V}_o = k_1 V_i \angle \theta_1$$

where

$$\boxed{k_1 = \frac{R_{DS}}{\sqrt{R_{DS}^2 + X_C^2}} \quad \text{and} \quad \theta_1 = \tan^{-1}\frac{X_C}{R_{DS}}} \tag{8.58}$$

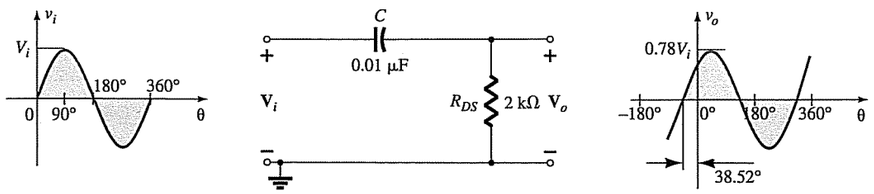


FIG. 8.59
RC phase-advance network.

Substituting the numerical values from above results in

$$X_C = \frac{1}{2\pi fC} = \frac{1}{2\pi(10\,\text{kHz})(0.01\,\mu\text{F})} = 1.592\,\text{k}\Omega$$

and

$$k_1 = \frac{R_{DS}}{\sqrt{R_{DS}^2 + X_C^2}} = \frac{2\,\text{k}\Omega}{\sqrt{(2\,\text{k}\Omega)^2 + (1.592\,\text{k}\Omega)^2}} = 0.782$$

with

$$\theta_1 = \tan^{-1}\frac{X_C}{R_{DS}} = \tan^{-1}\frac{1.592\,\text{k}\Omega}{2\,\text{k}\Omega} = \tan^{-1}0.796 = 38.52^\circ$$

so that

$$\mathbf{V}_o = 0.782V_i\angle 38.52^\circ$$

and an output signal that is 78.2% of its applied signal but with a phase shift of 38.52°.

In general, therefore, the network of Fig. 8.58a can introduce a positive phase shift extending from a few degrees (with X_C relatively small compared to R_{DS}) to almost 90° (with X_C relatively large compared to R_{DS}). Keep in mind, however, that for fixed values of R_{DS}, as the frequency increases, X_C will decrease and the phase shift will approach 0°. For decreasing frequencies and a fixed R_{DS}, the phase shift will approach 90°. It is also important to realize that for a fixed R_{DS}, an increasing level of X_C results in diminishing magnitude for V_o. For such a network, a balance between gain and desired phase shift will have to be made.

For the network of Fig. 8.58b, the resulting equation is

$$\boxed{\mathbf{V}_o = k_2 V_i\angle\theta_2} \tag{8.59}$$

where

$$k_2 = \frac{X_C}{\sqrt{R_{DS}^2 + X_C^2}} \quad \text{and} \quad \theta_2 = -\tan^{-1}\frac{R_{DS}}{X_C}$$

Motion-Detection System

The basic components of a passive infrared (PIR) motion-detection system are shown in Fig. 8.60. The heart of the system is **the pyroelectric detector, which generates a voltage that varies with the amount of incident heat**. It filters out all but the infrared radiation from a particular area and focuses the energy onto a temperature-sensing element. Recall from Chapter 7, Section 7.13, that the infrared band is a nonvisible band just below the visible light spectrum. **Passive detectors do not emit a signal of any kind but simply respond to the energy flow of the environment**.

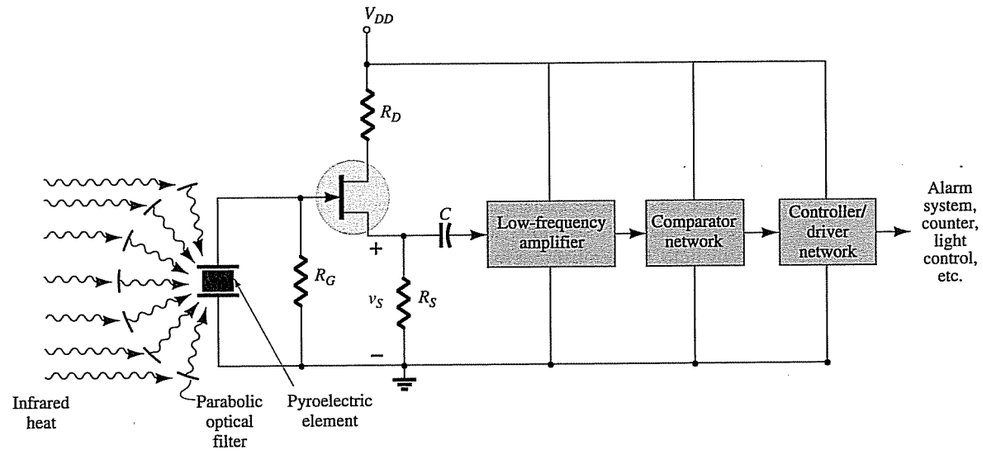
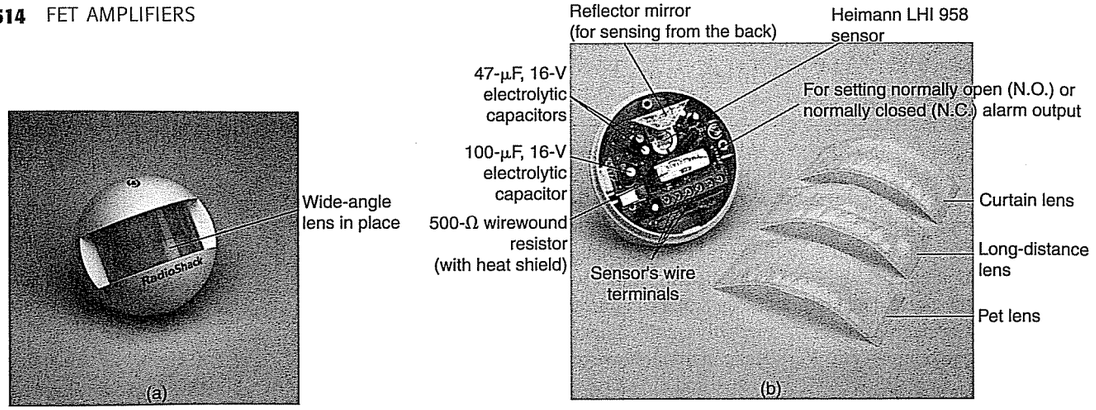


FIG. 8.60
Passive infrared (PIR) motion-detection system.



Lens No.	3
Type	Pet
Mounting Height	4.3 ft (1.3 m)
Zone's Coverage	110°

FIG. 8.61

Commercially available PIR motion-detection unit: (a) external appearance; (b) internal construction; (c) pet option coverage.

An external and an internal view of a commercially available unit are provided in Fig. 8.61a and b, respectively. Four interchangeable lens are provided for different coverage areas. For our purposes the "pet" option was selected with the coverage indicated in Fig. 8.61c. Note the space under the ray for pet motion and the maximum distance of 39.4 ft. The unit is mounted at a height of 6.6 ft and operates at a dc voltage of 9 V to 16 V, drawing a current of 25 mA at 12 V dc. In Fig. 8.61b, the Heimann LH1 958 pyroelectric detector is identified along with the deflector for side detection and the very prominent reed switch in the "can." The controlling ICs are on the other side of the printed circuit board.

To focus the incident ambient heat on the pyroelectric detector, the unit of Fig. 8.61 uses a parabolic deflector. As a person walks past a sensor, he or she will cut the various fields appearing in Fig. 8.61c, and the detector will sense the **rapid changes** in heat level. **The result is a changing dc level akin to a low-frequency ac signal of relatively high internal impedance appearing at the gate of the JFET**. One might then ask why turning a heating system on or turning on a lamp doesn't generate an alarm signal since heat will be generated. The answer is that both will generate a voltage at the detector that grows steadily with increasing heat level from the heating system or the burning bulb. Remember that for the lamp, the detector is heat sensitive and not light sensitive. The resulting voltage is not oscillating between levels, but simply climbing in level and will not set off the alarm—a varying ac voltage will not be generated by the pyroelectric detector!

Note in Fig. 8.60 that a JFET source-follower configuration was employed to ensure a very high input impedance to capture most of the pyroelectric signal. It is then passed through a low-frequency amplifier, followed by a peak-detecting network and a comparator to determine whether the alarm should be set off. The dc voltage comparator is a network that "captures" the peak value of the generated ac voltage and compares it to a known dc voltage level. The output processor determines whether the difference between the two levels is sufficient to tell the driver to energize the alarm.

8.18 SUMMARY

Important Conclusions and Concepts

1. **The transconductance parameter g_m** is determined by the **ratio of the change in drain current** associated with a particular **change in gate-to-source voltage** in the region of interest. The **steeper the slope** of the I_D-versus-V_{GS} curve, the **greater** is the level of g_m. In addition, the **closer the point or region of interest to the saturation current I_{DSS}**, the **greater** is the transconductance parameter.
2. On specification sheets, g_m is provided as y_{fs}.
3. When V_{GS} is **one-half the pinch-off value**, g_m is **one-half the maximum value**.
4. When I_D is **one-fourth the saturation level of I_{DSS}, g_m is one-half the value at saturation**.
5. The **output impedance** of FETs is **similar in magnitude** to that of **conventional BJTs**.
6. On specification sheets the **output impedance r_d is provided as $1/y_{os}$**. The **more horizontal** the characteristic curves on the drain characteristics, the **greater is the output impedance**.
7. The **voltage gain** for the fixed-bias and self-bias JFET configurations (with a bypassed source capacitance) **is the same**.
8. The **ac analysis** of JFETs and depletion-type MOSFETs **is the same**.
9. The **ac equivalent network** for an enhancement-type MOSFET **is the same** as that employed for JFETs and depletion-type MOSFETs. The only difference is the equation for g_m.
10. The **magnitude of the gain** of FET networks is typically **between 2 and 20**. The **self-bias configuration** (without a bypass source capacitance) and the **source-follower** are **low-gain configurations**.
11. There is **no phase shift** between input and output for the **source-follower** and **common-gate configurations**. Most others have a 180° phase shift.
12. The **output impedance** for most FET configurations is **determined primarily by R_D**. For the **source-follower** configuration it is determined by R_S and g_m.
13. The **input impedance** for most FET configurations is **quite high**. However, it is **quite low** for the **common-gate configuration**.
14. When **troubleshooting any electronic or mechanical system**, always check the **most obvious causes first**.

Equations

$$g_m = y_{fs} = \frac{\Delta I_D}{\Delta V_{GS}}$$

$$g_{m0} = \frac{2I_{DSS}}{|V_P|}$$

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right]$$

$$g_m = g_{m0}\sqrt{\frac{I_D}{I_{DSS}}}$$

$$r_d = \frac{1}{y_{os}} = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}=\text{constant}}$$

For JFET and depletion-type MOSFET configurations, see Tables 8.1 and 8.2.

8.19 COMPUTER ANALYSIS

PSpice Windows

JFET Fixed-Bias Configuration The first JFET configuration to be analyzed in the ac domain will be the fixed-bias configuration of Fig. 8.62, using a JFET with $V_P = -4$ V and $I_{DSS} = 10$ mA. The 10-MΩ resistor was added to act as a path to ground for the capacitor

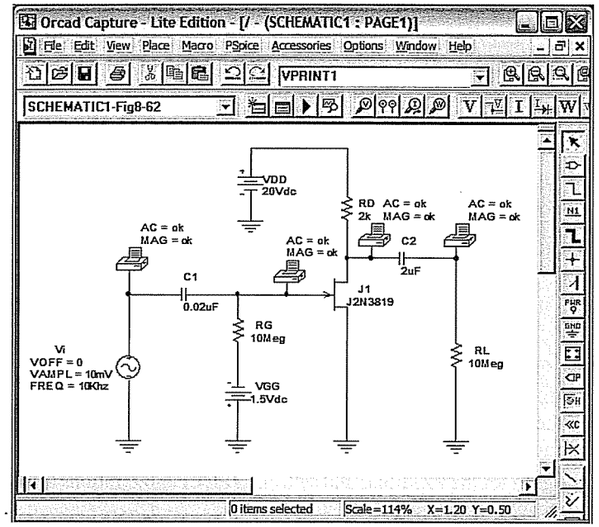


FIG. 8.62
Fixed-bias JFET configuration with an ac source.

but is essentially an open circuit for the ac analysis. The **J2N3819** *n*-channel JFET from the **EVAL** library was used, and the ac voltage is to be determined at four different points for comparison and review.

The constant **Beta** is determined by

$$\text{Beta} = \frac{I_{DSS}}{|V_P|^2} = \frac{10\,\text{mA}}{4^2\text{V}^2} = 0.625\,\text{mA/V}^2$$

and is inserted in the **Edit Model** dialog box obtained by the sequence **EDIT-PROPERTIES**. **Vto** is also changed to -4 V. The remaining elements of the network are set as described for the transistor in Chapter 5.

An analysis of the network results in the printout of Fig. 8.63. The **CIRCUIT DESCRIPTION** includes all the elements of the network along with their assigned nodes. In particular, note that **Vi** is set at **10 mV** at a frequency of **10 kHz** and a phase angle of **0** degrees. In the following list of **Junction FET MODEL PARAMETERS** note that **VTO** is -4 V and **BETA** is 625E-6 A/V^2 = 0.625 mA/V^2, as entered earlier. The **SMALL SIGNAL BIAS SOLUTION** reveals that the voltage at both ends of R_G is -1.5 V, resulting in $V_{GS} = -1.5$ V. The voltage levels of this section can be related to the original network by simply noting the assigned node list in the **CIRCUIT DESCRIPTION**. The voltage from drain to source (ground) is 12 V, leaving a drop of 8 V across R_D. The **AC ANALYSIS** listing reveals that the voltage at the source (N01707) is 10 mV as set, but the voltage at the other end of the capacitor is 3 μV less due to the impedance of the capacitor at 10 kHz—certainly a drop to be ignored. The choice of 0.02 μF for this frequency was obviously a good one. The voltages before and after the capacitor on the output side are exactly the same (to three places), revealing that the larger the capacitor, the closer are the characteristics to those of a short circuit. The output of 6.275E-2 = 62.75 mV reflects a gain of 6.275.

The **OPERATING POINT INFORMATION** reveals that I_D is 4 mA and g_m is 3.2 mS. We calculate the value of g_m from

$$g_m = \frac{2I_{DSS}}{|V_P|}\left(1 - \frac{V_{GS_Q}}{V_P}\right)$$

$$g_m = \frac{2(10\,\text{mA})}{4\,\text{V}}\left[1 - \frac{(-1.5\,\text{V})}{(-4\,\text{V})}\right]$$

$$= 3.125\,\text{mS}$$

which confirms our analysis.


```
*****     CIRCUIT DESCRIPTION
******************************************************************************
*Analysis directives:
.AC LIN 1 10kHz 10kHz
V_VDD         N01252 0 20Vdc
R_RD          N00727 N01252  2k
R_RG          N00754 N01282  10Meg
R_RL          0 N01189  10Meg
.PRINT          AC
+ VM([N01707])
.PRINT          AC
+ VM([N01282])
C_C1          N01707 N01282  0.02uF
C_C2          N00727 N01189  2uF
.PRINT          AC
+ VM([N00727])
V_VGG         0 N00754 1.5Vdc
.PRINT          AC
+ VM([N01189])
J_J1          N00727 N01282 0 J2N3819
V_Vi          N01707 0  AC 10mV
+SIN 0 10mV 10Khz 0 0 0
.END

 ****     Junction FET MODEL PARAMETERS
******************************************************************************
               J2N3819
               NJF
         VTO   -4
        BETA   625.000000E-06
      LAMBDA   2.250000E-03
          IS   33.570000E-15
         ISR   322.400000E-15
       ALPHA   311.700000E-06
          VK   243.6
          RD   1
          RS   1
         CGD   1.600000E-12
         CGS   2.414000E-12
           M   .3622
       VTOTC   -2.500000E-03
     BETATCE   -.5
          KF   9.882000E-18

 ****     SMALL SIGNAL BIAS SOLUTION       TEMPERATURE =   27.000 DEG C
******************************************************************************
 NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE
(N00727)   12.0020 (N00754)   -1.5000 (N01189)    0.0000 (N01252)   20.0000
(N01282)   -1.5000 (N01707)    0.0000

    VOLTAGE SOURCE CURRENTS
    NAME         CURRENT
    V_VDD       -3.999E-03
    V_VGG       -1.366E-12
    V_Vi         0.000E+00

 ****     OPERATING POINT INFORMATION      TEMPERATURE =   27.000 DEG C
******************************************************************************
**** JFETS
NAME            J_J1
MODEL           J2N3819
ID              4.00E-03
VGS            -1.50E+00
VDS             1.20E+01
GM              3.20E-03
GDS             8.76E-06
CGS             1.73E-12
CGD             6.07E-13

 ****     AC ANALYSIS                      TEMPERATURE =   27.000 DEG C
******************************************************************************
  FREQ         VM(N01707)
  1.000E+04    1.000E-02

  FREQ         VM(N01282)
  1.000E+04    9.997E-02

  FREQ         VM(N00727)
  1.000E+04    6.275E-02

  FREQ         VM(N01189)
  1.000E+04    6.275E-02
```

FIG. 8.63
Output file for the network of Fig. 8.62.

JFET Voltage-Divider Configuration The next network to be analyzed in the ac domain is the voltage-divider bias configuration of Fig. 8.64. Note that the parameters chosen are different from those employed in earlier examples, with V_i at 24 mV and a frequency of 5 kHz. In addition, the dc levels are displayed, and a plot of the output and input voltages are displayed on the same screen.

To run the analysis, select the **New Simulation Profile** key to obtain the **New Simulation** dialog box. After entering **Name** of **Fig8-64**, select **Create**, and the **Simulation Settings** dialog box will appear. Under **Analysis type**, select **AC/Sweep/Noise**, and then under **AC Sweep** choose **Linear**. The **Start Frequency** is **5 kHz**, the **End Frequency** is **5 kHz** and the **Total Points** is **1**. An **OK**, and the simulation can be initiated by selecting the **Run PSpice** key. A schematic will appear, which can be exited to result in the display of Fig. 8.64 with all the voltage levels displayed as controlled by the **V** option. The resulting dc levels reveal that V_{GS} is 1.823 V $-$ 3.636 V = -1.812 V, comparing very well with the -1.8 V calculated in Example 7.5. V_D is 10.18 V, compared to the calculated level of 10.24 V, and V_{DS} is 10.18 V $-$ 3.635 V = 6.545 V, compared to 6.64 V.

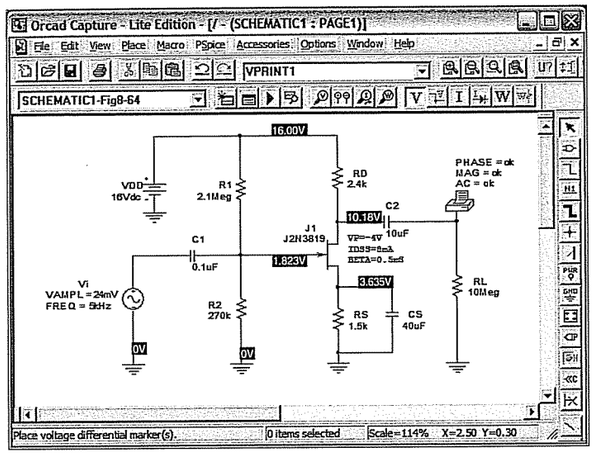


FIG. 8.64

JFET voltage-divider configuration with an ac source.

For the ac solution, we can select **View-Output File** and find under **OPERATING POINT INFORMATION** that g_m is 2.22 mS, comparing very well with the hand-calculated value of 2.2 mS, and under **AC ANALYSIS** that the output ac voltage is 125.8 mV, resulting in a gain of 125.8 mV/24 mV = 5.24. The hand-calculated level is $g_m R_D = (2.2\text{ mS})(2.4\,\text{k}\Omega) = 5.28$.

The ac waveform for the output voltage can be obtained by returning to the **Simulation Settings** dialog box and under **Analysis type** choosing **Time Domain (Transient)**. Then, since the period of a 5-kHz signal is 200 μs, select a **Run to** time of 1 ms, so that five cycles of the waveform will appear. Leave the **Start saving data after** option at 0 s, and under **Transient options** enter a **Maximum step size** of 2 μs, so that we have at least 100 plot points for each cycle of the waveform. An **OK**, and the **SCHEMATIC** screen will appear. Select **Trace-Add Trace-V(J1:d)** and the waveform at the bottom of Fig 8.65 appears. If you then choose **Plot-Add Plot to Window-Trace-Add Trace-V(Vi:+)**, the waveform of the applied voltage appears at the top of Fig. 8.65. Now shift **SEL>>** to the bottom waveform by simply bringing the cursor down to the left of the other waveform and left clicking the mouse once. Now select **Trace-Cursor-Display**, and a horizontal line will appear at the dc level of the output voltage at 10.184 V (note the level of **A1** in the **Probe Cursor** dialog box in the bottom right of the screen). A right click of the mouse, and a second set of intersecting lines will appear. Choose the **Cursor Peak** icon in the toolbar above the display, and the intersection will automatically go to the peak value of the waveform (**A2** in the dialog box). Note that **A2** indicates that the peak value occurs at 150 μs and the instantaneous peak value is 10.31 V. The **dif** is simply the difference between the **A1** and **A2** intersections for time and amplitude.

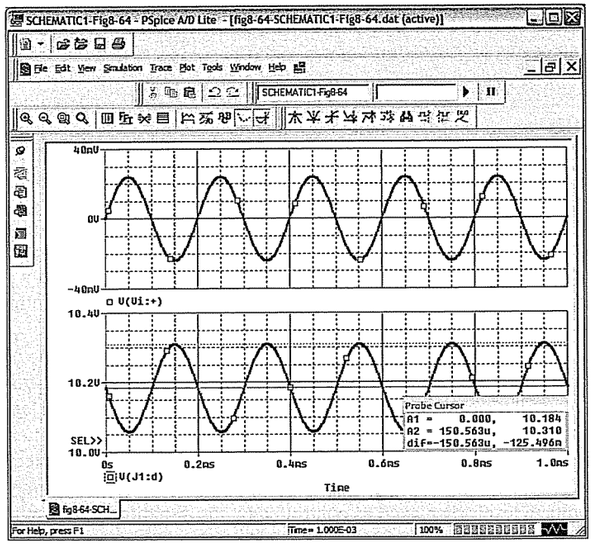


FIG. 8.65

The ac drain and gate voltage for the voltage-divider JFET configuration of Fig. 8.64.

Cascaded JFET Amplifier The extensive two-stage JFET amplifier of Fig. 8.66 can be created using the same procedures described in the previous examples using PSpice. For both JFETs, **Beta** was set at 0.625 mA/V^2 and **Vto** at -4 V as shown in Fig. 8.67. The applied frequency is 10 kHz to ensure that the capacitors take on a short-circuit approximation. The ac output at the output of each stage is requested.

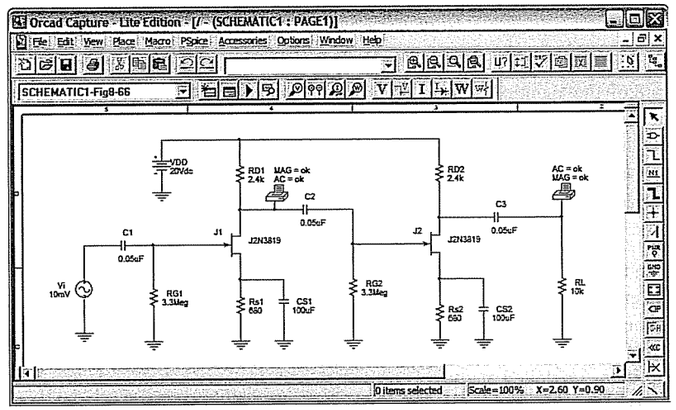


FIG. 8.66

Design Center network for analyzing cascaded JFET amplifiers.

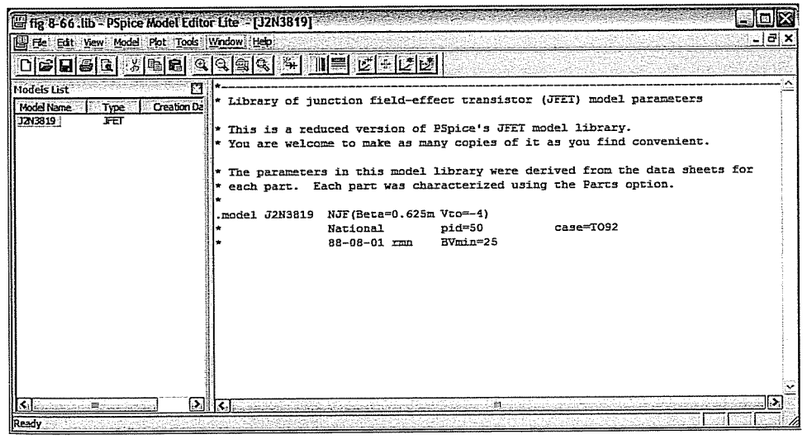


FIG. 8.67

Display of resulting JFET model definition.

After simulation, the output file of Fig. 8.68 results, revealing that the gain is 63.23 mV/10 mV = 6.3 after the first stage and 322.6 mV/10 mV = 32.3 after both stages. The gain for the second stage is 322.6 mV/63.23 mV = 5.1. The gains and output voltage are very close the results obtained in Example 8.1.

```
Cascade JFET Amplifier

****     Junction FET MODEL PARAMETERS
**********************************************
*******
         J2N3819
         NJF
      VTO  -4
    BETA  625.000000E-06

**** JFETS
NAME       J_J2        J_J1
MODEL      J2N3819     J2N3819
ID         2.78E-03    2.78E-03
VGS        -1.89E+00   -1.89E+00
VDS        1.14E+01    1.14E+01
GM         2.64E-03    2.64E-03

****     AC ANALYSIS
**********************************************
*******
 FREQ      VM(N00829)
 1.000E+04 3.226E-01

 FREQ      VM(N00727)
 1.000E+04 6.323E-02
```

FIG. 8.68

PSpice output for the network of Fig. 8.66 (edited).

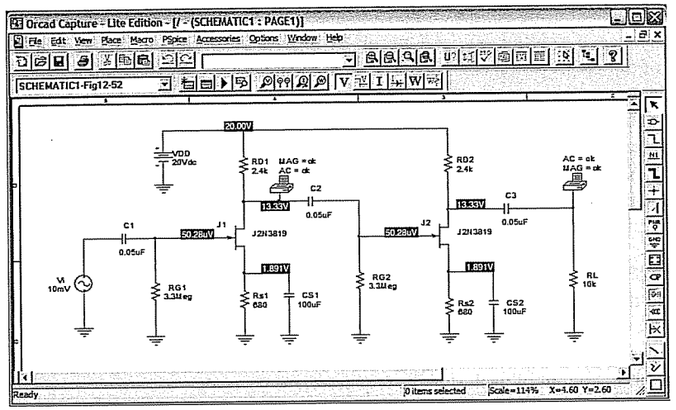


FIG. 8.69
Display showing dc bias levels.

In Fig. 8.69 the **V** option is selected to obtain the dc levels of the network. In particular, note how close the gate voltages are to 0 V, ensuring that the gate-to-source bias voltage is essentially the same as that across the source resistor. In fact, due to the isolation offered by the **C2** capacitor, the bias levels of each configuration are exactly the same.

Multisim

The ac gain for the JFET self-bias network of Fig. 8.70 will now be determined using Multisim. The entire procedure for setting up the network and obtaining the desired readings was described for BJT ac networks in Chapter 5. This particular network will appear again in Chapter 9 as Fig. 9.39 when we turn our attention to the frequency response of a loaded JFET amplifier. A detailed analysis is provided in Chapter 9, including determining the dc levels, the value of g_m, and the loaded gain. The drain current of Example 9.10 is 2 mA, resulting in a drain voltage of 10.6 V and a source voltage of 2 V, which compare very well with the 10.497 V and 2.009 V respectively, of Fig. 8.70. When a load such as R_L is added to the network, it will appear in parallel with R_D of the network, changing the gain equation

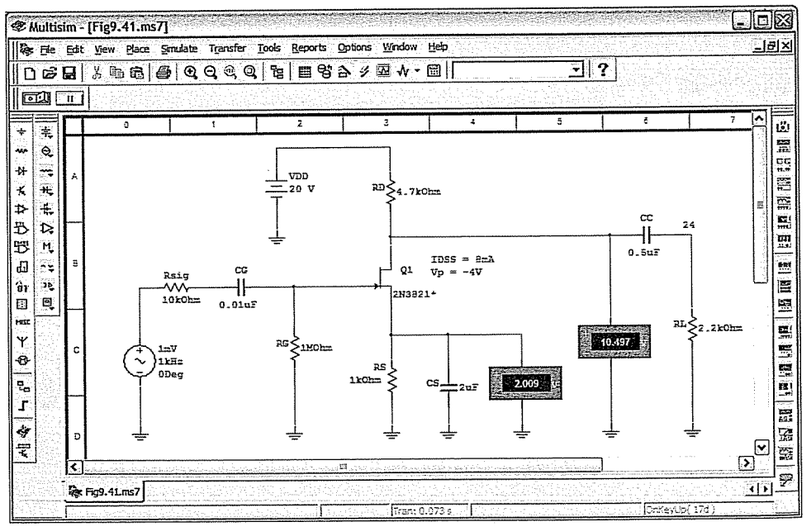


FIG. 8.70
JFET self-bias network using Multisim.

to $-g_m R_D \| R_L$. For Example 9.10, g_m is 2 mS, resulting in an overall gain of $(-2\text{ mS})(2.2\,\text{k}\Omega \| 4.7\,\text{k}\Omega) = -2.997$. The meters of Fig. 8.70 provide the effective values of the voltages at those points. Since we used a power source, the reading of the meter XMM1 is very close to that of the applied source. The difference is due solely to the ac drop of voltage across $\mathbf{R_{sig}}$ and **CG**. The magnitude of the ac gain of the configuration is 2.895 mV/1 mV = 2.895, which is very close to the hand-calculated solution.

PROBLEMS

Note: Asterisks indicate more difficult questions.

8.2 FET Small-Signal Model

1. Calculate g_{m0} for a JFET having device parameters $I_{DSS} = 15$ mA and $V_P = -5$ V.
2. Determine the pinch-off voltage of a JFET with $g_{m0} = 10$ mS and $I_{DSS} = 12$ mA.
3. For a JFET having device parameters $g_{m0} = 5$ mS and $V_P = -3.5$ V, what is the device current at $V_{GS} = 0$ V?
4. Calculate the value of g_m for a JFET ($I_{DSS} = 12$ mA, $V_P = -3$ V) at a bias point of $V_{GS} = -1$ V.
5. For a JFET having $g_m = 6$ mS at $V_{GS_Q} = -1$ V, what is the value of I_{DSS} if $V_P = -2.5$ V?
6. A JFET ($I_{DSS} = 10\text{ mA}, V_P = -5\text{ V}$) is biased at $I_D = I_{DSS}/4$. What is the value of g_m at that bias point?
7. Determine the value of g_m for a JFET ($I_{DSS} = 8$ mA, $V_P = -5$ V) when biased at $V_{GS_Q} = V_P/4$.
8. A specification sheet provides the following data (at a listed drain-source current):
   $$y_{fs} = 4.5\text{ mS}, \qquad y_{os} = 25\ \mu\text{S}$$
   At the listed drain–source current, determine:
   a. g_m.
   b. r_d.
9. For a JFET having specified values of $y_{fs} = 4.5$ mS and $y_{os} = 25\ \mu$S, determine the device output impedance Z_o(FET) and device ideal voltage gain A_v(FET).
10. If a JFET having a specified value of $r_d = 100\,\text{k}\Omega$ has an ideal voltage gain of $A_v(\text{FET}) = -200$, what is the value of g_m?
11. Using the transfer characteristic of Fig. 8.71:
    a. What is the value of g_{m0}?
    b. Determine g_m at $V_{GS} = -1.5$ V graphically.
    c. What is the value of g_m at $V_{GS_Q} = -1.5$ V using Eq. (8.6)? Compare with the solution to part (b).
    d. Graphically determine g_m at $V_{GS} = -2.5$ V.
    e. What is the value of g_m at $V_{GS_Q} = -2.5$ V using Eq. (8.6)? Compare with the solution to part (d).

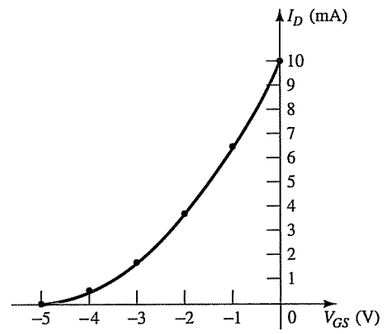


FIG. 8.71
JFET transfer characteristic for Problem 11.

12. Using the drain characteristic of Fig. 8.72:
    a. What is the value of r_d for $V_{GS} = 0$ V?
    b. What is the value of g_{m0} at $V_{DS} = 10$ V?

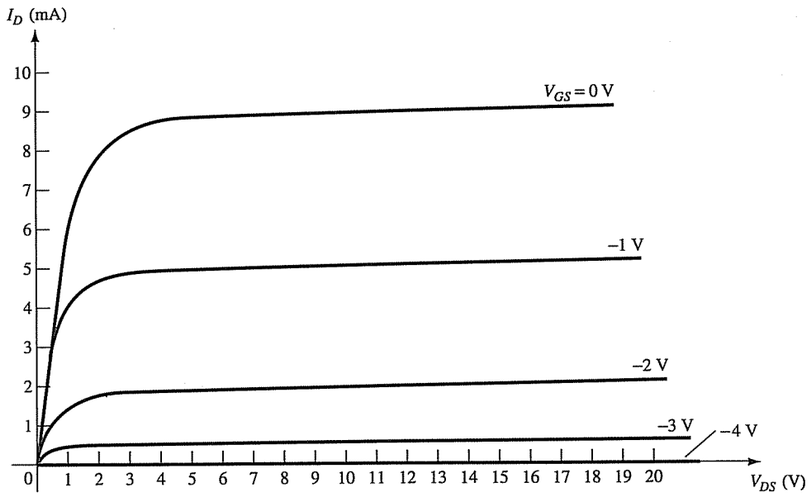


FIG. 8.72
JFET drain characteristic for Problem 12.

13. For a 2N4220 n-channel JFET [y_{fs}(minimum) = 750 μS, y_{os}(maximum) = 10 μS]:
    a. What is the value of g_m?
    b. What is the value of r_d?
14. a. Plot g_m versus V_{GS} for an n-channel JFET with $I_{DSS} = 8$ mA and $V_P = -6$ V.
    b. Plot g_m versus I_D for the same n-channel JFET as part (a).
15. Sketch the ac equivalent model for a JFET if $y_{fs} = 5.6$ mS and $y_{os} = 15$ μS.
16. Sketch the ac equivalent model for a JFET if $I_{DSS} = 10$ mA, $V_P = -4$ V, $V_{GS_Q} = -2$ V, and $y_{os} = 25$ μS.

8.3 JFET Fixed-Bias Configuration

17. Determine Z_i, Z_o, and A_v for the network of Fig. 8.73 if $I_{DSS} = 10$ mA, $V_P = -4$ V, and $r_d = 40$ kΩ.
18. Determine Z_i, Z_o, and A_v for the network of Fig. 8.73 if $I_{DSS} = 12$ mA, $V_P = -6$ V, and $y_{os} = 40$ μS.

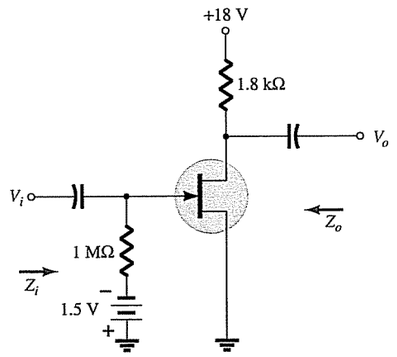


FIG. 8.73
Fixed-bias amplifier for Problems 17 and 18.

8.4 JFET Self-Bias Configuration

19. Determine Z_i, Z_o, and A_v for the network of Fig. 8.74 if $y_{fs} = 3000$ μS and $y_{os} = 50$ μs.
20. Determine Z_i, Z_o, and A_v for the network of Fig. 8.75 if $I_{DSS} = 6$ mA, $V_P = -6$ V, and $y_{os} = 40$ μS.

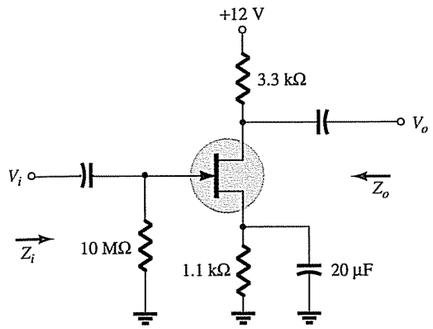


FIG. 8.74
Problems 19, 21, 22 and 46.

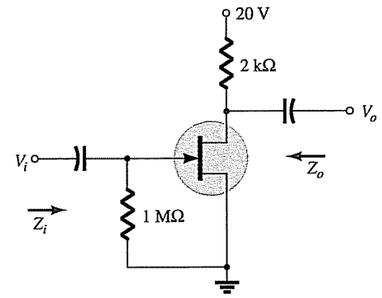


FIG. 8.75
Self-bias configuration for Problems 20 and 47.

21. Determine Z_i, Z_o, and A_v for the network of Fig. 8.74 if the 20-μF capacitor is removed and the parameters of the network are the same as in Problem 19. Compare results with those of Problem 19.
22. Repeat Problem 19 if y_{os} is 10 μS. Compare the results to those of Problem 19.

8.5 JFET Voltage-Divider Configuration

23. Determine Z_i, Z_o, and V_o for the network of Fig. 8.76 if $V_i = 20$ mV.

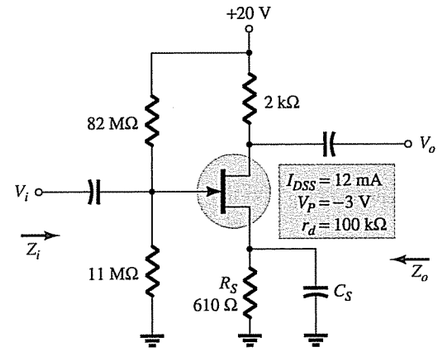


FIG. 8.76
Problems 23 to 26 and 48.

24. Determine Z_i, Z_o, and V_o for the network of Fig. 8.76 if $V_i = 20$ mV and the capacitor C_S is removed.
25. Repeat Problem 23 if $r_d = 20$ kΩ and compare results.
26. Repeat Problem 24 if $r_d = 20$ kΩ and compare results.

8.6 JFET Source-Follower Configuration

27. Determine Z_i, Z_o, and A_v for the network of Fig. 8.77.

28. Repeat Problem 27 if $r_d = 20\,\text{k}\Omega$.

29. Determine Z_i, Z_o, and A_v for the network of Fig. 8.78.

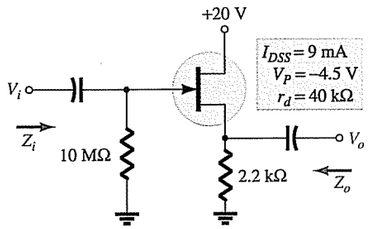


FIG. 8.77
Problems 27 and 28.

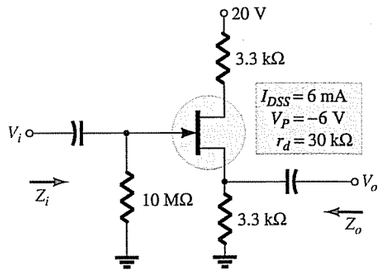


FIG. 8.78
Problem 29.

8.7 JFET Common-Gate Configuration

30. Determine Z_i, Z_o, and V_o for the network of Fig. 8.79 if $V_i = 0.1$ mV.

31. Repeat Problem 30 if $r_d = 25\,\text{k}\Omega$.

32. Determine Z_i, Z_o, and A_v for the network of Fig. 8.80 if $r_d = 33\,\text{k}\Omega$.

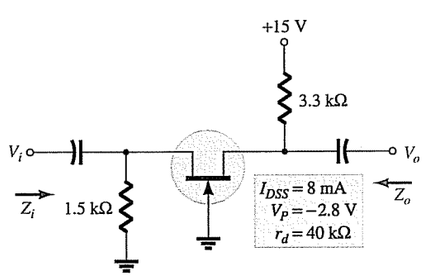


FIG. 8.79
Problems 30, 31, and 49.

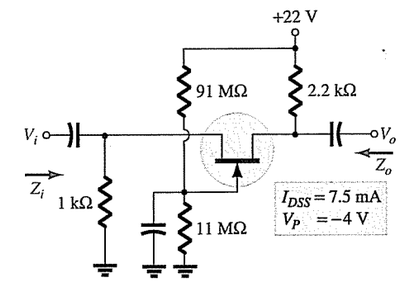


FIG. 8.80
Problem 32.

8.8 Depletion-Type MOSFETs

33. Determine V_o for the network of Fig. 8.81 if $y_{os} = 20\,\mu\text{S}$.

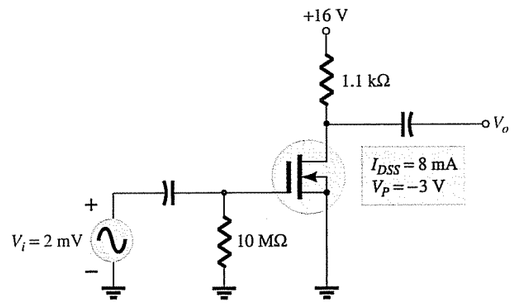


FIG. 8.81
Problem 33.

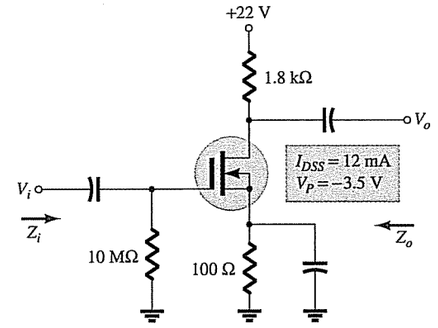


FIG. 8.82
Problems 34, 35, and 50.

34. Determine Z_i, Z_o, and A_v for the network of Fig. 8.82 if $r_d = 60\,\text{k}\Omega$.

35. Repeat Problem 34 if $r_d = 25\,\text{k}\Omega$.

36. Determine V_o for the network of Fig. 8.83 if $V_i = 4$ mV.

37. Determine Z_i, Z_o, and A_v for the network of Fig. 8.84.

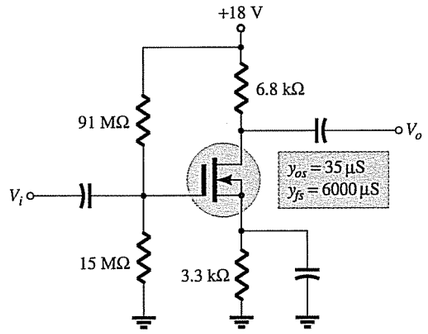


FIG. 8.83
Problem 36.

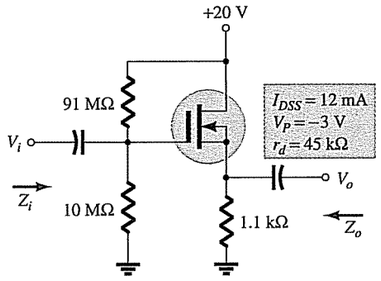


FIG. 8.84
Problem 37.

8.10 E-MOSFET Drain-Feedback Configuration

38. Determine g_m for a MOSFET if $V_{GS(\text{Th})} = 3\,\text{V}$ and it is biased at $V_{GS_Q} = 8\,\text{V}$. Assume $k = 0.3 \times 10^{-3}$.

39. Determine Z_i, Z_o, and A_v for the amplifier of Fig. 8.85 if $k = 0.3 \times 10^{-3}$.

40. Repeat Problem 39 if k drops to 0.2×10^{-3}. Compare results.

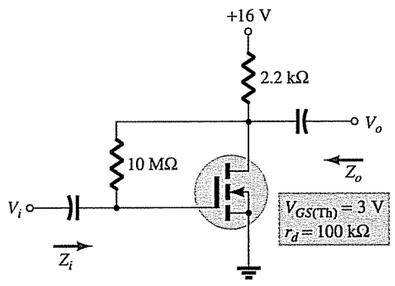


FIG. 8.85
Problems 39, 40, and 51.

41. Determine V_o for the network of Fig. 8.86 if $V_i = 20$ mV.

42. Determine V_o for the network of Fig. 8.86 if $V_i = 4$ mV, $V_{GS(Th)} = 4$ V, and $I_{D(on)} = 4$ mA, with $V_{GS(on)} = 7$ V and $y_{os} = 20\ \mu$S.

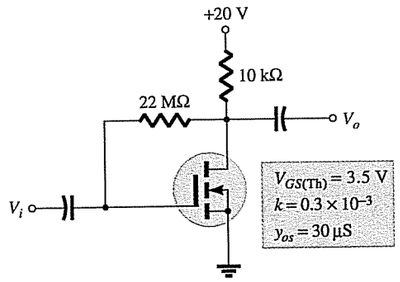


FIG. 8.86
Problems 41 and 42.

8.11 E-MOSFET Voltage-Divider Configuration

43. Determine the output voltage for the network of Fig. 8.87 if $V_i = 0.8$ mV and $r_d = 40$ kΩ.

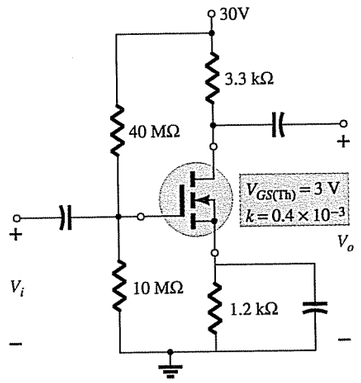


FIG. 8.87
Problem 43.

8.12 Designing FET Amplifier Networks

44. Design the fixed-bias network of Fig. 8.88 to have a gain of 8.

45. Design the self-bias network of Fig. 8.89 to have a gain of 10. The device should be biased at $V_{GS_Q} = \frac{1}{3}V_P$.

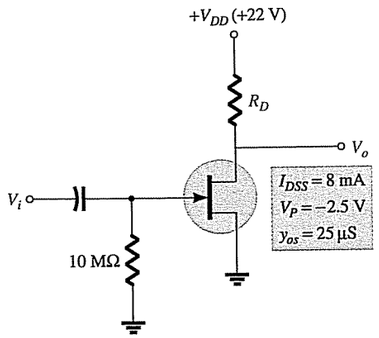


FIG. 8.88
Problem 44.

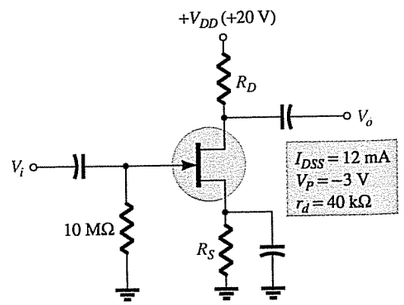


FIG. 8.89
Problem 45.

8.14 Effect of R_L and R_{sig}

46. For the self-bias JFET network of Fig. 8.90:
   a. Determine $A_{v_{NL}}$, Z_i, and Z_o.
   b. Sketch the two-port model of Fig. 5.77 with the parameters determined in part (a) in place.
   c. Determine A_v and A_{v_s}.
   d. Change R_L to 6.8 kΩ and R_{sig} to 1 kΩ and calculate the new levels of A_v and A_{v_s}. How are the voltage gains affected by changes in R_{sig} and R_L?
   e. For the same changes as part (d), determine Z_i and Z_o. What was the effect on both impedances?

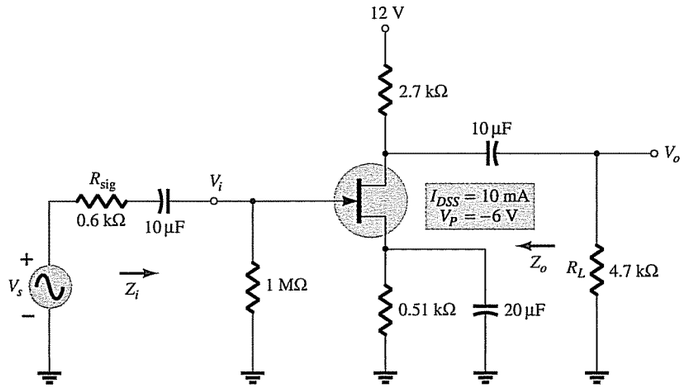


FIG. 8.90
Problem 46.

47. For the source-follower network of Fig. 8.91:
   a. Determine $A_{v_{NL}}$, Z_i, and Z_o.
   b. Sketch the two-port model of Fig. 5.77 with the parameters determined in part (a) in place.
   c. Determine A_v and A_{v_s}.
   d. Change R_L to 4.7 kΩ and calculate A_v and A_{v_s}. What was the effect of increasing levels of R_L on both voltage gains?
   e. Change R_{sig} to 1 kΩ (with R_L at 2.2 kΩ) and calculate A_v and A_{v_s}. What was the effect of increasing levels of R_{sig} on both voltage gains?
   f. Change R_L to 4.7 kΩ and R_{sig} to 1 kΩ and calculate Z_i and Z_o. What was the effect on both parameters?

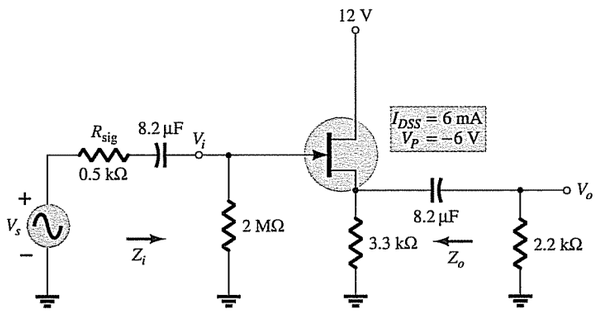


FIG. 8.91
Problem 47.

48. For the common-gate configuration of Fig. 8.92:
- **a.** Determine $A_{v_{NL}}$, Z_i, and Z_o.
- **b.** Sketch the two-port model of Fig. 5.77 with the parameters determined in part (a) in place.
- **c.** Determine A_v and A_{v_s}.

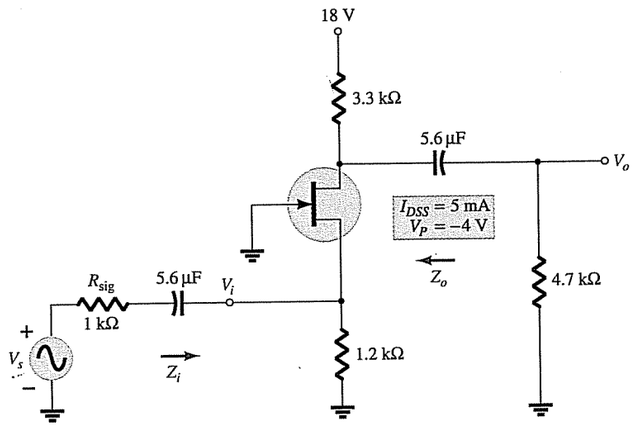


FIG. 8.92
Problem 48.

- **d.** Change R_L to 2.2 kΩ and calculate A_v and A_{v_s}. What was the effect of changing R_L on the voltage gains?
- **e.** Change R_{sig} to 0.5 kΩ (with R_L at 4.7 kΩ) and calculate A_v and A_{v_s}. What was the effect of changing R_{sig} on the voltage gains?
- **f.** Change R_L to 2.2 kΩ and R_{sig} to 0.5 kΩ and calculate Z_i and Z_o. What was the effect on both parameters?

8.15 Cascade Configuration

49. For the JFET cascade amplifier in Fig. 8.93, calculate the dc bias conditions for the two identical stages, using JFETs with $I_{DSS} = 8$ mA and $V_P = -4.5$ V.

50. For the JFET cascade amplifier of Fig. 8.93, using identical JFETs with $I_{DSS} = 8$ mA and $V_P = -4.5$ V, calculate the voltage gain of each stage, the overall gain of the amplifier, and the output voltage V_o.

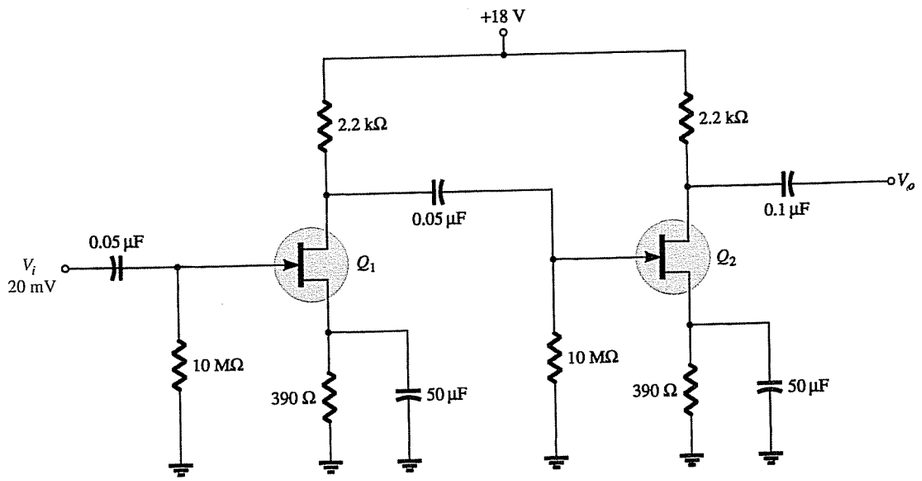


FIG. 8.93
Problems 49 to 53.

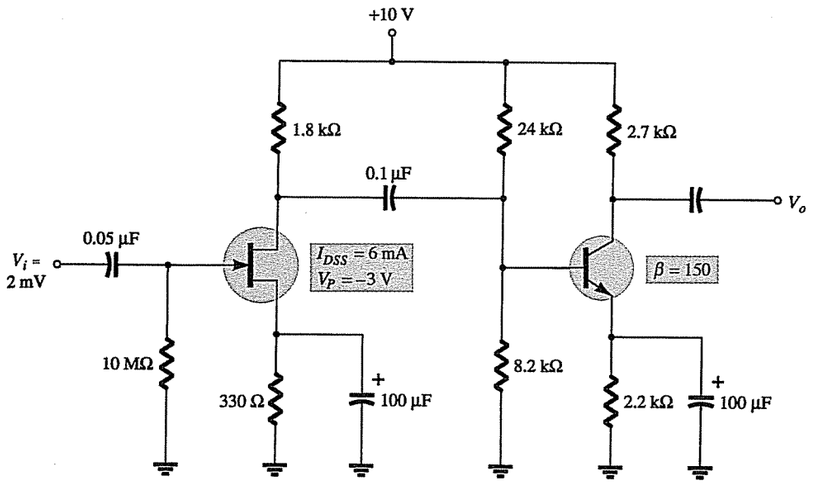


FIG. 8.94
Problems 54 to 56.

51. If both JFETs in the cascade amplifier of Fig. 8.93 are changed to those having specifications $I_{DSS} = 12$ mA and $V_P = -3$ V, calculate the resulting dc bias of each stage.

52. If both JFETs in the cascade amplifier of Fig. 8.93 are changed to those having the specifications $I_{DSS} = 12$ mA, $V_P = -3$ V, and $y_{os} = 25\ \mu$S, calculate the resulting voltage gain for each stage, the overall voltage gain, and the output voltage, V_o.

53. For the cascade amplifier of Fig. 8.93, using JFETs with specifications $I_{DSS} = 12$ mA, $V_P = -3$ V, and $y_{os} = 25\ \mu$S, calculate the circuit input impedance (Z_i) and output impedance (Z_o).

54. For the cascade amplifier of Fig. 8.94, calculate the dc bias voltages and collector current of each stage.

55. For the amplifier circuit of Fig. 8.94, calculate the voltage gain of each stage and the overall amplifier voltage gain.

56. Calculate the input impedance (Z_i) and output impedance (Z_o) for the amplifier circuit of Fig. 8.94.

8.19 Computer Analysis

57. Using PSpice Windows, determine the voltage gain for the network of Fig. 8.74.

58. Using Multisim, determine the voltage gain for the network of Fig. 8.75.

59. Using PSpice Windows, determine the voltage gain for the network of Fig. 8.76.

60. Using Multisim, determine the voltage gain for the network of Fig. 8.79.

61. Using PSpice Windows, determine the voltage gain for the network of Fig. 8.82.

62. Using PSpice Windows, determine the voltage gain for the network of Fig. 8.85.

***63.** Use the Design Center to draw a schematic circuit of the cascade JFET amplifier as in Fig. 8.93. Set the JFET parameters for $I_{DSS} = 12$ mA and $V_P = 3$ V, and have the analysis determine the dc bias.

***64.** Use the Design Center to draw a schematic circuit for a cascade JFET amplifier as shown in Fig. 8.93. Set the analysis to calculate the ac output voltage V_o for $I_{DSS} = 12$ mA and $V_P = -3$ V.

9 BJT and JFET Frequency Response

CHAPTER OUTLINE

9.1 Introduction
9.2 Logarithms
9.3 Decibels
9.4 General Frequency Considerations
9.5 Low-Frequency Analysis—Bode Plot
9.6 Low-Frequency Response—BJT Amplifier
9.7 Low-Frequency Response—FET Amplifier
9.8 Miller Effect Capacitance
9.9 High-Frequency Response—BJT Amplifier
9.10 High-Frequency Response—FET Amplifier
9.11 Multistage Frequency Effects
9.12 Square-Wave Testing
9.13 Summary
9.14 Computer Analysis

9.1 INTRODUCTION

The analysis thus far has been limited to a particular frequency. For the amplifier, it was a frequency that normally permitted ignoring the effects of the capacitive elements, reducing the analysis to one that included only resistive elements and sources of the independent and controlled variety. We will now investigate the frequency effects introduced by the larger capacitive elements of the network at low frequencies and the smaller capacitive elements of the active device at high frequencies. Since the analysis will extend through a wide frequency range, the logarithmic scale will be defined and used throughout the analysis. In addition, since industry typically uses a decibel scale on its frequency plots, the concept of the decibel is introduced in some detail. The similarities between the frequency response analyses of both BJTs and FETs permit the coverage of both in the same chapter.

9.2 LOGARITHMS

In this field, there is no escaping the need to become comfortable with the logarithmic function. The plotting of a variable between wide limits, comparing levels without having to deal with unwieldy numbers, and identifying levels of particular importance in the design, review, and analysis procedures are all positive features of using the logarithmic function.

As a first step in clarifying the relationship between the variables of a logarithmic function, consider the following mathematical equations:

$$\boxed{a = b^x, \qquad x = \log_b a} \tag{9.1}$$

The variables a, b, and x are the same in each equation. If a is determined by taking the base b to the x power, the same x will result if the log of a is taken to the base b. For instance, if $b = 10$ and $x = 2$,

$$a = b^x = (10)^2 = 100$$

but

$$x = \log_b a = \log_{10} 100 = 2$$

In other words, if you were asked to find the power of a number that would result in a particular level such as

$$10{,}000 = 10^x$$

you could determine the level of x using logarithms. That is,

$$x = \log_{10} 10{,}000 = 4$$

For the electrical/electronics industry and in fact for the vast majority of scientific research, the base in the logarithmic equation is chosen as either 10 or the number $e = 2.71828\ldots$.

Logarithms taken to the base 10 are referred to as *common logarithms,* whereas logarithms taken to the base e are referred to as *natural logarithms.* In summary:

$$\boxed{\text{Common logarithm:} \quad x = \log_{10} a} \tag{9.2}$$

$$\boxed{\text{Natural logarithm:} \quad y = \log_e a} \tag{9.3}$$

The two are related by

$$\boxed{\log_e a = 2.3 \log_{10} a} \tag{9.4}$$

On scientific calculators, the common logarithm is typically denoted by the **log** key and the natural logarithm by the **ln** key.

EXAMPLE 9.1 Using the calculator, determine the logarithm of the following numbers to the base indicated:

a. $\log_{10} 10^6$.
b. $\log_e e^3$.
c. $\log_{10} 10^{-2}$.
d. $\log_e e^{-1}$.

Solution:

a. **6** b. **3** c. **−2** d. **−1**

The results in Example 9.1 clearly reveal that the logarithm of a number taken to a power is simply the power of the number if the number matches the base of the logarithm. In the next example, the base and the variable x are not related by an integer power of the base.

EXAMPLE 9.2 Using the calculator, determine the logarithm of the following numbers:

a. $\log_{10} 64$.
b. $\log_e 64$.
c. $\log_{10} 1600$.
d. $\log_{10} 8000$.

Solution:

a. **1.806** b. **4.159** c. **3.204** d. **3.903**

Note in parts (a) and (b) of Example 9.2 that the logarithms $\log_{10} a$ and $\log_e a$ are indeed related as defined by Eq. (9.4). In addition, note that the logarithm of a number does not increase in the same linear fashion as the number. That is, 8000 is 125 times larger than 64, but the logarithm of 8000 is only about 2.16 times larger than the magnitude of the logarithm of 64, revealing a very nonlinear relationship. In fact, Table 9.1 clearly shows how the logarithm of a number increases only as the exponent of the number. If the antilogarithm of a number is desired, the 10^x or e^x calculator function is employed.

TABLE 9.1

$\log_{10} 10^0$	$= 0$
$\log_{10} 10$	$= 1$
$\log_{10} 100$	$= 2$
$\log_{10} 1{,}000$	$= 3$
$\log_{10} 10{,}000$	$= 4$
$\log_{10} 100{,}000$	$= 5$
$\log_{10} 1{,}000{,}000$	$= 6$
$\log_{10} 10{,}000{,}000$	$= 7$
$\log_{10} 100{,}000{,}000$	$= 8$
etc.	

EXAMPLE 9.3 Using a calculator, determine the antilogarithm of the following expressions:

a. $1.6 = \log_{10} a$.
b. $0.04 = \log_e a$.

Solution:

a. $a = 10^{1.6}$
Calculator keys: [1] [.] [6] [2nd F] [10^x]
and $a = \mathbf{39.81}$
b. $a = e^{0.04}$
Calculator keys: [0] [.] [0] [4] [2nd F] [e^x]
and $a = \mathbf{1.0408}$

Since the remaining analysis of this chapter employs the common logarithm, we review a few properties of logarithms using solely the common logarithm. In general, however, the same relationships hold true for logarithms to any base. First, note that

$$\log_{10} 1 = 0 \tag{9.5}$$

as clearly revealed by Table 9.1, since $10^0 = 1$. Next,

$$\log_{10} \frac{a}{b} = \log_{10} a - \log_{10} b \tag{9.6}$$

which for the special case of $a = 1$ becomes

$$\log_{10} \frac{1}{b} = -\log_{10} b \tag{9.7}$$

which shows that for any b greater than 1, the logarithm of a number less than 1 is always negative. Finally,

$$\log_{10} ab = \log_{10} a + \log_{10} b \tag{9.8}$$

In each case, the equations employing natural logarithms have the same format.

EXAMPLE 9.4 Using a calculator, determine the logarithm of the following numbers:

a. $\log_{10} 0.5$.
b. $\log_{10} \frac{4000}{250}$.
c. $\log_{10} (0.6 \times 30)$.

Solution:

a. $\mathbf{-0.3}$
b. $\log_{10} 4000 - \log_{10} 250 = 3.602 - 2.398 = \mathbf{1.204}$
Check: $\log_{10} \frac{4000}{250} = \log_{10} 16 = \mathbf{1.204}$
c. $\log_{10} 0.6 + \log_{10} 30 = -0.2218 + 1.477 = \mathbf{1.255}$
Check: $\log_{10} (0.6 \times 30) = \log_{10} 18 = \mathbf{1.255}$

The use of log scales can significantly expand the range of variation of a particular variable on a graph. Most graph paper available is of the semilog or double-log (log-log) variety. The term *semi* (meaning one-half) indicates that only one of the two scales is a log scale, whereas double-log indicates that both scales are log scales. A semilog scale appears in Fig. 9.1. Note that the vertical scale is a linear scale with equal divisions. The spacing between the lines of the log plot is shown on the graph. The log of 2 to the base 10 is approximately 0.3. The distance from 1 ($\log_{10} 1 = 0$) to 2 is therefore 30% of the span. The log of 3 to the base 10 is 0.4771 or almost 48% of the span (very close to one-half the

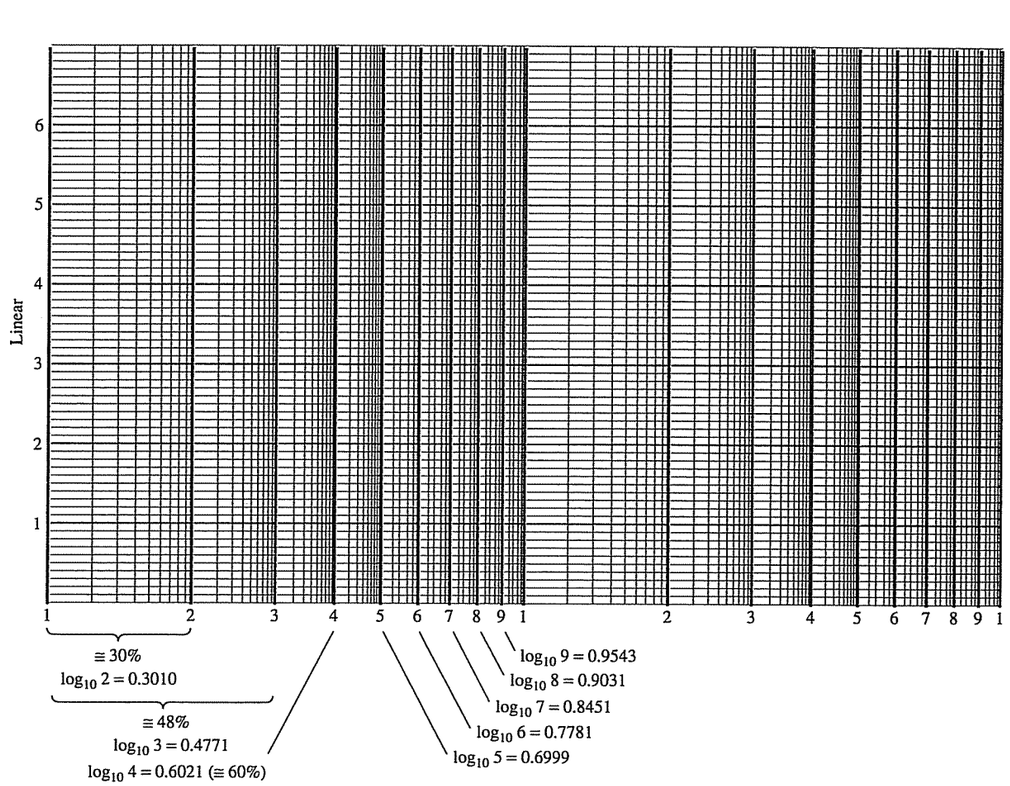


FIG. 9.1
Semilog graph paper.

distance between power-of-10 increments on the log scale). Since $\log_{10} 5 \cong 0.7$, it is marked off at a point 70% of the distance. Note that between any two digits the same compression of the lines appears as you progress from the left to the right. It is important to note the resulting numerical value and the spacing, since plots will typically only have the tic marks indicated in Fig.9.2 due to a lack of space. The longer bars for this figure have the numerical values of 0.3, 3, and 30 associated with them, whereas the next-shorter bars have values of 0.5, 5, and 50 and the shortest bars 0.7, 7, and 70.

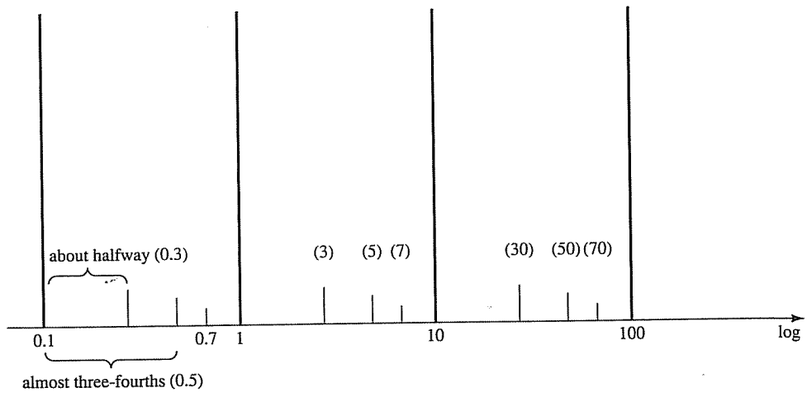


FIG. 9.2
Identifying the numerical values of the tic marks on a log scale.

Plotting a function on a log scale can change the general appearance of the waveform as compared to a plot on a linear scale. A straight-line plot on a linear scale can develop a curve on a log scale, and a nonlinear plot on a linear scale can take on the appearance of a straight line on a log plot. The important point is that the results extracted at each level should be correctly labeled by developing a familiarity with the spacing of Figs. 9.1 and 9.2. This is particularly true for some of the log-log plots that appear later in the book.

9.3 DECIBELS

The concept of the decibel (dB) and the associated calculations will become increasingly important in the remaining sections of this chapter. The term *decibel* has its origin in the fact that power and audio levels are related on a logarithmic basis. That is, an increase in power level from, say, 4 W to 16 W does not result in an audio level increase by a factor of $16/4 = 4$, but by a factor of 2, as derived from the power of 4 in the following manner: $(4)^2 = 16$. For a change of 4 W to 64 W, the audio level will increase by a factor of 3 since $(4)^3 = 64$. In logarithmic form, the relationship can be written as $\log_4 64 = 3$.

The term *bel* is derived from the surname of Alexander Graham Bell. For standardization, the bel (B) is defined by the following equation relating two power levels, P_1 and P_2:

$$G = \log_{10} \frac{P_2}{P_1} \quad \text{bel} \tag{9.9}$$

It was found, however, that the bel was too large a unit of measurement for practical purposes, so the decibel (dB) is defined such that 10 decibels = 1 bel. Therefore,

$$G_{\text{dB}} = 10 \log_{10} \frac{P_2}{P_1} \quad \text{dB} \tag{9.10}$$

The terminal rating of electronic communication equipment (amplifiers, microphones, etc.) is commonly in decibels. Equation (9.10) indicates clearly, however, that the decibel rating is a measure of the difference in magnitude between *two* power levels. For a specified terminal (output) power (P_2) there must be a reference power level (P_1). The reference level is generally accepted to be 1 mW, although on occasion, the 6-mW standard of earlier years is applied. The resistance associated with the 1-mW power level is 600 Ω, chosen because it is the characteristic impedance of audio transmission lines. When the 1-mW level is employed as the reference level, the decibel symbol frequently appears as dBm. In equation form,

$$G_{\text{dBm}} = 10 \log_{10} \frac{P_2}{1\ \text{mW}}\bigg|_{600\ \Omega} \quad \text{dBm} \tag{9.11}$$

There exists a second equation for decibels that is applied frequently. It can be best described through the system of Fig. 9.3. For V_i equal to some value V_1, $P_1 = V_1^2/R_i$, where R_i is the input resistance of the system of Fig. 9.3. If V_i should be increased (or decreased) to some other level, V_2 then $P_2 = V_2^2/R_i$. If we substitute into Eq. (9.10) to determine the resulting difference in decibels between the power levels, we obtain

$$G_{\text{dB}} = 10 \log_{10} \frac{P_2}{P_1} = 10 \log_{10} \frac{V_2^2/R_i}{V_1^2/R_i} = 10 \log_{10} \left(\frac{V_2}{V_1}\right)^2$$

and

$$G_{\text{dB}} = 20 \log_{10} \frac{V_2}{V_1} \quad \text{dB} \tag{9.12}$$

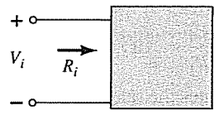


FIG. 9.3
Configuration employed in the discussion of Eq. (9.12).

Frequently, the effect of different impedances ($R_1 \neq R_2$) is ignored and Eq. (9.12) applied simply to establish a basis of comparison between levels—voltage or current. For situations of this type, the decibel gain should more correctly be referred to as the voltage or current gain in decibels to differentiate it from the common usage of decibel as applied to power levels.

One of the advantages of the logarithmic relationship is the manner in which it can be applied to cascaded stages. For example, the magnitude of the overall voltage gain of a cascaded system is given by

$$|A_{v_T}| = |A_{v_1}| \cdot |A_{v_2}| \cdot |A_{v_3}| \cdots |A_{v_n}| \tag{9.13}$$

Applying the proper logarithmic relationship results in

$$G_v = 20 \log_{10} |A_{v_T}| = 20 \log_{10} |A_{v_1}| + 20 \log_{10} |A_{v_2}| + 20 \log_{10} |A_{v_3}| + \cdots + 20 \log_{10} |A_{v_n}| \quad \text{(db)} \tag{9.14}$$

In words, the equation states that the decibel gain of a cascaded system is simply the sum of the decibel gains of each stage, that is,

$$G_{\text{dB}_T} = G_{\text{dB}_1} + G_{\text{dB}_2} + G_{\text{dB}_3} + \cdots + G_{\text{dB}_n} \quad \text{dB} \tag{9.15}$$

Table 9.2 shows the association between dB levels and voltage gains. First note that a gain of 2 results in a dB level of +6 dB, whereas a drop to $\frac{1}{2}$ results in a −6-dB level. A change in V_o/V_i from 1 to 10, 10 to 100, or 100 to 1000 results in the same 20-dB change in level. When $V_o = V_i$, $V_o/V_i = 1$, and the dB level is 0. At a very high gain of 1000, the dB level is 60, whereas at the much higher gain of 10,000, the dB level is 80 dB, an increase of only 20 dB—a result of the logarithmic relationship. Table 9.2 clearly reveals that voltage gains of 50 dB or higher should immediately be recognized as being quite high.

TABLE 9.2

Comparing $A_v = \dfrac{V_o}{V_i}$ *to dB*

Voltage Gain, V_o/V_i	dB Level
0.5	−6
0.707	−3
1	0
2	6
10	20
40	32
100	40
1000	60
10,000	80
etc.	

EXAMPLE 9.5 Find the magnitude gain corresponding to a voltage gain of 100 dB.

Solution: By Eq. (9.12),

$$G_{\text{dB}} = 20\log_{10}\frac{V_2}{V_1} = 100\text{ dB} \Rightarrow \log_{10}\frac{V_2}{V_1} = 5$$

so that

$$\frac{P_2}{P_1} = \mathbf{10^5 = 100{,}000}$$

This example clearly demonstrates the range of decibel values to be expected from practical devices. Certainly, a calculation giving a decibel result in the neighborhood of 100 should be questioned immediately.

EXAMPLE 9.6 The input power to a device is 10,000 W at a voltage of 1000 V. The output power is 500 W and the output impedance is 20 Ω.

a. Find the power gain in decibels.
b. Find the voltage gain in decibels.
c. Explain why parts (a) and (b) agree or disagree.

Solution:

a. $G_{\text{dB}} = 10\log_{10}\dfrac{P_o}{P_i} = 10\log_{10}\dfrac{500\text{ W}}{10\text{ kW}} = 10\log_{10}\dfrac{1}{20} = -10\log_{10}20$

$= -10(1.301) = \mathbf{-13.01\text{ dB}}$

b. $G_v = 20\log_{10}\dfrac{V_o}{V_i} = 20\log_{10}\dfrac{\sqrt{PR}}{1000} = 20\log_{10}\dfrac{\sqrt{(500\text{ W})(20\ \Omega)}}{1000\text{ V}}$

$= 20\log_{10}\dfrac{100}{1000} = 20\log_{10}\dfrac{1}{10} = -20\log_{10}10 = \mathbf{-20\text{ dB}}$

c. $R_i = \dfrac{V_i^2}{P_i} = \dfrac{(1\text{ kV})^2}{10\text{ kW}} = \dfrac{10^6}{10^4} = \mathbf{100\ \Omega} \neq R_o = \mathbf{20\ \Omega}$

EXAMPLE 9.7 An amplifier rated at 40-W output is connected to a 10-Ω speaker.

a. Calculate the input power required for full power output if the power gain is 25 dB.
b. Calculate the input voltage for rated output if the amplifier voltage gain is 40 dB.

Solution:

a. Eq. (9.10): $25 = 10\log_{10}\dfrac{40\text{ W}}{P_i} \Rightarrow P_i = \dfrac{40\text{ W}}{\text{antilog}\,(2.5)} = \dfrac{40\text{ W}}{3.16\times10^2}$

$= \dfrac{40\text{ W}}{316} \cong \mathbf{126.5\text{ mW}}$

b. $G_v = 20\log_{10}\dfrac{V_o}{V_i} \Rightarrow 40 = 20\log_{10}\dfrac{V_o}{V_i}$

$\dfrac{V_o}{V_i} = \text{antilog}\,2 = 100$

$V_o = \sqrt{PR} = \sqrt{(40\text{ W})(10\text{ V})} = 20\text{ V}$

$V_i = \dfrac{V_o}{100} = \dfrac{20\text{ V}}{100} = 0.2\text{ V} = \mathbf{200\text{ mV}}$

Mathcad

There are a number of ways to obtain the log of a number or an expression using Mathcad. The most direct is simply to type **log( )**, insert the quantity of interest within the brackets, and then select the equal sign. The result appears immediately.

Another approach is to use the sequence **View-Toolbars-Calculator**; the **Calculator** with all its options will appear on the screen. Selecting log will result in **log( )** with a request for the quantity in the brackets.

Lastly, the sequence **Insert-Function** will result in an **Insert Function** dialog box, from which **Log and Exponential** can be chosen under **Function Category** and **Log** under **Function Name**.

For Example 9.6, part (a) will appear as shown in Fig. 9.4. In Example 9.7, the antilogarithm is required in part (b). Keeping in mind that if $x = \log_b a$, then $a = b^x$, we can simply insert $b = 10$ and $x = 2$ into the equation $a = 10^2 = 100$ as shown in Fig. 9.4. To obtain the power of a number using Mathcad, simply use the **Shift** + ^ keys and insert the power followed by the equal sign.

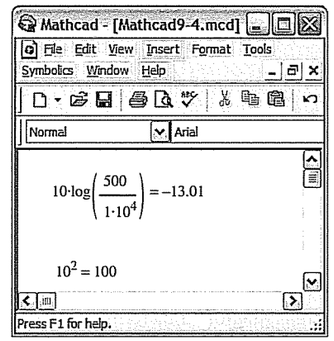


FIG. 9.4
Example 9.6, part (a), using Mathcad.

9.4 GENERAL FREQUENCY CONSIDERATIONS

The frequency of the applied signal can have a pronounced effect on the response of a single-stage or multistage network. The analysis thus far has been for the midfrequency spectrum. At low frequencies, we shall find that the coupling and bypass capacitors can no longer be replaced by the short-circuit approximation because of the increase in reactance of these elements. The frequency-dependent parameters of the small-signal equivalent circuits and the stray capacitive elements associated with the active device and the network will limit the high-frequency response of the system. An increase in the number of stages of a cascaded system will also limit both the high- and low-frequency responses.

The magnitudes of the gain response curves of an *RC*-coupled, direct-coupled, and transformer-coupled amplifier system are provided in Fig. 9.5. Note that the horizontal scale is a logarithmic scale to permit a plot extending from the low- to the high-frequency regions. For each plot, a low-, a high-, and a mid-frequency region has been defined. In addition, the primary reasons for the drop in gain at low and high frequencies have also been indicated

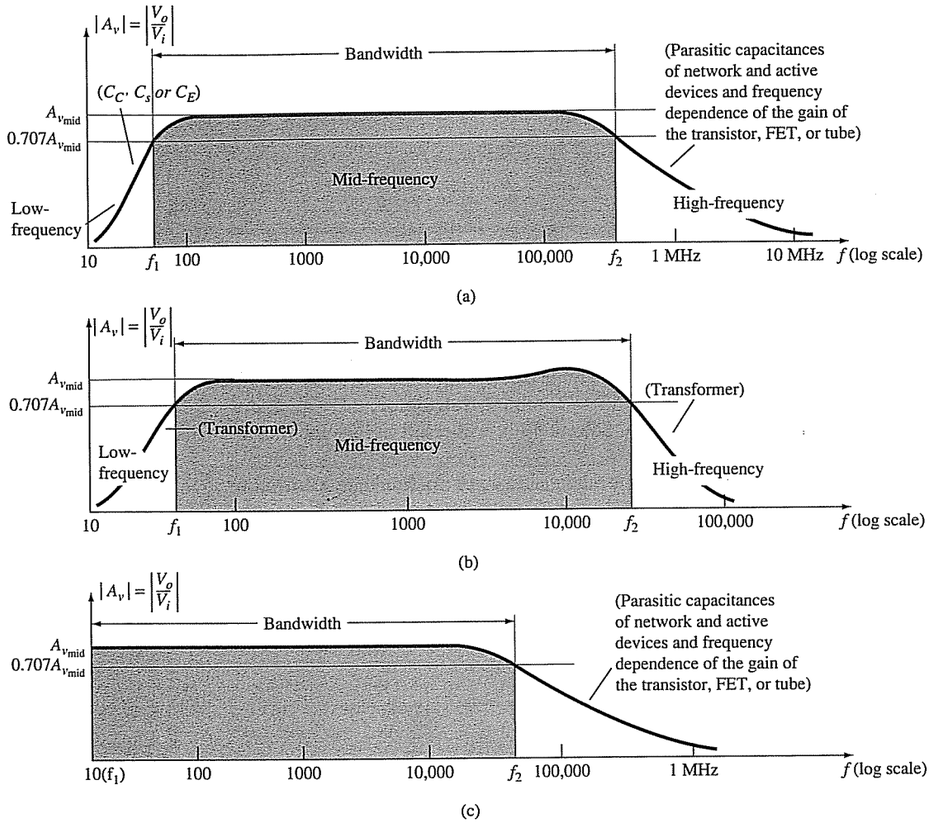


FIG. 9.5

Gain versus frequency: (a) RC-coupled amplifiers; (b) transformer-coupled amplifiers; (c) direct-coupled amplifiers.

within the parentheses. For the *RC*-coupled amplifier, the drop at low frequencies is due to the increasing reactance of C_C, C_s, or C_E, whereas its upper frequency limit is determined by either the parasitic capacitive elements of the network or the frequency dependence of the gain of the active device. An explanation of the drop in gain for the transformer-coupled system requires a basic understanding of "transformer action" and the transformer equivalent circuit. For the moment, let us say that it is simply due to the "shorting effect" (across the input terminals of the transformer) of the magnetizing inductive reactance at low frequencies ($X_L = 2\pi fL$). The gain must obviously be zero at $f = 0$ since at this point there is no longer a changing flux established through the core to induce a secondary or output voltage. As indicated in Fig. 9.5, the high-frequency response is controlled primarily by the stray capacitance between the turns of the primary and secondary windings. For the direct-coupled amplifier, there are no coupling or bypass capacitors to cause a drop in gain at low frequencies. As the figure indicates, it is a flat response to the upper cutoff frequency, which is determined by either the parasitic capacitances of the circuit or the frequency dependence of the gain of the active device.

For each system of Fig. 9.5, there is a band of frequencies in which the magnitude of the gain is either equal or relatively close to the midband value. To fix the frequency boundaries of relatively high gain, $0.707A_{v_{mid}}$ was chosen to be the gain at the cutoff levels. The corresponding frequencies f_1 and f_2 are generally called the *corner, cutoff, band, break,* or *half-power frequencies.* The multiplier 0.707 was chosen because at this level the output power is half the midband power output, that is, at midfrequencies,

$$P_{o_{mid}} = \frac{|V_o^2|}{R_o} = \frac{|A_{v_{mid}} V_i|^2}{R_o}$$

and at the half-power frequencies,

$$P_{o_{HPF}} = \frac{|0.707\, A_{v_{mid}} V_i|^2}{R_o} = 0.5\,\frac{|A_{v_{mid}} V_i|^2}{R_o}$$

and

$$\boxed{P_{o_{HPF}} = 0.5\, P_{o_{mid}}} \qquad \textbf{(9.16)}$$

The bandwidth (or passband) of each system is determined by f_1 and f_2, that is,

$$\boxed{\text{bandwidth (BW)} = f_2 - f_1} \qquad \textbf{(9.17)}$$

For applications of a communications nature (audio, video), a decibel plot of the voltage gain versus frequency is more useful than that appearing in Fig. 9.5. Before obtaining the logarithmic plot, however, the curve is generally normalized as shown in Fig. 9.6. In this figure, the gain at each frequency is divided by the midband value. Obviously, the midband value is then 1 as indicated. At the half-power frequencies, the resulting level is $0.707 = 1/\sqrt{2}$. A decibel plot can now be obtained by applying Eq. (9.12) in the following manner:

$$\boxed{\left.\frac{A_v}{A_{v_{mid}}}\right|_{dB} = 20\log_{10}\frac{A_v}{A_{v_{mid}}}} \qquad \textbf{(9.18)}$$

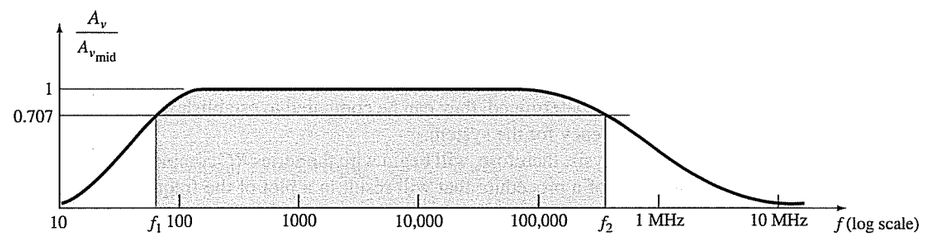


FIG. 9.6

Normalized gain versus frequency plot.

At midband frequencies, $20\log_{10} 1 = 0$, and at the cutoff frequencies, $20\log_{10} 1/\sqrt{2} = -3$ dB. Both values are clearly indicated in the resulting decibel plot of Fig. 9.7. The smaller the fraction ratio, the more negative is the decibel level.

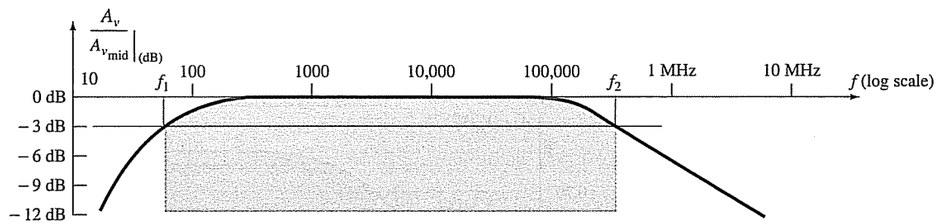


FIG. 9.7

Decibel plot of the normalized gain versus frequency plot of Fig. 9.6.

For the greater part of the discussion to follow, a decibel plot will be made only for the low- and high-frequency regions. Keep Fig. 9.7 in mind, therefore, to permit a visualization of the broad system response.

Most amplifiers introduce a 180° phase shift between input and output signals. This fact must now be expanded to indicate that this is the case only in the midband region. At low frequencies, there is a phase shift such that V_o lags V_i by an increased angle. At high frequencies, the phase shift drops below 180°. Figure 9.8 is a standard phase plot for an *RC*-coupled amplifier.

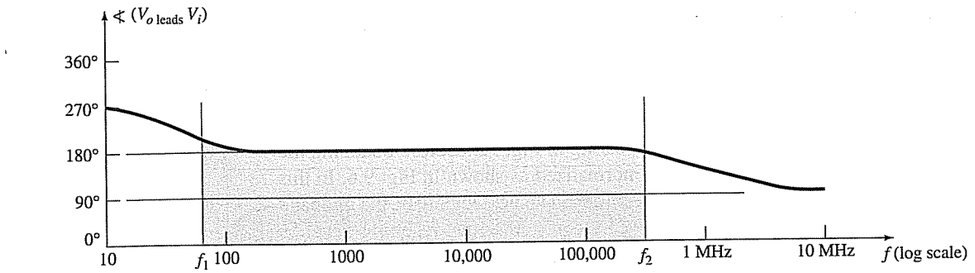


FIG. 9.8
Phase plot for an RC-coupled amplifier system.



Multisim

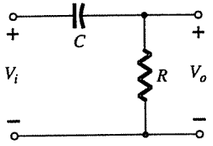


FIG. 9.9
RC combination that will define a low-cutoff frequency.

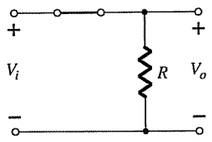


FIG. 9.10
RC circuit of Fig. 9.9 at very high frequencies.

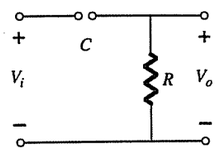


FIG. 9.11
RC circuit of Fig. 9.9 at $f = 0$ Hz.

9.5 LOW-FREQUENCY ANALYSIS—BODE PLOT

In the low-frequency region of the single-stage BJT or FET amplifier, it is the *RC* combinations formed by the network capacitors C_C, C_E, and C_s and the network resistive parameters that determine the cutoff frequencies. In fact, an *RC* network similar to Fig. 9.9 can be established for each capacitive element, and the frequency at which the output voltage drops to 0.707 of its maximum value can be determined. Once the cutoff frequencies due to each capacitor are determined, they can be compared to establish which will determine the low-cutoff frequency for the system.

Our analysis, therefore, will begin with the series *RC* combination of Fig. 9.9 and the development of a procedure that will result in a plot of the frequency response with a minimum of time and effort. At very high frequencies,

$$X_C = \frac{1}{2\pi fC} \cong 0\ \Omega$$

and the short-circuit equivalent can be substituted for the capacitor as shown in Fig. 9.10. The result is that $V_o \cong V_i$ at high frequencies. At $f = 0$ Hz,

$$X_C = \frac{1}{2\pi fC} = \frac{1}{2\pi(0)C} = \infty\Omega$$

and the open-circuit approximation can be applied as shown in Fig. 9.11, with the result that $V_o = 0$ V.

Between the two extremes, the ratio $A_v = V_o/V_i$ will vary as shown in Fig. 9.12. As the frequency increases, the capacitive reactance decreases and more of the input voltage appears across the output terminals.

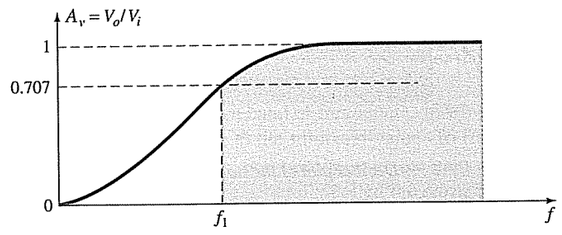


FIG. 9.12
Low-frequency response for the RC circuit of Fig. 9.9.

The output and input voltages are related by the voltage-divider rule in the following manner:

$$\mathbf{V_o = \frac{RV_i}{R + X_C}}$$

with the magnitude of V_o determined by

$$V_o = \frac{RV_i}{\sqrt{R^2 + X_C^2}}$$

For the special case where $X_C = R$,

$$V_o = \frac{RV_i}{\sqrt{R^2X_C^2}} = \frac{RV_i}{\sqrt{R^2 + R^2}} = \frac{RV_i}{\sqrt{2R^2}} = \frac{RV_i}{\sqrt{2}R} = \frac{1}{\sqrt{2}}V_i$$

and

$$\boxed{|A_v| = \frac{V_o}{V_i} = \frac{1}{\sqrt{2}} = 0.707|_{X_C=R}} \qquad \textbf{(9.19)}$$

the level of which is indicated on Fig. 9.12. In other words, at the frequency for which $X_C = R$, the output will be 70.7% of the input for the network of Fig. 9.9.

The frequency at which this occurs is determined from

$$X_C = \frac{1}{2\pi f_1 C} = R$$

and

$$\boxed{f_1 = \frac{1}{2\pi RC}} \qquad \textbf{(9.20)}$$

In terms of logs,

$$G_v = 20\log_{10}A_v = 20\log_{10}\frac{1}{\sqrt{2}} = -3\ \text{dB}$$

whereas at $A_v = V_o/V_i = 1$ or $V_o = V_i$ (the maximum value),

$$G_v = 20\log_{10}1 = 20(0) = 0\ \text{dB}$$

In Fig. 9.7, we recognize that there is a 3-dB drop in gain from the midband level when $f = f_1$. In a moment, we will find that an *RC* network will determine the low-frequency cutoff for a BJT transistor and f_1 will be determined by Eq. (9.20).

If the gain equation is written as

$$A_v = \frac{V_o}{V_i} = \frac{R}{R - jX_C} = \frac{1}{1 - j(X_C/R)} = \frac{1}{1 - j(1/\omega CR)} = \frac{1}{1 - j(1/2\pi fCR)}$$

we obtain, using the frequency defined above,

$$\boxed{A_v = \frac{1}{1 - j(f_1/f)}} \qquad \textbf{(9.21)}$$

In the magnitude and phase form,

$$A_v = \frac{V_o}{V_i} = \underbrace{\frac{1}{\sqrt{1 + (f_1/f)^2}}}_{\text{magnitude of } A_v}\ \underbrace{/\tan^{-1}(f_1/f)}_{\substack{\text{phase } \sphericalangle \text{ by which} \\ V_o \text{ leads } V_i}} \qquad \textbf{(9.22)}$$

For the magnitude when $f = f_1$,

$$|A_v| = \frac{1}{\sqrt{1 + (1)^2}} = \frac{1}{\sqrt{2}} = 0.707 \Rightarrow -3\ \text{dB}$$

In the logarithmic form, the gain in dB is

$$\boxed{A_{v(\text{dB})} = 20\log_{10}\frac{1}{\sqrt{1+(f_1/f)^2}}} \tag{9.23}$$

$$A_{v(\text{dB})} = -20\log_{10}\left[1+\left(\frac{f_1}{f}\right)^2\right]^{1/2}$$

$$= -\left(\tfrac{1}{2}\right)(20)\log_{10}\left[1+\left(\frac{f_1}{f}\right)^2\right]$$

$$= -10\log_{10}\left[1+\left(\frac{f_1}{f}\right)^2\right]$$

For frequencies where $f \ll f_1$ or $(f_1/f)^2 \gg 1$, the equation above can be approximated by

$$A_{v(\text{dB})} = -10\log_{10}\left(\frac{f_1}{f}\right)^2$$

and finally,

$$\boxed{A_{v(\text{dB})} = -20\log_{10}\frac{f_1}{f}} \quad f \ll f_1 \tag{9.24}$$

Ignoring the condition $f \ll f_1$ for a moment, we find that a plot of Eq. (9.24) on a frequency log scale yields a result very useful for future decibel plots.

$$\text{At } f = f_1\text{: } \frac{f_1}{f} = 1 \text{ and } -20\log_{10} 1 = 0 \text{ dB}$$

$$\text{At } f = \tfrac{1}{2}f_1\text{: } \frac{f_1}{f} = 2 \text{ and } -20\log_{10} 2 \cong -6 \text{ dB}$$

$$\text{At } f = \tfrac{1}{4}f_1\text{: } \frac{f_1}{f} = 4 \text{ and } -20\log_{10} 4 \cong -12 \text{ dB}$$

$$\text{At } f = \tfrac{1}{10}f_1\text{: } \frac{f_1}{f} = 10 \text{ and } -20\log_{10} 10 = -20 \text{ dB}$$

A plot of these points is indicated in Fig. 9.13 from $0.1f_1$ to f_1. Note that this results in a straight line when plotted against a log scale. In the same figure, a straight line is also drawn for the condition of 0 dB for $f \gg f_1$. As stated earlier, the straight-line segments (asymptotes) are only accurate for 0 dB when $f \gg f_1$ and the sloped line when $f_1 \gg f$. We know,

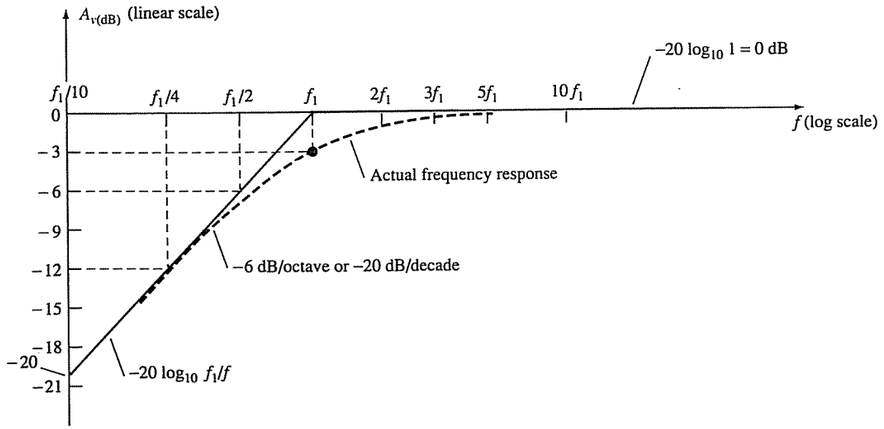


FIG. 9.13
Bode plot for the low-frequency region.

however, that when $f = f_1$, there is a 3-dB drop from the mid-band level. Employing this information in association with the straight-line segments permits a fairly accurate plot of the frequency response as indicated in the same figure.

The piecewise linear plot of the asymptotes and associated breakpoints is called a* Bode plot *of the magnitude versus frequency.

The calculations above and the curve itself demonstrate clearly that:

A change in frequency by a factor of two, equivalent to one octave, results in a 6-dB change in the ratio, as shown by the change in gain from $f_1/2$ to f_1.

As noted by the change in gain from $f_1/2$ to f_1:

For a 10:1 change in frequency, equivalent to one decade, there is a 20-dB change in the ratio, as demonstrated between the frequencies of $f_1/10$ and f_1.

Therefore, a decibel plot can easily be obtained for a function having the format of Eq. (9.24). First, simply find f_1 from the circuit parameters and then sketch two asymptotes—one along the 0-dB line and the other drawn through f_1 sloped at 6 dB/octave or 20 dB/decade. Then, find the 3-dB point corresponding to f_1 and sketch the curve.

EXAMPLE 9.8 For the network of Fig. 9.14:

a. Determine the break frequency.
b. Sketch the asymptotes and locate the −3-dB point.
c. Sketch the frequency response curve.



Solution:

a. $f_1 = \dfrac{1}{2\pi RC} = \dfrac{1}{(6.28)(5\times10^3\,\Omega)(0.1\times10^{-6}\,\text{F})}$

$\cong$ **318.5 Hz**

b. and c. See Fig. 9.15.

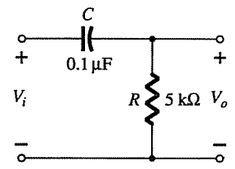


FIG. 9.14
Example 9.8.

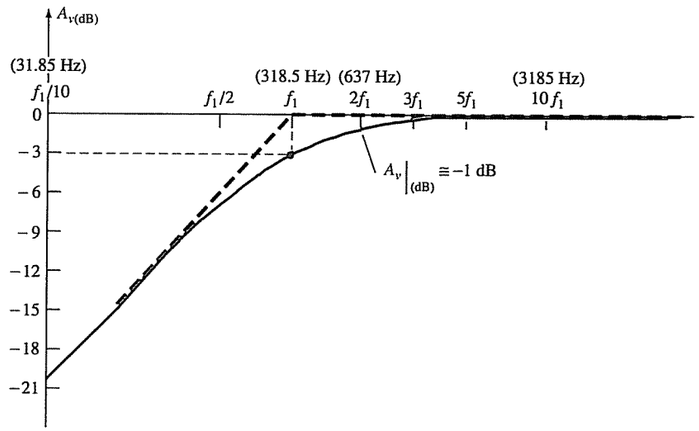


FIG. 9.15
Frequency response for the RC circuit of Fig. 9.14.

Mathcad

Mathcad will now be used to obtain a plot of the dB gain for Example 9.8 using Eq. (9.23) without using the approximations introduced in the development of Eq. (9.24). In other words, the response obtained will be a point-to-point plot of the gain equation.

Using Mathcad, the first step is to set up a range for the horizontal variable, frequency (f). This is done by first typing **f** followed by **Shift:** to obtain the colon and equal sign appearing in Fig. 9.16. Next, in an attempt to match the curve of Fig. 9.15, the starting frequency is chosen as 10 Hz as also indicated on Fig. 9.16. Then a range is defined by selecting the semicolon key to obtain the two sequential dots that follow the 10. Finally, the upper limit of 10 kHz is selected with 1 followed by an * for multiplication and the 10 to the fourth power using the ^ key and the number **4.** The range of the variable f has now been defined for the equation to follow.

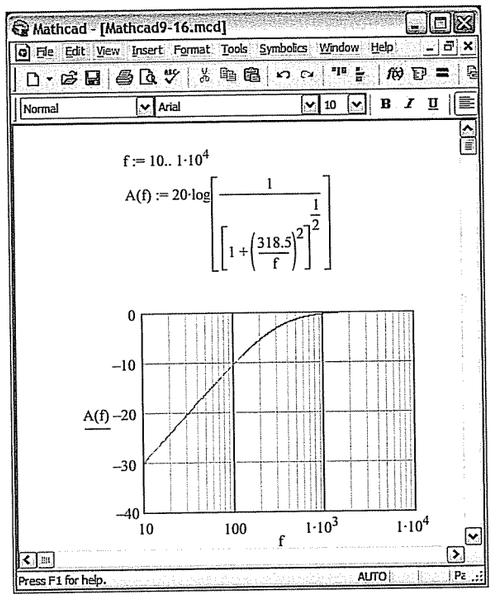


FIG. 9.16
Plot of dB gain for Example 9.8 using Mathcad.

Using the capital letter **A** to represent amplification (gain), the variable against which the gain is to be determined **must** be defined by (f). Forgetting to add the (f) will result in a meaningless response. Next the equation must be entered, paying particular attention to the location of the **placeholders.** A **placeholder** can be moved using the left or right **directional** keys (← →). In addition, you can move backward through an equation using the **backspace** key; but remember that as you backspace, the quantity to the left of the vertical component of the **placeholder** is lost—not so with the directional keys. The **spacebar** will also permit some backward motion through the equation.

Now we have to generate the desired plot. First position the crosshair in the area in which you want to generate the plot. Then type in **A(f)** and select **Insert-Graph-X-Y Plot** or **View-Toolbars-Graph** to obtain the **Graph palette** on which **X-Y Plot Shift + 2** can be chosen. The result is a frame for the graph that has some solid squares at various points around the frame. Type **A(f)** at the location of the solid black square at the middle of the vertical line and **f** at the solid black square at the center of the horizontal line to define the variables to be plotted on each axis. Then simply click anywhere on the screen outside the defined area, and the plot will appear with a scaling chosen by Mathcad.

To change the horizontal axis to a log scale, first click anywhere on the graph to create the rectangular enclosure around the plot. Then use the sequence **Format-Graph-X-Y Plot** to obtain the **Setting Default Formats for X-Y Plots** dialog box. Choose **X-Y Axes** followed by **X-Axes-Log Scale** to set the log scale and **Grid Lines** to clearly show the log scale. After choosing **OK,** the plot of Fig. 9.16 will result.

Note that the results of Example 9.8 are verified by the intersection of the −3-dB level and $f = f_1 = 318.5$ Hz. In addition, note how closely the −20-dB level corresponds with $f = f_1/10 = 31.85$ Hz on Fig. 9.15. The results certainly verify the approximations applied to obtain a quick response with a minimum of mathematical difficulty.

The gain at any frequency can be determined from the frequency plot in the following manner:

$$A_{v(\text{dB})} = 20 \log_{10} \frac{V_o}{V_i}$$

but

$$\frac{A_{v(\text{dB})}}{20} = \log_{10} \frac{V_o}{V_i}$$

and

$$\boxed{A_v = \frac{V_o}{V_i} = 10^{A_v(\text{dB})/20}} \qquad \textbf{(9.25)}$$

For example, if $A_{v(\text{dB})} = -3$ dB,

$$A_v = \frac{V_o}{V_i} = 10^{(-3/20)} = 10^{(-0.15)} \cong 0.707 \qquad \text{as expected}$$

The quantity $10^{-0.15}$ is determined using the 10^x function found on most scientific calculators.

From Fig. 9.15, $A_{v(\text{dB})} \cong -1$ dB at $f = 2f_1 = 637$ Hz. The gain at this point is

$$A_v = \frac{V_o}{V_i} = 10^{A_{v(\text{dB})}/20} = 10^{(-1/20)} = 10^{(-0.05)} = 0.891$$

and

$$V_o = 0.891 V_i$$

or V_o is 89.1% of V_i at $f = 637$ Hz.

The phase angle of θ is determined from

$$\boxed{\theta = \tan^{-1} \frac{f_1}{f}} \qquad \textbf{(9.26)}$$

from Eq. (9.22).

For frequencies $f \ll f_1$,

$$\theta = \tan^{-1} \frac{f_1}{f} \rightarrow 90°$$

For instance, if $f_1 = 100f$,

$$\theta = \tan^{-1} \frac{f_1}{f} = \tan^{-1}(100) = 89.4°$$

For $f = f_1$,

$$\theta = \tan^{-1} \frac{f_1}{f} = \tan^{-1} 1 = 45°$$

For $f \gg f_1$,

$$\theta = \tan^{-1} \frac{f_1}{f} \rightarrow 0°$$

For instance, if $f = 100f_1$,

$$\theta = \tan^{-1} \frac{f_1}{f} = \tan^{-1} 0.01 = 0.573°$$

A plot of $\theta = \tan^{-1}(f_1/f)$ is provided in Fig. 9.17. If we add the additional 180° phase shift introduced by an amplifier, the phase plot of Fig. 9.8 is obtained. The magnitude and phase response for an *RC* combination have now been established. In Section 9.6, each capacitor of importance in the low-frequency region will be redrawn in an *RC* format and the cutoff frequency for each determined to establish the low-frequency response for the BJT amplifier.

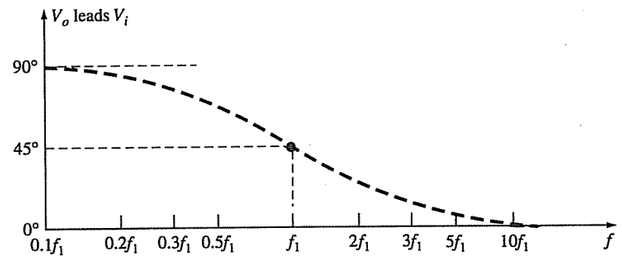


FIG. 9.17
Phase response for the RC circuit of Fig. 9.9.

9.6 LOW-FREQUENCY RESPONSE—BJT AMPLIFIER

The analysis of this section will employ the loaded voltage-divider BJT bias configuration, but the results can be applied to any BJT configuration. It will simply be necessary to find the appropriate equivalent resistance for the *RC* combination. For the network of Fig. 9.18, the capacitors C_s, C_C, and C_E will determine the low-frequency response. We will now examine the impact of each independently in the order listed.

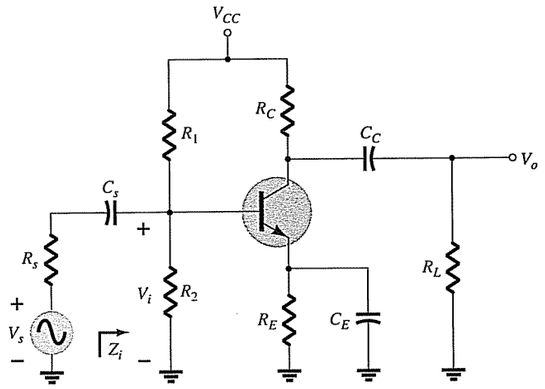


FIG. 9.18
Loaded BJT amplifier with capacitors that affect the low-frequency response.

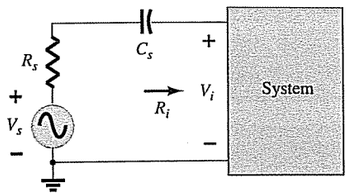


FIG. 9.19
Determining the effect of C_s on the low-frequency response.

C_s Since C_s is normally connected between the applied source and the active device, the general form of the *RC* configuration is established by the network of Fig. 9.19. The total resistance is now and the cutoff frequency as established in Section 9.5 is

$$f_{L_s} = \frac{1}{2\pi(R_s + R_i)C_s} \tag{9.27}$$

At mid or high frequencies, the reactance of the capacitor will be sufficiently small to permit a short-circuit approximation for the element. The voltage V_i will then be related to V_s by

$$V_i|_{\text{mid}} = \frac{R_i V_s}{R_i + R_s} \tag{9.28}$$

At f_{L_s}, the voltage V_i will be 70.7% of the value determined by Eq. (9.28), assuming that C_s is the only capacitive element controlling the low-frequency response.

For the network of Fig. 9.18, when we analyze the effects of C_s we must make the assumption that C_E and C_C are performing their designed function or the analysis becomes too unwieldy, that is, that the magnitudes of the reactances of C_E and C_C permit employing a short-circuit equivalent in comparison to the magnitude of the other series impedances. Using this hypothesis, the ac equivalent network for the input section of Fig. 9.18 will appear as shown in Fig. 9.20.

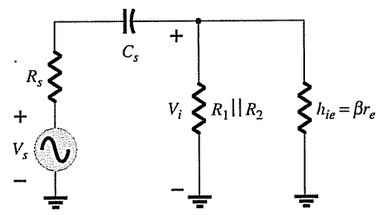


FIG. 9.20
Localized ac equivalent for C_s.

The value of R_i for Eq. (9.27) is determined by

$$R_i = R_1 \| R_2 \| \beta r_e \tag{9.29}$$

The voltage $\mathbf{V}_i$ applied to the input of the active device can be calculated using the voltage-divider rule:

$$\mathbf{V}_i = \frac{R_i \mathbf{V}_s}{R_s + R_i - jX_{C_s}} \tag{9.30}$$

C_C Since the coupling capacitor is normally connected between the output of the active device and the applied load, the *RC* configuration that determines the low-cutoff frequency due to C_C appears in Fig. 9.21. From Fig. 9.21, the total series resistance is now $R_o + R_L$, and the cutoff frequency due to C_C is determined by

$$f_{L_C} = \frac{1}{2\pi(R_o + R_L)C_C} \tag{9.31}$$

Ignoring the effects of C_s and C_E, we have that the output voltage V_o will be 70.7% of its midband value at f_{L_C}. For the network of Fig. 9.18, the ac equivalent network for the output section with $V_i = 0$ V appears in Fig. 9.22. The resulting value for R_o in Eq. (9.31) is then simply

$$R_o = R_C \| r_o \tag{9.32}$$

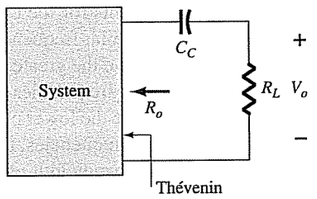


FIG. 9.21
Determining the effect of C_C on the low-frequency response.

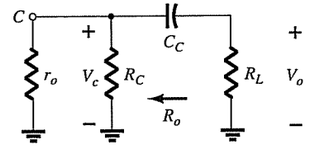


FIG. 9.22
Localized ac equivalent for C_C with $V_i = 0$ V.

C_E To determine f_{L_E}, the network "seen" by C_E must be determined as shown in Fig. 9.23. Once the level of R_e is established, the cutoff frequency due to C_E can be determined using the following equation:

$$f_{L_E} = \frac{1}{2\pi R_e C_E} \tag{9.33}$$

For the network of Fig. 9.18, the ac equivalent as "seen" by C_E appears in Fig. 9.24. The value of R_e is therefore determined by

$$R_e = R_E \| \left(\frac{R_s'}{\beta} + r_e \right) \tag{9.34}$$

where $R_s' = R_s \| R_1 \| R_2$.

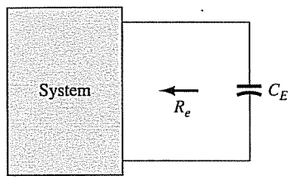


FIG. 9.23
Determining the effect of C_E on the low-frequency response.

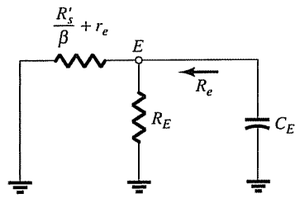


FIG. 9.24
Localized ac equivalent of C_E.

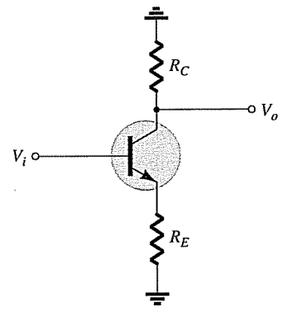


FIG. 9.25
Network employed to describe the effect of C_E on the amplifier gain.

The effect of C_E on the gain is best described in a quantitative manner by recalling that the gain for the configuration of Fig. 9.25 is given by

$$A_v = \frac{-R_C}{r_e + R_E}$$

The maximum gain is obviously available where R_E is 0 Ω. At low frequencies, with the bypass capacitor C_E in its "open-circuit" equivalent state, all of R_E appears in the gain equation above, resulting in the minimum gain. As the frequency increases, the reactance of the capacitor C_E will decrease, reducing the parallel impedance of R_E and C_E until the resistor R_E is effectively "shorted out" by C_E. The result is a maximum or midband gain determined by $A_v = -R_C/r_e$. At f_{L_E} the gain will be 3 dB below the midband value determined with R_E "shorted out."

Before continuing, keep in mind that C_s, C_C, and C_E will affect only the low-frequency response. At the midband frequency level, the short-circuit equivalents for the capacitors can be inserted. Although each will affect the gain $A_v = V_o/V_i$ in a similar frequency range, the highest low-frequency cutoff determined by C_s, C_C, or C_E will have the greatest impact since it will be the last encountered before the midband level. If the frequencies are relatively far apart, the highest cutoff frequency will essentially determine the lower cutoff frequency for the entire system. If there are two or more "high" cutoff frequencies, the effect will be to raise the lower cutoff frequency and reduce the resulting bandwidth of the system. In other words, there is an interaction between capacitive elements that can affect the resulting low-cutoff frequency. However, if the cutoff frequencies established by each capacitor are sufficiently separated, the effect of one on the other can be ignored with a high degree of accuracy—a fact that will be demonstrated by the printouts to appear in the following example.

EXAMPLE 9.9



a. Determine the lower cutoff frequency for the network of Fig. 9.18 using the following parameters:
$C_s = 10\ \mu\text{F}$, $C_E = 20\ \mu\text{F}$, $C_C = 1\ \mu\text{F}$
$R_s = 1\ \text{k}\Omega$, $R_1 = 40\ \text{k}\Omega$, $R_2 = 10\ \text{k}\Omega$, $R_E = 2\ \text{k}\Omega$, $R_C = 4\ \text{k}\Omega$, $R_L = 2.2\ \text{k}\Omega$
$\beta = 100$, $r_o = \infty\Omega$, $V_{CC} = 20\ \text{V}$

b. Sketch the frequency response using a Bode plot.

Solution:

a. To determine r_e for dc conditions, we use

$$\beta R_E = (100)(2\ \text{k}\Omega) = 200\ \text{k}\Omega \gg 10R_2 = 100\ \text{k}\Omega$$

The result is

$$V_B \cong \frac{R_2 V_{CC}}{R_2 + R_1} = \frac{10\ \text{k}\Omega(20\ \text{V})}{10\ \text{k}\Omega + 40\ \text{k}\Omega} = \frac{200\ \text{V}}{50} = 4\ \text{V}$$

with

$$I_E = \frac{V_E}{R_E} = \frac{4\ \text{V} - 0.7\ \text{V}}{2\ \text{k}\Omega} = \frac{3.3\ \text{V}}{2\ \text{k}\Omega} = 1.65\ \text{mA}$$

so that

$$r_e = \frac{26\ \text{mV}}{1.65\ \text{mA}} \cong \mathbf{15.76\ \Omega}$$

and

$$\beta r_e = 100(15.76\ \Omega) = 1576\ \Omega = \mathbf{1.576\ k\Omega}$$

Midband Gain

$$A_v = \frac{V_o}{V_i} = \frac{-R_C \| R_L}{r_e} = -\frac{(4\ \text{k}\Omega) \| (2.2\ \text{k}\Omega)}{15.76\ \Omega} \cong -90$$

The input impedance is given by

$$Z_i = R_i = R_1 \| R_2 \| \beta r_e$$
$$= 40\ \text{k}\Omega \| 10\ \text{k}\Omega \| 1.576\ \text{k}\Omega$$
$$\cong 1.32\ \text{k}\Omega$$

and from Fig. 9.26,

$$V_i = \frac{R_i V_s}{R_i + R_s}$$

or

$$\frac{V_i}{V_s} = \frac{R_i}{R_i + R_s} = \frac{1.32\ \text{k}\Omega}{1.32\ \text{k}\Omega + 1\ \text{k}\Omega} = 0.569$$

so that

$$A_{v_s} = \frac{V_o}{V_s} = \frac{V_o}{V_i} \cdot \frac{V_i}{V_s} = (-90)(0.569)$$
$$= \mathbf{-51.21}$$

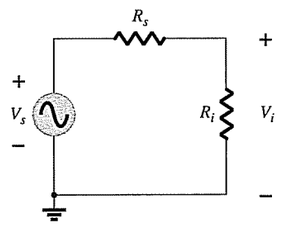


FIG. 9.26
Determining the effect of R_s on the gain A_{v_s}.

C_s

$$R_i = R_1 \| R_2 \| \beta r_e = 40\ \text{k}\Omega \| 10\ \text{k}\Omega \| 1.576\ \text{k}\Omega \cong 1.32\ \text{k}\Omega$$

$$f_{L_s} = \frac{1}{2\pi(R_s + R_i)C_s} = \frac{1}{(6.28)(1\ \text{k}\Omega + 1.32\ \text{k}\Omega)(10\ \mu\text{F})}$$

$$f_{L_s} \cong \mathbf{6.86\ Hz}$$

PSpice Analysis

The results just obtained will now be verified using PSpice Windows. The network with its various capacitors appears in Fig. 9.27. The sequence **Edit-PSpice Model** was used to set I_s to 2E-15A and beta to 100. The remaining parameters of the **PSpice Model** for the transistor were removed to idealize the response to the greatest degree possible. In the **Simulation Settings** dialog box **AC Sweep/Noise** was selected under the **Analysis type** heading, and **Linear** was chosen under the **AC Sweep Type.** The **Start Frequency** was set at 10 kHz, the **End Frequency** at 10 kHz, and the number of **Points** at 1. A **Simulation** resulted in the dc bias voltage levels of Fig. 9.27. Note that V_B is 3.875 V, compared to the calculated level of 4 V, and that V_E is 3.166 V, compared to the calculated level of 3.3 V. These values are very close when you consider that the approximate model was used to represent the transistor. The output file reveals that the ac voltage across the load at a frequency of 10 kHz is 49.67 mV, resulting in a gain of 49.67, which is very close to the calculated level of 51.21

A plot of the gain versus frequency will now be obtained with only C_s as a determining factor. The other capacitors, C_C and C_E, will be set to very high values, so they are essentially short circuits at any of the frequencies of interest. Setting C_C and C_E to 1 F will remove any effect they might have on the response in the low-frequency region. Here, however, one must be careful because the program does not recognize 1 F as one farad. It must be entered as 1E6uF. Since the plot desired is gain versus frequency, we must set the **Simulation** to run through a range of frequencies, not as in the first **Simulation** where the frequency was fixed at 10 kHz. This is accomplished by first selecting the **New Simulation key**, giving the run a new **Name,** and proceeding to the **Simulation Settings** dialog box. Under **Analysis type, AC Sweep/Noise** is selected, and under **AC Sweep Type, Linear** is chosen, followed by a **Start Frequency** of 1 Hz, an **End Frequency** of 100 Hz, and **Points** set at 1000. The **Start Frequency** is set at 1 Hz because 0 Hz is an invalid entry. If one is really concerned about what happens between 0 Hz and 1 Hz, one could choose the start frequency as 0.001 Hz and work from there. However, 1 Hz is only 1/100 of the full scale and will be fine for this analysis. The **End Frequency** was selected as 100 Hz because we limit our interest to the low-frequency range. With 1000 points there will be sufficient data points to provide a smooth plot throughout the frequency range. Once **Simulation** is enacted followed by **Trace-Add Trace-V(RL:1)**, a plot appears extending to 120 Hz. Note also that the computer selected a log scale even though we called for a **Linear** plot. If we choose **Plot-Axis Settings-X-Axis-Linear,** we get a linear plot to 120 Hz, but the curve of interest is in the low end—the log axis obviously provided a better plot for our region of interest. Returning to **Plot-Axis Settings-X-Axis-Log**

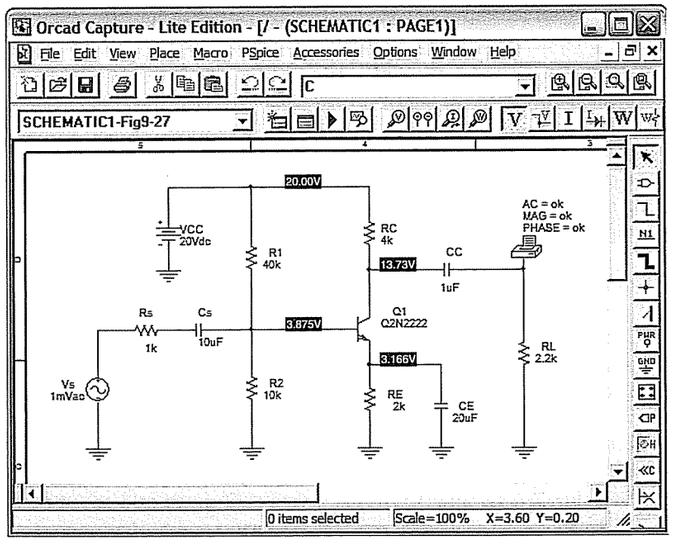


FIG. 9.27
Network of Fig. 9.18 with assigned values.

returns the original plot. Our interest lies in the region of 1 Hz to 100 Hz, so the remaining frequencies to 1 kHz should be removed with **Plot-Axis Settings-User Defined-1 Hz to 100 Hz-OK.** The vertical axis also goes to 60 mV, and we want to limit the range to 50 mV for this frequency range. This is accomplished through **Plot-Axis Settings-Y-Axis User Defined-0V to 50 mV-OK,** after which the plot of Fig. 9.28 will be obtained.

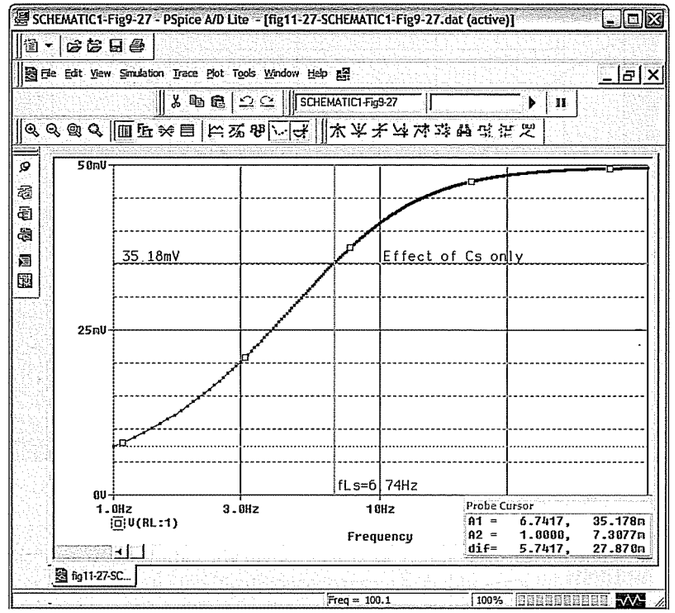


FIG. 9.28
Low-frequency response due to C_s.

Note how closely the curve approaches 50 mV in this range. The cutoff level is determined by 0.707(49.67 mV) = 35.12 mV, which can be found using the **Cursor** option. Going to **Trace-Cursor** results in intersecting lines whose horizontal and vertical values at the intersection appear in the **Probe Cursor** box in the bottom right of the plot. Moving the cursor (**A1**) along the curve until we are as close to the 35.12-mV level as possible results in the intersection shown in Fig. 9.28 at 35.178 mV. Note that the corresponding frequency is 6.7417 Hz, which corresponds very closely to the predicted value of 6.86 Hz. **A2** was placed at 1 Hz to obtain a level of 7.3077 mV. The labels were added using the **Tools-Label-Text** option.

C_C

$$f_{L_C} = \frac{1}{2\pi(R_C + R_L)C_C}$$
$$= \frac{1}{(6.28)(4\,\text{k}\Omega + 2.2\,\text{k}\Omega)(1\,\mu\text{F})}$$
$$\cong \mathbf{25.68\ Hz}$$

PSpice Analysis

To investigate the effects of C_C on the lower cutoff frequency, both C_S and C_E must be set to 1 F as described above. Following the procedure outlined above results in the plot of Fig. 9.29, with a cutoff frequency of 25.68 Hz, providing an exact match with the calculated level of 25.68 Hz.

C_E

$$R'_s = R_s \| R_1 \| R_2 = 1\,\text{k}\Omega \| 40\,\text{k}\Omega \| 10\,\text{k}\Omega \cong 0.889\,\text{k}\Omega$$
$$R_e = R_E \left\| \left(\frac{R'_s}{\beta} + r_e \right) = 2\,\text{k}\Omega \right\| \left(\frac{0.889\,\text{k}\Omega}{100} + 15.76\,\Omega \right)$$
$$= 2\,\text{k}\Omega \| (8.89\,\Omega + 15.76\,\Omega) = 2\,\text{k}\Omega \| 24.65\,\Omega \cong 24.35\,\Omega$$
$$f_{L_E} = \frac{1}{2\pi R_e C_E} = \frac{1}{(6.28)(24.35\,\Omega)(20\,\mu\text{F})} = \frac{10^6}{3058.36} \cong \mathbf{327\ Hz}$$

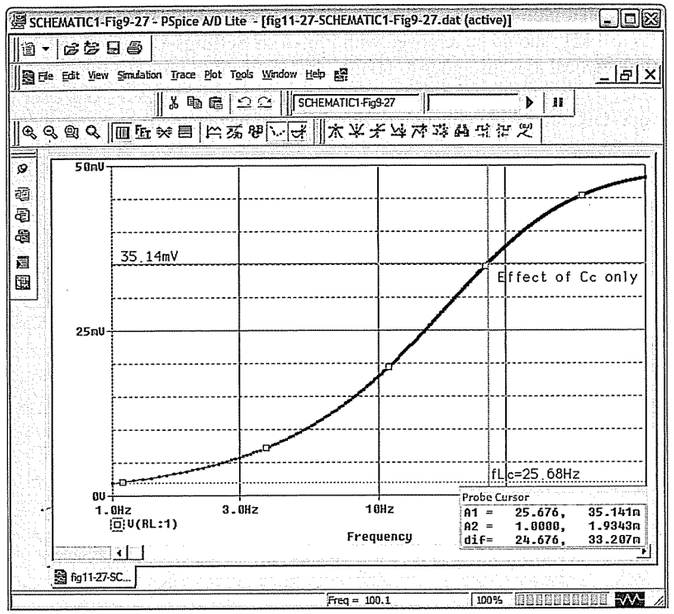


FIG. 9.29
Low-frequency response to C_C.

PSpice Analysis

The effect of C_E can be examined using PSpice Windows by setting both C_s and C_C to 1 F. In addition, since the frequency range is greater, the start frequency has to be changed to 10 Hz and the final frequency to 1 kHz. The result is the plot of Fig. 9.30, with a cutoff frequency of 321.37 Hz, providing a close match with the calculated value of 327 Hz.

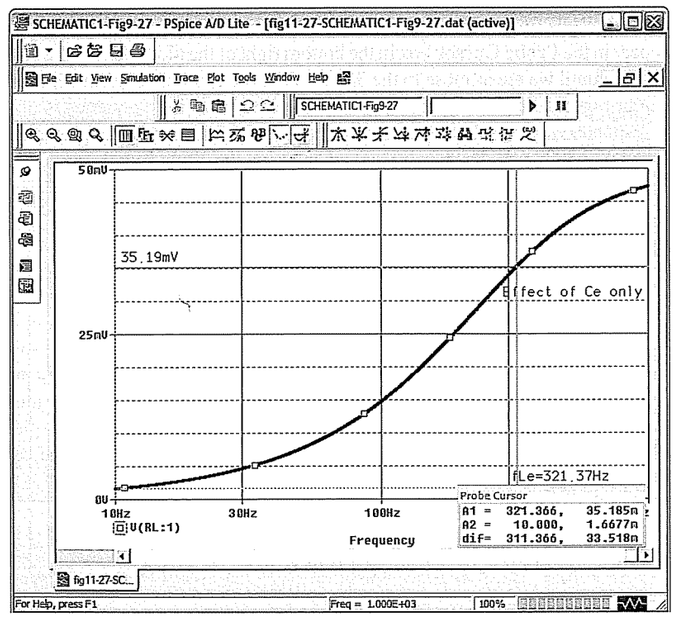


FIG. 9.30
Low-frequency response due to C_E.

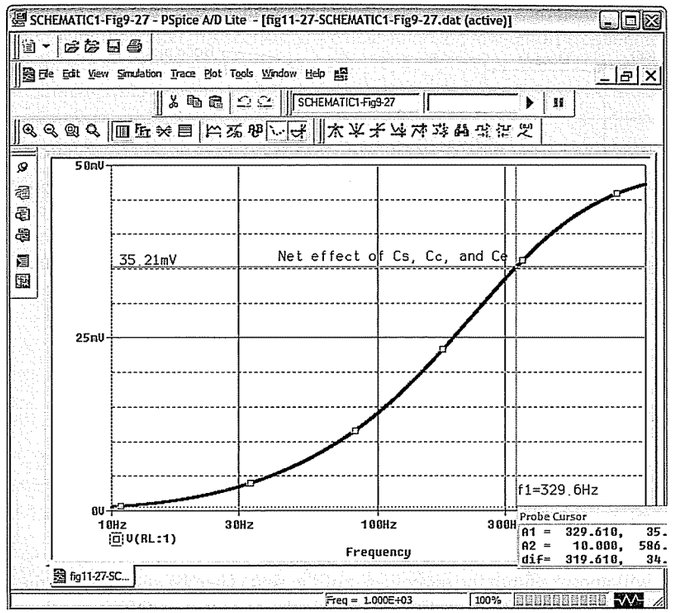


FIG. 9.31
Low-frequency response due to C_S, C_E, and C_C.

The fact that f_{L_E} is significantly higher than f_{L_S} or f_{L_C} suggests that it will be the predominant factor in determining the low-frequency response for the complete system. To test the accuracy of our hypothesis, the network is simulated with all the initial values of capacitance level to obtain the results of Fig. 9.31. Note the strong similarity with the waveform of Fig. 9.30, with the only visible difference being the higher gain at lower frequencies on Fig. 9.30. Without question, the plot supports the fact that the highest of the low cutoff frequencies will have the most impact on the low cutoff frequency for the system.

(b) It was mentioned earlier that dB plots are usually normalized by dividing the voltage gain A_v by the magnitude of the midband gain. For Fig. 9.18, the magnitude of the midband gain is 51.21, and naturally the ratio $|A_v/A_{v_{mid}}|$ will be 1 in the midband region. The result is a 0-dB asymptote in the midband region as shown in Fig. 9.32. Defining f_{L_E} as our lower cutoff frequency f_1, we can draw an asymptote at -6 dB/octave as shown in Fig. 9.32 to form the Bode plot and our envelope for the actual response. At f_1, the actual curve is -3 dB down from the midband level as defined by the $0.707A_{v_{mid}}$ level, permitting a sketch of the actual frequency response curve as shown in Fig. 9.32. A -6-dB/octave asymptote was drawn at each frequency defined in the analysis above to demonstrate clearly that it is f_{L_E} for this network that will determine the -3-dB point. It is not until about -24 dB that f_{L_C} begins to affect the shape of the envelope. The magnitude plot shows that the slope of the resultant asymptote is the sum of the asymptotes having the same sloping direction in the same frequency interval. Note in Fig. 9.32 that the slope has dropped to -12 dB/octave for frequencies less than f_{L_C} and could drop to -18 dB/octave if the three defined cutoff frequencies of Fig. 9.32 were closer together.

PSpice Analysis

A dB plot of the low-frequency response can be obtained by creating a **Simulation** for the frequency range and then, when the **Add Traces** dialog box appears, creating the desired **Trace Expression** using the provided listings. For a plot of $20 \log_{10}|A_v/A_{v_{mid}}|$ the ratio $A_v/A_{v_{mid}}$ can also be written as $(V_o/V_i)/(V_{o_{mid}}/V_i) = V_o/V_{o_{mid}}$, resulting in the following expression for the dB gain:

$$20 \log_{10}|A_v/A_{v_{mid}}| = 20 \log_{10}|V_o/V_{o_{mid}}| = \text{dB}(V_o/V_{o_{mid}}) = \text{dB}(V_{R_L}/49.7\,\text{mV})$$

The **Trace Expression** can be created by first selecting **DB** from the **Function** list and then selecting **V(RL:1)** from the **Simulation Output Variable** list. Note that the second

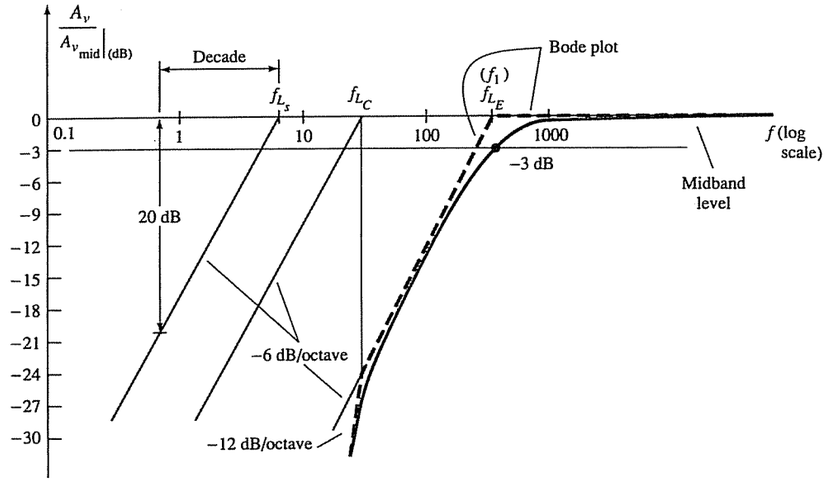


FIG. 9.32
Low-frequency plot for the network of Example 9.9.

selection will appear within the parentheses of the first. Then be sure to enter the division sign and the number 0.0497 V = 49.7 mV within the parentheses. Of course, the entire expression can be written directly if you prefer not to use the listings. Once the expression is properly written, select **OK** and the plot of Fig. 9.33 will result. The plot clearly reveals the change in slope of the asymptote at f_{L_C} and how the actual curve follows the envelope created by the Bode plot. In addition, note the 3-dB drop at f_1.

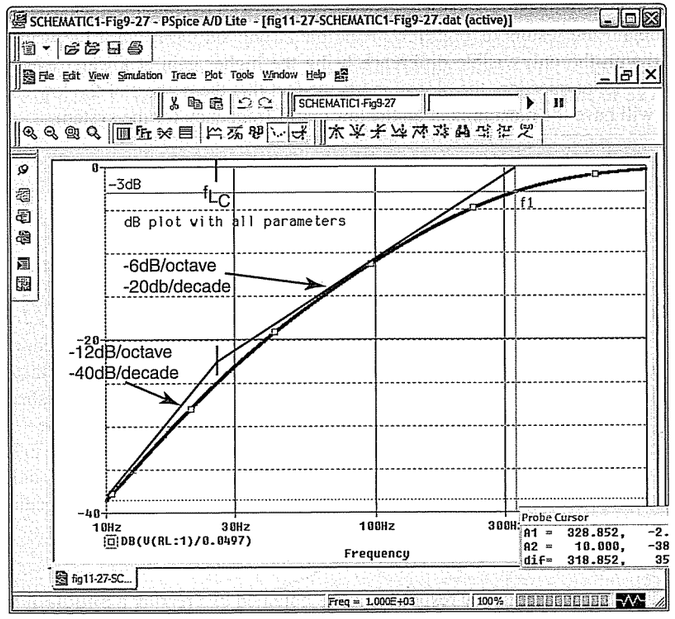


FIG. 9.33
dB plot of the low-frequency response of the BJT amplifier of Fig. 9.27.

Keep in mind as we proceed to the next section that the analysis of this section is not limited to the network of Fig. 9.18. For any transistor configuration it is simply necessary to isolate each *RC* combination formed by a capacitive element and determine the break frequencies. The resulting frequencies will then determine whether there is a strong interaction between capacitive elements in determining the overall response and which element will have the greatest effect on establishing the lower cutoff frequency. In fact, the analysis of the next section will parallel this section as we determine the low-cutoff frequencies for the FET amplifier.

9.7 LOW-FREQUENCY RESPONSE—FET AMPLIFIER

The analysis of the FET amplifier in the low-frequency region will be quite similar to that of the BJT amplifier of Section 9.6. There are again three capacitors of primary concern as appearing in the network of Fig. 9.34: C_G, C_C, and C_S. Although Fig. 9.34 will be used to establish the fundamental equations, the procedure and conclusions can be applied to most FET configurations.

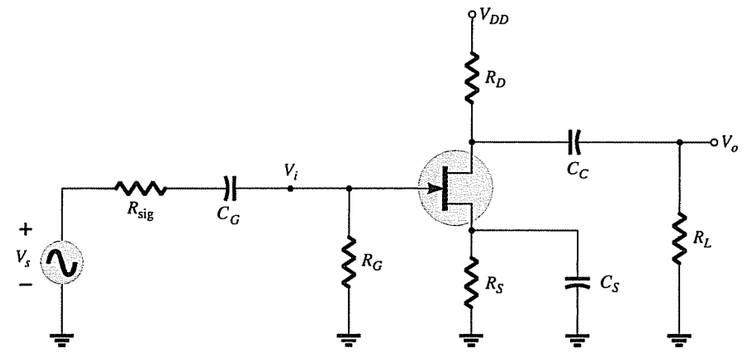


FIG. 9.34
Capacitive elements that affect the low-frequency response of a JFET amplifier.

C_G For the coupling capacitor between the source and the active device, the ac equivalent network is as shown in Fig. 9.35. The cutoff frequency determined by C_G is

$$f_{L_G} = \frac{1}{2\pi(R_{sig} + R_i)C_G} \tag{9.35}$$

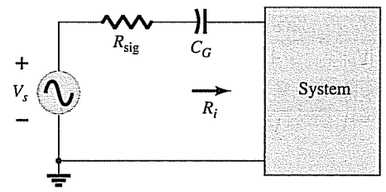


FIG. 9.35
Determining the effect of C_G *on the low-frequency response.*

which is an exact match of Eq. (9.27). For the network of Fig. 9.34,

$$R_i = R_G \tag{9.36}$$

Typically, $R_G \gg R_{sig}$, and the lower cutoff frequency is determined primarily by R_G and C_G. The fact that R_G is so large permits a relatively low level of C_G while maintaining a low cutoff frequency level for f_{L_G}.

C_C For the coupling capacitor between the active device and the load the network of Fig. 9.36 results, which is also an exact match of Fig. 9.21. The resulting cutoff frequency is

$$f_{L_C} = \frac{1}{2\pi(R_o + R_L)C_C} \tag{9.37}$$

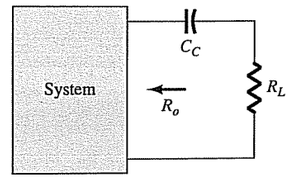


FIG. 9.36
Determining the effect of C_C *on the low-frequency response.*

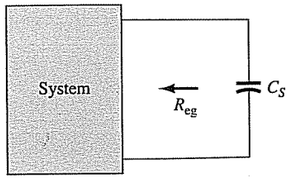


FIG. 9.37
Determining the effect of C_S on the low-frequency response.

For the network of Fig. 9.34,

$$R_o = R_D \| r_d \tag{9.38}$$

C_S For the source capacitor C_S, the resistance level of importance is defined by Fig. 9.37. The cutoff frequency is defined by

$$f_{L_s} = \frac{1}{2\pi R_{eq} C_S} \tag{9.39}$$

For Fig. 9.34, the resulting value of R_{eq} is

$$R_{eq} = \frac{R_S}{1 + R_S(1 + g_m r_d)/(r_d + R_D \| R_L)} \tag{9.40}$$

which for $r_d \cong \infty\,\Omega$ becomes

$$R_{eq} = R_S \| \frac{1}{g_m} \tag{9.41}$$


PSpice

EXAMPLE 9.10

a. Determine the lower cutoff frequency for the network of Fig. 9.34 using the following parameters:

$C_G = 0.01\,\mu F, \quad C_C = 0.5\,\mu F, \quad C_S = 2\,\mu F$

$R_{sig} = 10\,k\Omega, \quad R_G = 1\,M\Omega, \quad R_D = 4.7\,k\Omega, \quad R_S = 1\,k\Omega, \quad R_L = 2.2\,k\Omega$

$I_{DSS} = 8\,mA, \quad V_P = -4\,V \quad r_d = \infty\,\Omega, \quad V_{DD} = 20\,V$

b. Sketch the frequency response using a Bode plot.

Solution:

a. DC analysis: Plotting the transfer curve of $I_D = I_{DSS}(1 - V_{GS}/V_P)^2$ and superimposing the curve defined by $V_{GS} = -I_D R_S$ results in an intersection at $V_{GS_Q} = -2\,V$ and $I_{D_Q} = 2\,mA$. In addition,

$$g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(8\,mA)}{4\,V} = 4\,mS$$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 4\,mS\left(1 - \frac{-2\,V}{-4\,V}\right) = 2\,mS$$

C_G Eq. (9.35): $f_{L_G} = \dfrac{1}{2\pi(10\,k\Omega + 1\,M\Omega)(0.01\,\mu F)} \cong$ **15.8 Hz**

C_C Eq. (9.37): $f_{L_C} = \dfrac{1}{2\pi(4.7\,k\Omega + 2.2\,k\Omega)(0.5\,\mu F)} \cong$ **46.13 Hz**

C_S $R_{eq} = R_S \| \dfrac{1}{g_m} = 1\,k\Omega \| \dfrac{1}{2\,mS} = 1\,k\Omega \| 0.5\,k\Omega = 333.33\,\Omega$

Eq. (9.39): $f_{L_S} = \dfrac{1}{2\pi(333.33\,\Omega)(2\,\mu F)} =$ **238.73 Hz**

Since f_{L_S} is the largest of the three cutoff frequencies, it defines the low-cutoff frequency for the network of Fig. 9.34.

b. The midband gain of the system is determined by

$$A_{v_{mid}} = \frac{V_o}{V_i} = -g_m(R_D \| R_L) = -(2\,mS)(4.7\,k\Omega \| 2.2\,k\Omega)$$

$$= -(2\,mS)(1.499\,k\Omega)$$

$$\cong -3$$

Using the midband gain to normalize the response for the network of Fig. 9.34 results in the frequency plot of Fig. 9.38.

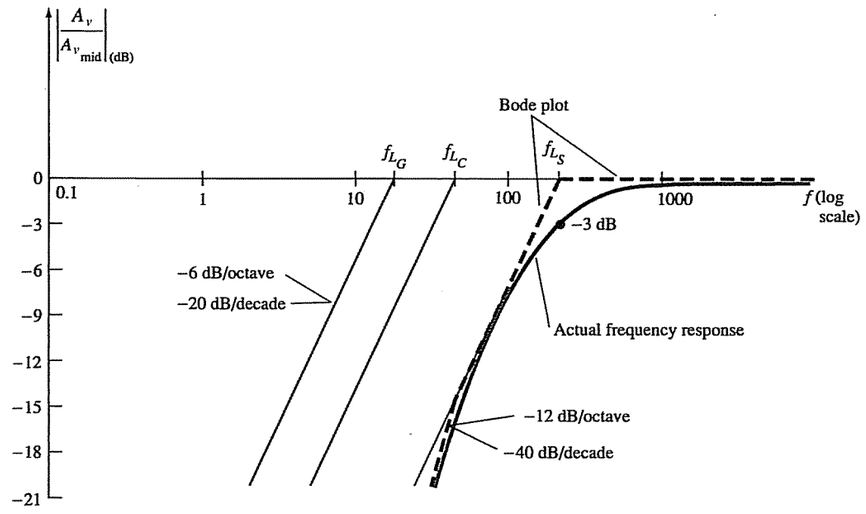


FIG. 9.38
Low-frequency response for the JFET configuration of Example 9.10.

PSpice Windows

Applying PSpice to the network of Fig. 9.34 results in the display of Fig. 9.39. The JFET parameters were set at **Beta** = 0.5 mA/V^2 and **Vto** at −4 V with all other parameters in the model listing deleted. The frequency of interest is 10 kHz. The resulting dc levels confirm that V_{GS} is −2 V with V_D at 10.60 V, which should be in the middle of the linear active region

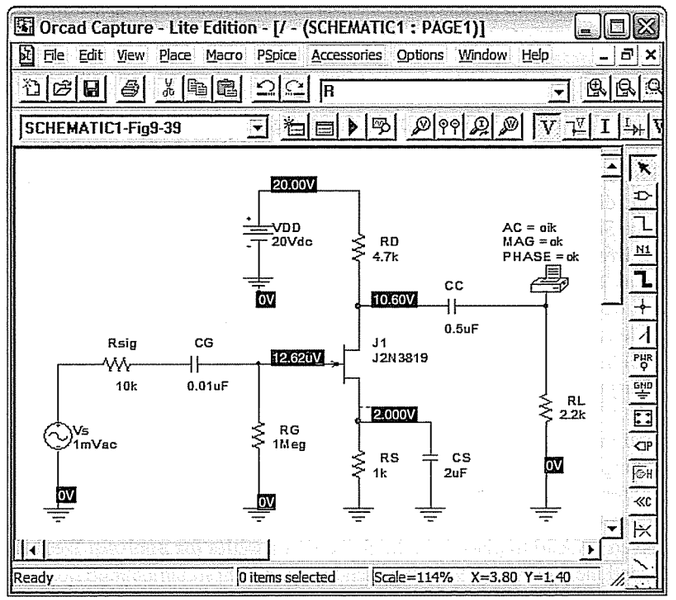


FIG. 9.39
Schematic network for Example 9.10.

since $V_{GS} = \frac{1}{2} V_D$ and $V_{DS} = \frac{1}{2} V_{DD}$. The ac response reveals that the output voltage is 2.993 mV for a gain of 2.993, which is essentially equal to the calculated gain of 3.

If we establish a **New Simulation** and set the **Analysis type** to **AC Sweep/Noise,** we can generate a plot for the low-frequency region. The **Start Frequency** is set at 10 Hz, the **End Frequency** 10 kHz, and the number of **Points** at 1000. The sequence **Simulation-Trace-Add Trace-** then permits establishing the **Trace Expression DB(V(RL:1)/2.993 mV),** which, following an **OK,** results in the plot of Fig. 9.40. The low cutoff frequency of 221.82 Hz was primarily determined by the source capacitance **CG.**

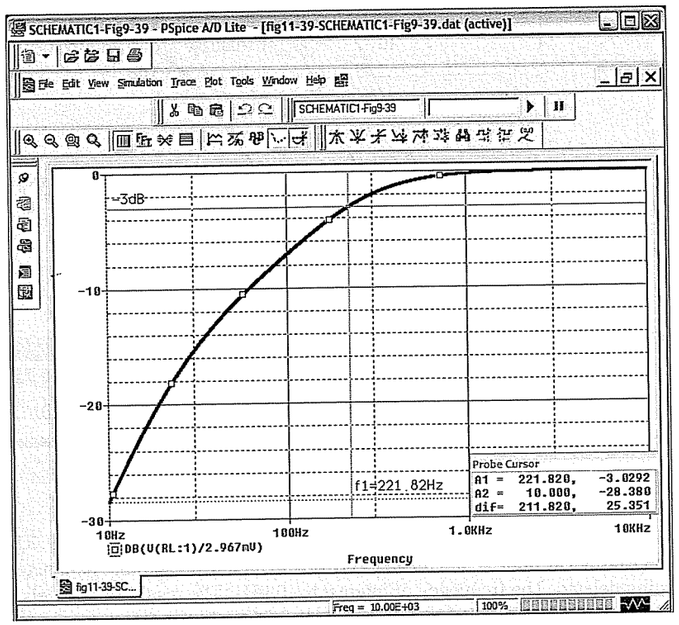


FIG. 9.40

dB response for the low-frequency region in the network of Example 9.10.

Multisim

Multisim can also provide a frequency plot of the gain and phase response of a BJT or a JFET network by first constructing the network or calling it up from storage. Since the network of Fig. 9.39 is the same as that analyzed using Multisim in Chapter 8 (Fig. 8.64), is retrieved and displayed as Fig. 9.41 with its dc levels at the drain and source terminals. Next the sequence **Simulate-Analyses-AC Analysis** is applied to obtain the **Ac Analysis** dialog box. Under **Frequency Parameters,** the **Start frequency** is selected as **10Hz** and the **Stop frequency** as **10kHz** to match the plot of Fig. 9.40. The **Sweep type** is left at the default selection of **decade,** and the **Number of points** per decade is also left at **100.** Finally, the vertical scale is set in the linear mode since it is the magnitude of the output voltage versus frequency rather than the dB gain as in Fig. 9.40.

Next, **Output variables** are selected in the dialog box. Under the heading **Variables in circuit,** select **Voltage** to reduce the number of options. Each option is defined in the listing obtained through **Reports-Netlist Report,** which lists all the components of the network. Working our way down the **Component** list until we hit **RL,** we find the **Net** listing of 24 and 0 for the resistor, indicating that is connected between nodes 24 and 0. Since we want a plot of the output voltage versus frequency, we select **$24** under **Variables in circuit,** followed by **Add** to place it in the **Selected variables for analysis.** We then choose **Simulate,** and the plot of Fig. 9.42 results.

At first, the plot may appear without a grid structure to help define the levels at each frequency. This is corrected by the sequence **View-Show/Hide Grid** as shown in Fig. 9.42. Always be aware that the red arrow along the left vertical column defines the plot under

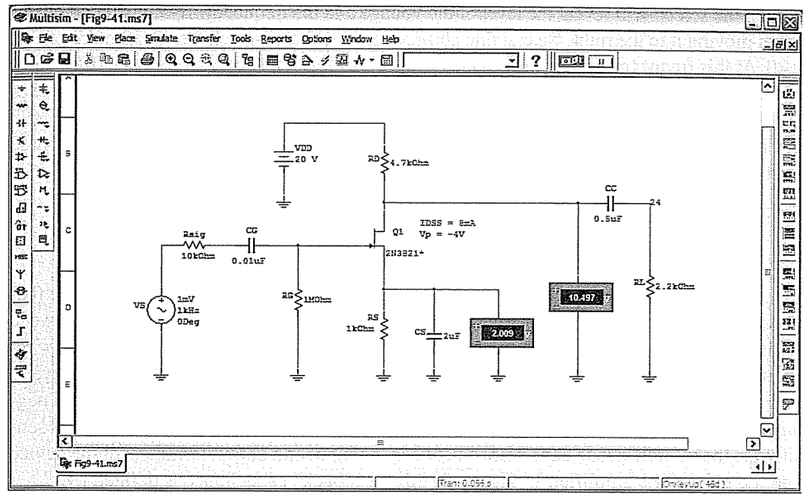


FIG. 9.41

Network of Fig. 9.34 (Example 9.10) using Multisim.

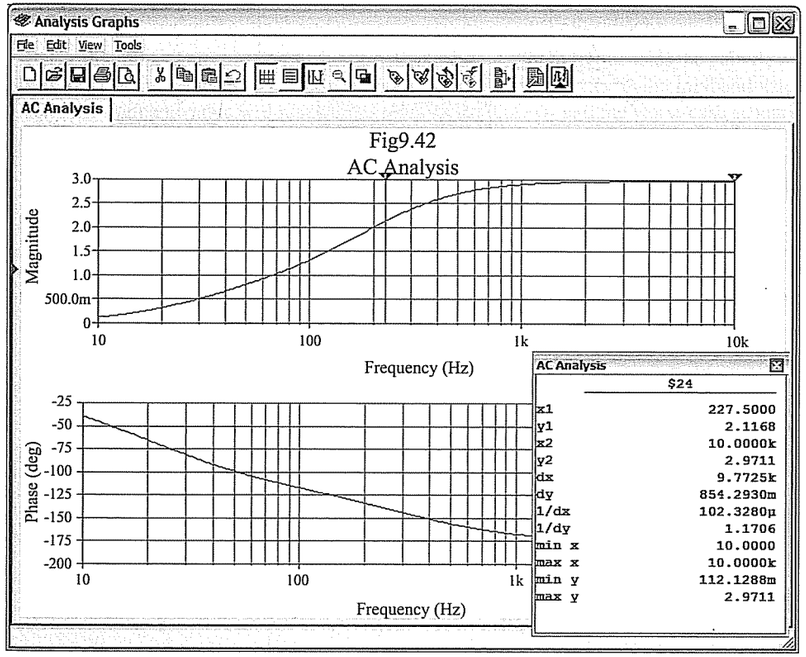


FIG. 9.42

Multisim plot for Example 9.10.

review. To add the grid to the phase plot, simply click on the lower graph at any point, and the red arrow will drop down. Then follow with the same sequence as above to establish the grid structure. If you want the graph to fill the entire screen, simply select the full-screen option at the top right corner of the **Analysis Graphs.**

Finally, cursors can be added to define the level of the plotted function at any frequency. Simply select **View-Show/Hide Cursors,** and the cursors will appear on the selected graph (which is the magnitude plot in Fig. 9.42). Then click on cursor 1, and the **AC Analysis** dialog

box on the screen will reveal the level of the voltage and the frequency. By clicking on cursor 1 and moving it to the right, we can find an **x1** value of 227.5 to match the –3-dB point of Fig. 9.40. At this frequency the output voltage (**y1**) is 2.12 V, which is very close to the 0.707 level of the 2.93 gain (actually 2.07 V) obtained in Chapter 8. Cursor 2 was moved to an **x2** value of 10 kHz to obtain a voltage of 2.97 V, which again is very close to the maximum gain of 2.93 in Chapter 8. Before leaving Fig. 9.42, note that the higher the frequency, the closer is the phase shift to 180° as the relatively large, low-frequency capacitors lose their effect.

9.8 MILLER EFFECT CAPACITANCE

In the high-frequency region, the capacitive elements of importance are the interelectrode (between-terminals) capacitances internal to the active device and the wiring capacitance between leads of the network. The large capacitors of the network that controlled the low-frequency response are all replaced by their short-circuit equivalent due to their very low reactance levels.

For *inverting* amplifiers (phase shift of 180° between input and output, resulting in a negative value for A_v), the input and output capacitance is increased by a capacitance level sensitive to the interelectrode capacitance between the input and output terminals of the device and the gain of the amplifier. In Fig. 9.43, this "feedback" capacitance is defined by C_f.

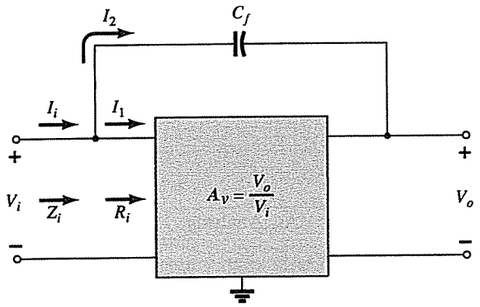


FIG. 9.43
Network employed in the derivation of an equation for the Miller input capacitance.

Applying Kirchhoff's current law gives

$$I_i = I_1 + I_2$$

Using Ohm's law yields

$$I_i = \frac{V_i}{Z_i}, \quad I_1 = \frac{V_i}{R_i}$$

and

$$I_2 = \frac{V_i - V_o}{X_{C_f}} = \frac{V_i - A_v V_i}{X_{C_f}} = \frac{(1 - A_v)V_i}{X_{C_f}}$$

Substituting, we obtain

$$\frac{V_i}{Z_i} = \frac{V_i}{R_i} + \frac{(1 - A_v)V_i}{X_{C_f}}$$

and

$$\frac{1}{Z_i} = \frac{1}{R_i} + \frac{1}{X_{C_f}/(1 - A_v)}$$

but

$$\frac{X_{C_f}}{1 - A_v} = \frac{1}{\underbrace{\omega\,(1 - A_v)C_f}_{C_M}} = X_{CM}$$

and

$$\frac{1}{Z_i} = \frac{1}{R_i} + \frac{1}{X_{C_M}}$$

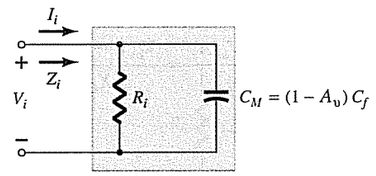


FIG. 9.44
Demonstrating the effect of the Miller effect capacitance.

establishing the equivalent network of Fig. 9.44. The result is an equivalent input impedance to the amplifier of Fig. 9.43 that includes the same R_i that we dealt with in previous chapters, with the addition of a feedback capacitor magnified by the gain of the amplifier. Any interelectrode capacitance at the input terminals to the amplifier will simply be added in parallel with the elements of Fig. 9.44.

In general, therefore, the Miller effect input capacitance is defined by

$$\boxed{C_{M_i} = (1 - A_v)C_f} \qquad \textbf{(9.42)}$$

This shows us that:

For any inverting amplifier, the input capacitance will be increased by a Miller effect capacitance sensitive to the gain of the amplifier and the interelectrode (parasitic) capacitance between the input and output terminals of the active device.

The dilemma of an equation such as Eq. (9.42) is that at high frequencies the gain A_v will be a function of the level of C_{M_i}. However, since the maximum gain is the midband value, using the midband value will result in the highest level of C_{M_i} and the worst-case scenario. In general, therefore, the midband value is typically employed for A_v in Eq. (9.42).

The reason for the constraint that the amplifier be of the inverting variety is now more apparent when one examines Eq. (9.42). A positive value for A_v would result in a negative capacitance (for $A_v > 1$).

The Miller effect will also increase the level of output capacitance, which must also be considered when the high-frequency cutoff is determined. In Fig. 9.45, the parameters of importance to determine the output Miller effect are in place. Applying Kirchhoff's current law results in

$$I_o = I_1 + I_2$$

with

$$I_1 = \frac{V_o}{R_o} \quad \text{and} \quad I_2 = \frac{V_o - V_i}{X_{C_f}}$$

The resistance R_o is usually sufficiently large to permit ignoring the first term of the equation compared to the second term and assuming that

$$I_o \cong \frac{V_o - V_i}{X_{C_f}}$$

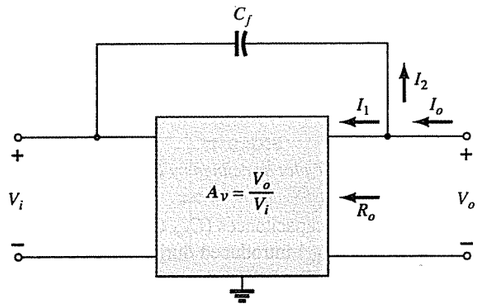


FIG. 9.45
Network employed in the derivation of an equation for the Miller output capacitance.

Substituting $V_i = V_o/A_v$ from $A_v = V_o/V_i$ results in

$$I_o = \frac{V_o - V_o/A_v}{X_{C_f}} = \frac{V_o(1 - 1/A_v)}{X_{C_f}}$$

and

$$\frac{I_o}{V_o} = \frac{1 - 1/A_v}{X_{C_f}}$$

or

$$\frac{V_o}{I_o} = \frac{X_{C_f}}{1 - 1/A_v} = \frac{1}{\omega C_f(1 - 1/A_v)} = \frac{1}{\omega C_{M_o}}$$

resulting in the following equation for the Miller output capacitance:

$$C_{M_o} = \left(1 - \frac{1}{A_v}\right)C_f \tag{9.43}$$

For the usual situation where $A_v \gg 1$, Eq. (9.43) reduces to

$$C_{M_o} \cong C_f \quad |A_v| >> 1 \tag{9.44}$$

Examples of the use of Eq. (9.43) appear in the next two sections as we investigate the high-frequency responses of BJT and FET amplifiers.

9.9 HIGH-FREQUENCY RESPONSE—BJT AMPLIFIER

At the high-frequency end, there are two factors that define the −3-dB *cutoff point: the network capacitance (parasitic and introduced) and the frequency dependence of* $h_{fe}(\beta)$.

Multisim

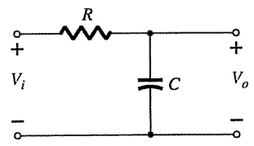


FIG. 9.46
RC combination that will define a high-cutoff frequency.

Network Parameters

In the high-frequency region, the *RC* network of concern has the configuration appearing in Fig. 9.46. At increasing frequencies, the reactance X_C will decrease in magnitude, resulting in a shorting effect across the output and a decrease in gain. The derivation leading to the corner frequency for this R_C configuration follows along similar lines to that encountered for the low-frequency region. The most significant difference is in the following general form of A_v:

$$A_v = \frac{1}{1 + j(f/f_2)} \tag{9.45}$$

This results in a magnitude plot such as shown in Fig. 9.47 that drops off at 6 dB/octave with increasing frequency. Note that f_2 is in the denominator of the frequency ratio rather than the numerator as occurred for f_1 in Eq. (9.21).

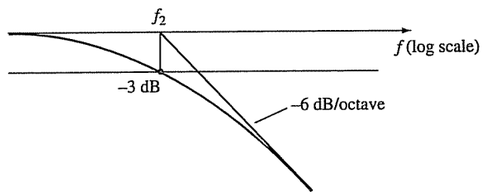


FIG. 9.47
Asymptotic plot as defined by Eq. (9.45).

In Fig. 9.48, the various parasitic capacitances (C_{be}, C_{bc}, C_{ce}) of the transistor are included with the wiring capacitances (C_{W_i}, C_{W_o}) introduced during construction. The high-frequency equivalent model for the network of Fig. 9.48 appears in Fig. 9.49. Note the absence of the capacitors C_S, C_C, and C_E, which are all assumed to be in the short-circuit state at these frequencies. The capacitance C_i includes the input wiring capacitance C_{W_i}, the transition capacitance C_{be}, and the Miller capacitance C_{M_i}. The capacitance C_o includes the output wiring capacitance C_{W_o}, the parasitic capacitance C_{ce}, and the output Miller capacitance C_{M_o}. In general, the capacitance C_{be} is the largest of the parasitic capacitances, with C_{ce} the smallest. In fact,

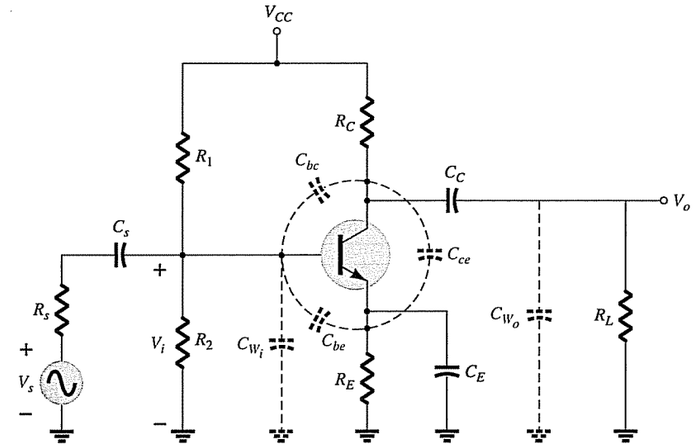


FIG. 9.48
Network of Fig. 9.18 with the capacitors that affect the high-frequency response.

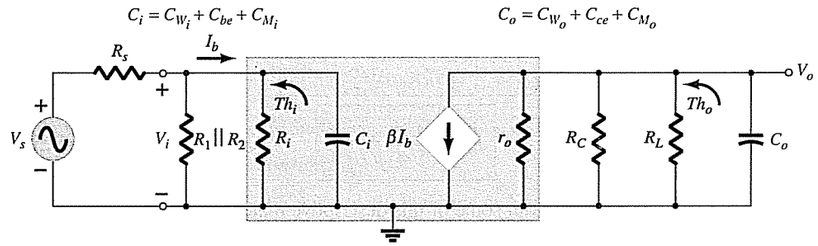


FIG. 9.49
High-frequency ac equivalent model for the network of Fig. 9.48.

most specification sheets simply provide the levels of C_{be} and C_{bc} and do not include C_{ce} unless it will affect the response of a particular type of transistor in a specific area of application.

Determining the Thévenin equivalent circuit for the input and output networks of Fig. 9.49 results in the configurations of Fig. 9.50. For the input network, the −3-dB frequency is defined by

$$f_{H_i} = \frac{1}{2\pi R_{\text{Th}_i} C_i} \tag{9.46}$$

with

$$R_{\text{Th}_i} = R_s \| R_1 \| R_2 \| R_i \tag{9.47}$$

and

$$C_i = C_{W_i} + C_{be} + C_{M_i} = C_{W_i} + C_{be} + (1 - A_v)C_{bc} \tag{9.48}$$

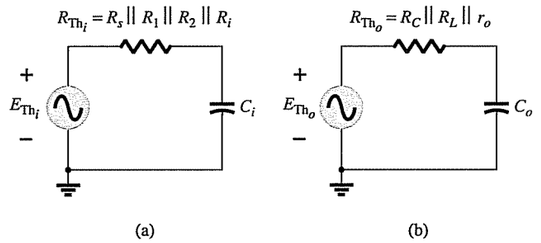


FIG. 9.50
Thévenin circuits for the input and output networks of the network of Fig. 9.49.

At very high frequencies, the effect of C_i is to reduce the total impedance of the parallel combination of R_1, R_2, R_i, and C_i in Fig. 9.49. The result is a reduced level of voltage across C_i, a reduction in I_b, and a gain for the system.

For the output network,

$$f_{H_o} = \frac{1}{2\pi R_{\text{Th}_o} C_o} \tag{9.49}$$

with

$$R_{Th_o} = R_C \| R_L \| r_o \tag{9.50}$$

and

$$C_o = C_{W_o} + C_{ce} + C_{M_o} \tag{9.51}$$

At very high frequencies, the capacitive reactance of C_o will decrease and consequently reduce the total impedance of the output parallel branches of Fig. 9.49. The net result is that V_o will also decline toward zero as the reactance X_C becomes smaller. The frequencies f_{H_i} and f_{H_o} will each define a −6-dB/octave asymptote such as depicted in Fig. 9.47. If the parasitic capacitors were the only elements to determine the high-cutoff frequency, the lowest frequency would be the determining factor. However, the decrease in h_{fe} (or β) with frequency must also be considered as to whether its break frequency is lower than f_{H_i} or f_{H_o}.

h_{fe} (or β) Variation

The variation of h_{fe} (or β) with frequency will approach, with some degree of accuracy, the following relationship:

$$h_{fe} = \frac{h_{fe_{\text{mid}}}}{1 + j(f/f_\beta)} \tag{9.52}$$

The use of h_{fe} rather than β in some of this descriptive material is due primarily to the fact that manufacturers typically use the hybrid parameters when covering this issue in their specification sheets, and so on.

The only undefined quantity, f_β, is determined by a set of parameters employed in the *hybrid* π or *Giacoletto* model introduced in Section 5.6. It appears in Fig. 9.51. The various parameters warrant a moment of explanation. The resistance r_b includes the base contact, base bulk, and base spreading resistance. The first is due to the actual connection to the base. The second includes the resistance from the external terminal to the active region of the transistors, and the last is the actual resistance within the active base region. The resistances r_π, r_o, and r_u are the resistances between the indicated terminals when the device is in the active region. The same is true for the capacitances C_{bc} and C_{be}, although the former is a transition capacitance, whereas the latter is a diffusion capacitance. A more detailed explanation of the frequency dependence of each can be found in a number of readily available texts.

If we remove the base resistance r_b, the base-to-collector resistance r_u, and all the parasitic capacitances, the result is an ac equivalent circuit that matches the small-signal equivalent for the common-emitter configuration used in Chapter 5. The base-to-emitter resistance r_π is βr_e and the output resistance r_o is simply a value provided through the hybrid parameter h_{oe}. The controlled source is also βI_b as used in Chapter 5. However, if we include the resistance r_u

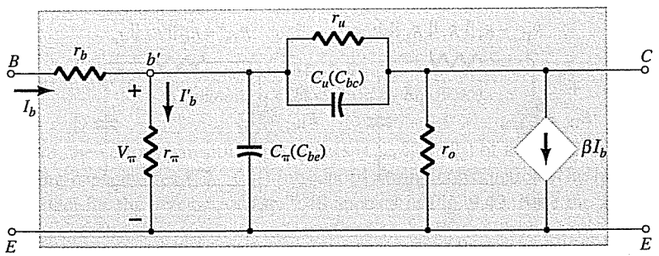


FIG. 9.51

Giacoletto (or hybrid π) high-frequency transistor small-signal ac equivalent circuit.

(usually quite large, $\gg \beta r_o$) between base and collector, it does provide a feedback loop between output and input circuits to match the contribution of h_{r_e} for the hybrid equivalent circuit. Recall from Chapter 5 that the feedback term is normally inconsequential for most applications, but if a particular application puts it at the forefront, then the model of Fig. 9.51 will bring it into play. The resistance r_u is a result of the fact that the base current is somewhat sensitive to the collector-to-base voltage. Since the base-to-emitter voltage is linearly related to the base current through Ohm's law and the output voltage is equal to the difference between the base-to-emitter voltage and collector-to-base voltage, we can conclude that the base current is sensitive to the changes in output voltage as revealed by the hybrid parameter h_{r_e}.

In terms of these parameters,

$$f_\beta \text{ (sometimes appearing as } f_{h_{fe}}) = \frac{1}{2\pi r_\pi (C_\pi + C_u)} \tag{9.53}$$

or, since $r_\pi = \beta r_e = h_{fe_{\text{mid}}} r_e$,

$$f_\beta = \frac{1}{h_{fe_{\text{mid}}}} \frac{1}{2\pi r_e (C_\pi + C_u)} \tag{9.54}$$

or

$$f_\beta \cong \frac{1}{2\pi \beta_{\text{mid}} r_e (C_\pi + C_u)} \tag{9.55}$$

Equation (9.55) clearly reveals that since r_e is a function of the network design:

f_β is a function of the bias configuration.

The basic format of Eq. (9.52) is exactly the same as Eq. (9.45) if we extract the multiplying factor $h_{fe_{\text{mid}}}$, revealing that h_{fe} will drop off from its midband value with a 6-dB/octave slope as shown in Fig. 9.52. The same figure has a plot of h_{fb} (or α) versus frequency. Note the small change in h_{fb} for the chosen frequency range, revealing that the common-base configuration displays improved high-frequency characteristics over the common-emitter

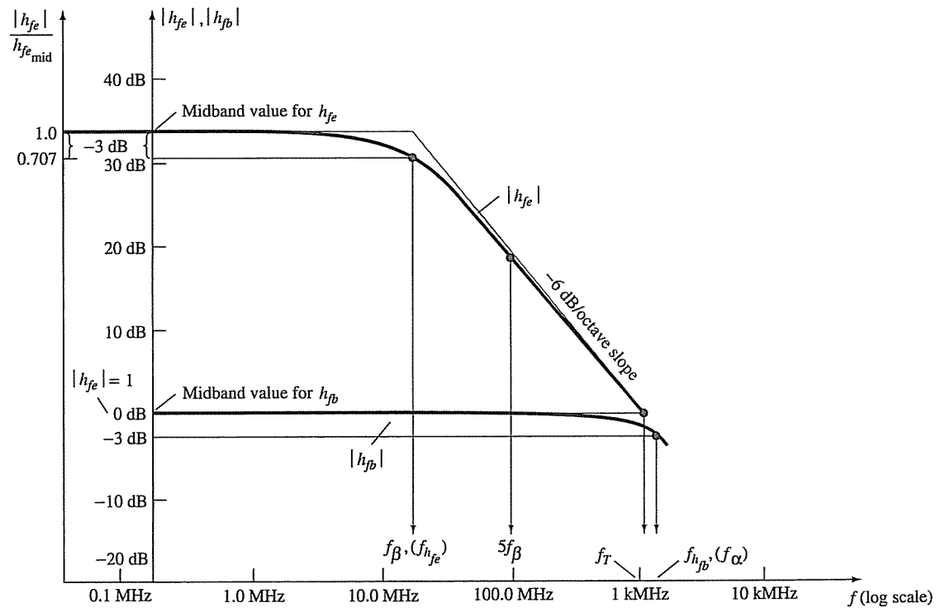


FIG. 9.52

h_{fe} and h_{fb} versus frequency in the high-frequency region.

configuration. Recall also the absence of the Miller effect capacitance due to the noninverting characteristics of the common-base configuration. For this very reason, common-base high-frequency parameters rather than common-emitter parameters are often specified for a transistor — especially those designed specifically to operate in the high-frequency regions.

The following equation permits a direct conversion for determining f_β if f_α and α are specified:

$$f_\beta = f_\alpha(1 - \alpha) \tag{9.56}$$

A quantity called the *gain–bandwidth product* is defined for the transistor by the condition

$$\left|\frac{h_{fe_{\text{mid}}}}{1 + j(f/f_\beta)}\right| = 1$$

so that

$$|h_{fe}|_{\text{dB}} = 20\log_{10}\left|\frac{h_{fe_{\text{mid}}}}{1 + j(f/f_\beta)}\right| = 20\log_{10}1 = 0\,\text{dB}$$

The frequency at which $|h_{fe}|_{\text{dB}} = 0$ dB is clearly indicated by f_T in Fig. 9.52. The magnitude of h_{fe} at the defined condition point ($f_T \gg f_\beta$) is given by

$$\frac{h_{fe_{\text{mid}}}}{\sqrt{1 + (f_T/f_\beta)^2}} \cong \frac{h_{fe_{\text{mid}}}}{f_T/f_\beta} = 1$$

so that

$$f_T \cong h_{fe_{\text{mid}}}\overbrace{f_\beta}^{(\cong \text{BW})} \quad \text{(gain–bandwidth product)} \tag{9.57}$$

or

$$f_T \cong \beta_{\text{mid}}\, f_\beta \tag{9.58}$$

with

$$f_\beta = \frac{f_T}{\beta_{\text{mid}}} \tag{9.59}$$

Substituting Eq. (9.55) for f_β in Eq. (9.57) gives

$$f_T \cong \beta_{\text{mid}}\frac{1}{2\pi\beta_{\text{mid}}r_e(C_\pi + C_u)}$$

and

$$f_T \cong \frac{1}{2\pi r_e(C_\pi + C_u)} \tag{9.60}$$

PSpice

EXAMPLE 9.11 Use the network of Fig. 9.48 with the same parameters as in Example 9.9, that is,

$$R_s = 1\,\text{k}\Omega, R_1 = 40\,\text{k}\Omega, R_2 = 10\,\text{k}\Omega, R_E = 2\,\text{k}\Omega, R_C = 4\,\text{k}\Omega, R_L = 2.2\,\text{k}\Omega$$
$$C_s = 10\,\mu\text{F}, C_C = 1\,\mu\text{F}, C_E = 20\,\mu\text{F}$$
$$\beta = 100, r_o = \infty\Omega, V_{CC} = 20\,\text{V}$$

with the addition of

$$C_\pi(C_{be}) = 36\,\text{pF}, C_u(C_{bc}) = 4\,\text{pF}, C_{ce} = 1\,\text{pF}, C_{W_i} = 6\,\text{pF}, C_{W_o} = 8\,\text{pF}$$

a. Determine f_{H_i} and f_{H_o}.
b. Find f_β and f_T.
c. Sketch the frequency response for the low- and high-frequency regions using the results of Example 9.9 and the results of parts (a) and (b).
d. Obtain the PSpice response for the full frequency spectrum and compare with the results of part (c).

Solution:

a. From Example 9.9:

$$R_i = 1.32\,\text{k}\Omega, \qquad A_{v_{\text{mid}}}(\text{amplifier}) = -90$$

and

$$R_{\text{Th}_i} = R_s\|R_1\|R_2\|R_i = 1\,\text{k}\Omega\,\|\,40\,\text{k}\Omega\,\|\,10\,\text{k}\Omega\,\|\,1.32\,\text{k}\Omega$$
$$\cong 0.531\,\text{k}\Omega$$

with

$$C_i = C_{W_i} + C_{be} + (1 - A_v)C_{be}$$
$$= 6\,\text{pF} + 36\,\text{pF} + [1 - (-90)]4\,\text{pF}$$
$$= 406\,\text{pF}$$
$$f_{H_i} = \frac{1}{2\pi R_{\text{Th}_i}C_i} = \frac{1}{2\pi(0.531\,\text{k}\Omega)(406\,\text{pF})}$$
$$= \mathbf{738.24\,kHz}$$
$$R_{\text{Th}_o} = R_C\|R_L = 4\,\text{k}\Omega\,\|2.2\,\text{k}\Omega = 1.419\,\text{k}\Omega$$
$$C_o = C_{W_o} + C_{ce} + C_{M_o} = 8\,\text{pF} + 1\,\text{pF} + \left(1 - \frac{1}{-90}\right)4\,\text{pF}$$
$$= 13.04\,\text{pF}$$
$$f_{H_o} = \frac{1}{2\pi R_{\text{Th}_o}C_o} = \frac{1}{2\pi(1.419\,\text{k}\Omega)(13.04\,\text{pF})}$$
$$= \mathbf{8.6\,MHz}$$

b. Applying Eq. (9.55) gives

$$f_\beta = \frac{1}{2\pi\beta_{\text{mid}}r_e(C_{be} + C_{bc})}$$
$$= \frac{1}{2\pi(100)(15.76\,\Omega)(36\,\text{pF} + 4\,\text{pF})} = \frac{1}{2\pi(100)(15.76\,\Omega)(40\,\text{pF})}$$
$$= \mathbf{2.52\,MHz}$$
$$f_T = \beta_{\text{mid}}f_\beta = (100)(2.52\,\text{MHz})$$
$$= \mathbf{252\,MHz}$$

c. See Fig. 9.53. Both f_β and f_{H_o} will lower the upper cutoff frequency below the level determined by f_{H_i}. The frequency f_β is closer to f_{H_i} and therefore will have a greater effect than f_{H_o}. In any event, the bandwidth will be less than that defined solely by f_{H_i}. In fact, for the parameters of this network the upper cutoff frequency will be relatively close to 600 kHz.

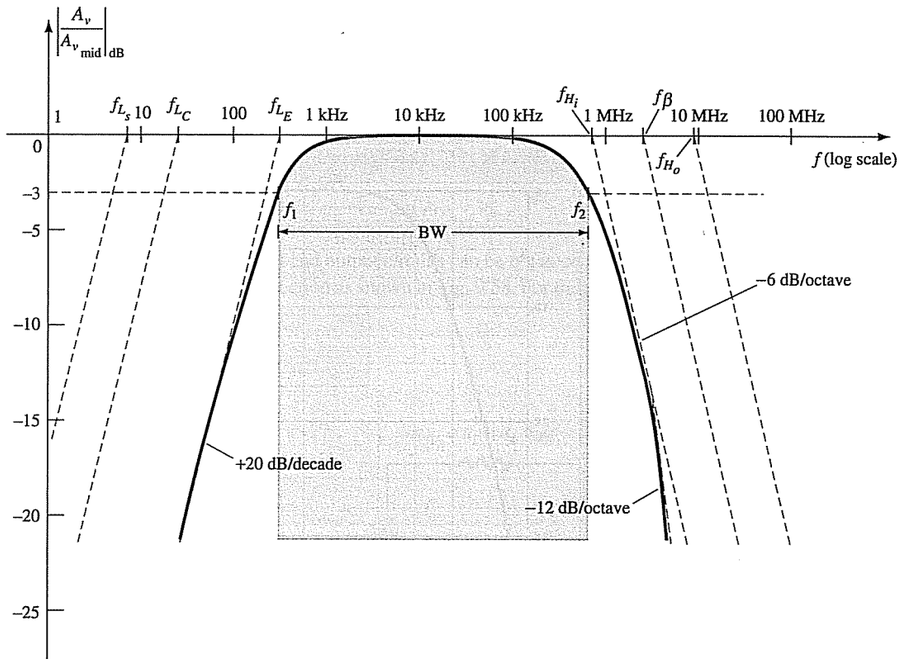


FIG. 9.53
Full frequency response for the network of Fig. 9.48.

In general, therefore, the lowest of the upper cutoff frequencies defines a maximum possible bandwidth for a system.

d. To obtain a PSpice analysis for the full frequency range, the parasitic capacitances have to be added to the network as shown in Fig. 9.54.

An **Analysis** will result in the plot of Fig. 9.55 using the **Trace Expression** appearing at the bottom of the plot. The vertical scale was changed from −60 to 0 dB to −30 to 0 dB to highlight the area of interest using the **Y-Axis Settings.** The low-cutoff frequency of 320.6 Hz is as determined primarily by f_{L_E}, and the high-cutoff frequency is near 663.7 kHz. Even though f_{H_o} is more than a decade higher than f_{H_i}, it will have an effect on the high-cutoff frequency. In total, however, the PSpice analysis is a welcome verification of the handwritten approach.

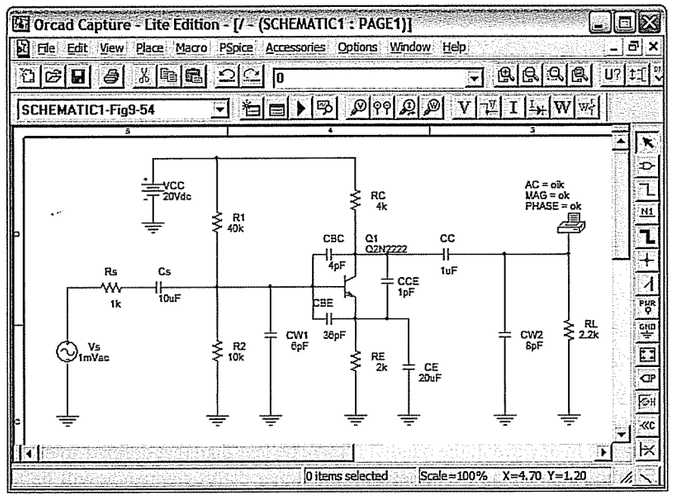


FIG. 9.54

Network of Fig. 9.27 with parasitic capacitances in place.

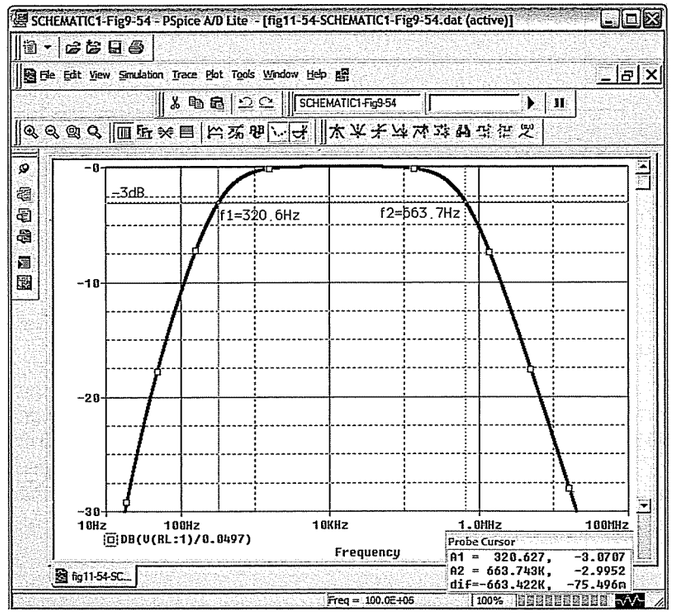


FIG. 9.55

Full frequency response for the network of Fig. 9.54.

9.10 HIGH-FREQUENCY RESPONSE–FET AMPLIFIER

The analysis of the high-frequency response of the FET amplifier will proceed in a very similar manner to that encountered for the BJT amplifier. As shown in Fig. 9.56, there are interelectrode and wiring capacitances that will determine the high-frequency characteristics of the amplifier. The capacitors C_{gs} and C_{gd} typically vary from 1 pF to 10 pF, whereas the capacitance C_{ds} is usually quite a bit smaller, ranging from 0.1 pF to 1 pF.

Since the network of Fig. 9.56 is an inverting amplifier, a Miller effect capacitance will appear in the high-frequency ac equivalent network appearing in Fig. 9.57. At high frequencies, C_i will approach a short-circuit equivalent and V_{gs} will drop in value and reduce the overall gain. At frequencies where C_o approaches its short-circuit equivalent, the parallel output voltage V_o will drop in magnitude.

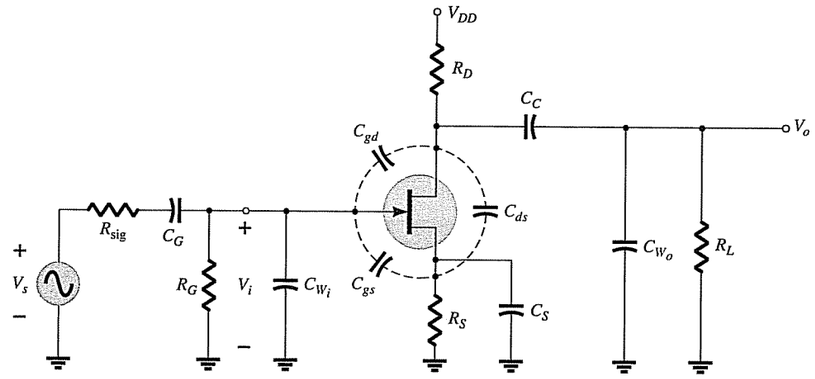


FIG. 9.56

Capacitive elements that affect the high-frequency response of a JFET amplifier.

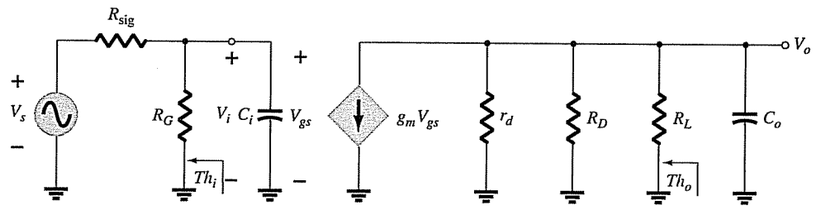


FIG. 9.57

High-frequency ac equivalent circuit for Fig. 9.56.

The cutoff frequencies defined by the input and output circuits can be obtained by first finding the Thévenin equivalent circuits for each section as shown in Fig. 9.58. For the input circuit,

$$f_{H_i} = \frac{1}{2\pi R_{\text{Th}_i} C_i} \tag{9.61}$$

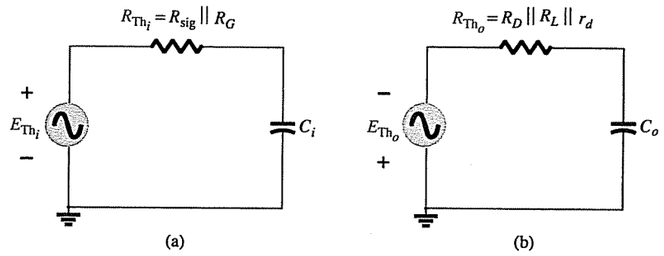


FIG. 9.58

The Thévenin equivalent circuits for (a) the input circuit and (b) the output circuit.

and

$$R_{\text{Th}_i} = R_{\text{sig}} \| R_G \tag{9.62}$$

with

$$C_i = C_{W_i} + C_{gs} + C_{M_i} \tag{9.63}$$

and

$$C_{M_i} = (1 - A_v)C_{gd} \tag{9.64}$$

for the output circuit,

$$f_{H_o} = \frac{1}{2\pi R_{\text{Th}_o} C_o} \tag{9.65}$$

with

$$R_{\text{Th}_o} = R_D \| R_L \| r_d \tag{9.66}$$

and

$$C_o = C_{W_o} + C_{ds} + C_{M_o} \tag{9.67}$$

and

$$C_{M_o} = \left(1 - \frac{1}{A_v}\right) C_{gd} \tag{9.68}$$

PSpice

EXAMPLE 9.12

a. Determine the high-cutoff frequencies for the network of Fig. 9.56 using the same parameters as Example 9.10:

$$C_G = 0.01\,\mu\text{F}, \quad C_C = 0.5\,\mu\text{F}, \quad C_S = 2\,\mu\text{F}$$
$$R_{\text{sig}} = 10\,\text{k}\Omega, \quad R_G = 1\,\text{M}\Omega, \quad R_D = 4.7\,\text{k}\Omega, \quad R_S = 1\,\text{k}\Omega, \quad R_L = 2.2\,\text{k}\Omega$$
$$I_{DSS} = 8\,\text{mA}, \quad V_P = -4\,\text{V}, \quad r_d = \infty\Omega, \quad V_{DD} = 20\,\text{V}$$

with the addition of

$$C_{gd} = 2\,\text{pF}, \quad C_{gs} = 4\,\text{pF}, \quad C_{ds} = 0.5\,\text{pF}, \quad C_{W_i} = 5\,\text{pF}, \quad C_{W_o} = 6\,\text{pF}$$

b. Obtain a PSpice response for the full frequency range and note whether it supports the conclusions of Example 9.10 and the calculations above.

Solution:

a. $R_{\text{Th}_i} = R_{\text{sig}} \| R_G = 10\,\text{k}\Omega \| 1\,\text{M}\Omega = 9.9\,\text{k}\Omega$

From Example 9.10, $A_v = -3$. We have

$$\begin{aligned} C_i &= C_{W_i} + C_{gs} + (1 - A_v)C_{gd} \\ &= 5\,\text{pF} + 4\,\text{pF} + (1 + 3)2\,\text{pF} \\ &= 9\,\text{pF} + 8\,\text{pF} \\ &= 17\,\text{pF} \end{aligned}$$

$$f_{H_i} = \frac{1}{2\pi R_{\text{Th}_i} C_i} = \frac{1}{2\pi(9.9\,\text{k}\Omega)(17\,\text{pF})} = \mathbf{945.67\,kHz}$$

$$\begin{aligned} R_{\text{Th}_o} &= R_D \| R_L \\ &= 4.7\,\text{k}\Omega \| 2.2\,\text{k}\Omega \\ &\cong 1.5\,\text{k}\Omega \end{aligned}$$

$$C_o = C_{W_o} + C_{ds} + C_{M_o} = 6\,\text{pF} + 0.5\,\text{pF} + \left(1 - \frac{1}{-3}\right)2\,\text{pF} = 9.17\,\text{pF}$$

$$f_{H_o} = \frac{1}{2\pi(1.5\,\text{k}\Omega)(9.17\,\text{pF})} = \mathbf{11.57\,MHz}$$

The results above clearly indicate that the input capacitance with its Miller effect capacitance will determine the upper cutoff frequency. This is typically the case due to the smaller value of C_{ds} and the resistance levels encountered in the output circuit.

b. With PSpice Windows, the schematic for the network appears as shown in Fig. 9.59.

For the full frequency response the **Start Frequency** is set at 10 Hz and the **End Frequency** at 10 MHz, and 1000 **Points** is selected. The **Trace Expression** is set as **DB(V(RL:1)/2.993 mV)** to obtain the plot of Fig. 9.60. Consider how much time it would take to sketch the curve of Fig. 9.60 using a hand-held calculator. We often forget how computer methods can save us an enormous amount of time.

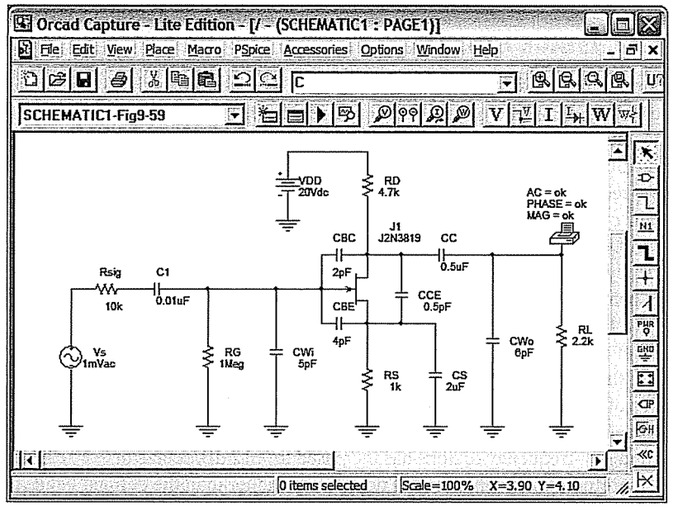


FIG. 9.59
Network of Fig. 9.56 with assigned values.

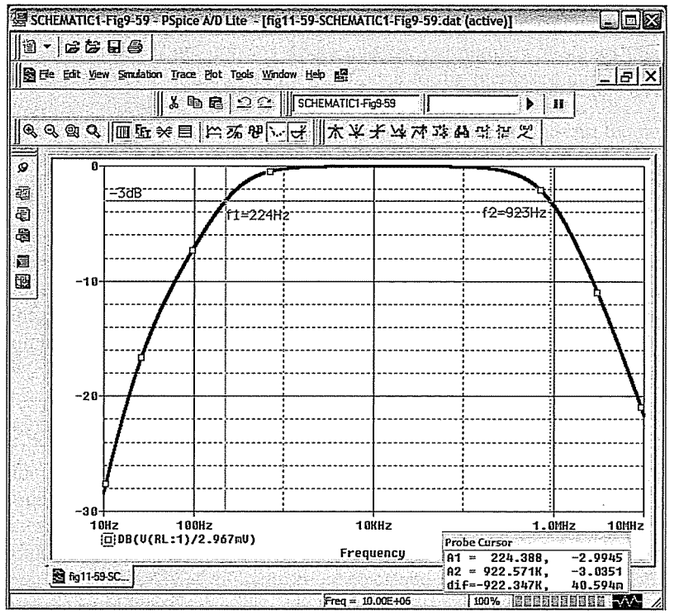


FIG. 9.60
Frequency response for the network of Example 9.12.

Using the cursor, we find the lower and upper cutoff frequencies to be 224 Hz and 923 kHz, respectively, providing a nice match with the calculated values.

Even though the analysis of the last few sections has been limited to two configurations, the general procedure for determining the cutoff frequencies should support the analysis of any other transistor configuration. Keep in mind that the Miller capacitance is limited to inverting amplifiers and that f_α is significantly greater than f_β if the common-base configuration is encountered. There is a great deal more literature on the analysis of single-stage amplifiers that goes beyond the coverage of this chapter. However, the content of this chapter should provide a firm foundation for any analysis of frequency effects.

9.11 MULTISTAGE FREQUENCY EFFECTS

For a second transistor stage connected directly to the output of a first stage, there will be a significant change in the overall frequency response. In the high-frequency region, the output capacitance C_o must now include the wiring capacitance (C_{W_1}), parasitic capacitance (C_{be}), and Miller capacitance (C_{M_i}) of the following stage. Furthermore, there will be additional low-frequency cutoff levels due to the second stage, which will further reduce the overall gain of the system in this region. For each additional stage, the upper cutoff frequency will be determined primarily by the stage having the lowest cutoff frequency. The low-frequency cutoff is primarily determined by that stage having the highest low-frequency cutoff frequency. Obviously, therefore, one poorly designed stage can offset an otherwise well-designed cascaded system.

The effect of increasing the number of *identical* stages can be clearly demonstrated by considering the situations indicated in Fig. 9.61. In each case, the upper and lower cutoff frequencies of each of the cascaded stages are identical. For a single stage, the cutoff frequencies are f_1 and f_2 as indicated. For two identical stages in cascade, the drop-off rate in the high- and low-frequency regions has increased to -12 dB/octave or -40 dB/decade. At f_1 and f_2, therefore, the decibel drop is now -6 dB rather than the defined band frequency gain level of -3 dB. The -3-dB point has shifted to f_1' and f_2' as indicated, with a resulting drop in the bandwidth. A -18-dB/octave or -60-dB/decade slope will result for a three-stage system of identical stages with the indicated reduction in bandwidth (f_1'' and f_2'').

Assuming identical stages, we can determine an equation for each band frequency as a function of the number of stages (n) in the following manner: For the low-frequency region,

$$A_{v_{\text{low, (overall)}}} = A_{v_{1_{\text{low}}}} A_{v_{2_{\text{low}}}} A_{v_{3_{\text{low}}}} \cdots A_{v_{n_{\text{low}}}}$$

but since all stages are identical, $A_{v_{1_{\text{low}}}} = A_{v_{2_{\text{low}}}} = \text{etc.}$, and

$$A_{v_{\text{low, (overall)}}} = (A_{v_{1_{\text{low}}}})^n$$

or

$$\frac{A_{v_{\text{low}}}}{A_{v_{\text{mid}}}} \text{ (overall)} = \left(\frac{A_{v_{\text{low}}}}{A_{v_{\text{mid}}}}\right)^n = \frac{1}{(1 - jf_1/f)^n}$$

Setting the magnitude of this result equal to $1/\sqrt{2}$(-3 dB level) results in

$$\frac{1}{\sqrt{[1 + (f_1/f_1')^2]^n}} = \frac{1}{\sqrt{2}}$$

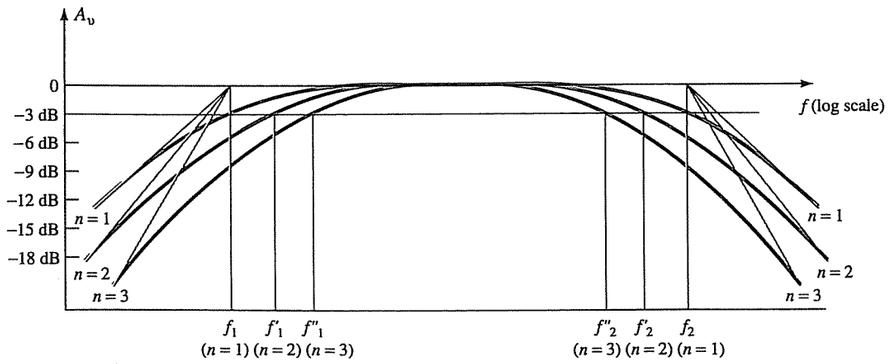


FIG. 9.61
Effect of an increased number of stages on the cutoff frequencies and the bandwidth.

or

$$\left\{\left[1 + \left(\frac{f_1}{f_1'}\right)^{2^-}\right]^{1/2}\right\}^n = \left\{\left[1 + \left(\frac{f_1}{f_1'}\right)^2\right]^n\right\}^{1/2} = (2)^{1/2}$$

so that

$$\left[1 + \left(\frac{f_1}{f_1'}\right)^2\right]^n = 2$$

and

$$1 + \left(\frac{f_1}{f_1'}\right)^2 = 2^{1/n}$$

with the result that

$$\boxed{f_1' = \frac{f_1}{\sqrt{2^{1/n} - 1}}} \tag{9.69}$$

In a similar manner, it can be shown that for the high-frequency region,

$$\boxed{f_2' = (\sqrt{2^{1/n} - 1})\, f_2} \tag{9.70}$$

Note the presence of the same factor $\sqrt{2^{1/n} - 1}$ in each equation. The magnitude of this factor for various values of n is listed below.

n	$\sqrt{2^{1/n} - 1}$
2	0.64
3	0.51
4	0.43
5	0.39

For $n = 2$, consider that the upper cutoff frequency $f_2' = 0.64f_2$, or 64% of the value obtained for a single stage, whereas $f_1' = (1/0.64)f_1 = 1.56f_1$. For $n = 3, f_2' = 0.51f_2$, or approximately one-half the value of a single stage, and $f_1' = (1/0.51)f_1 = 1.96f_1$, or approximately *twice* the single-stage value.

For the *RC*-coupled transistor amplifier, if $f_2 = f_\beta$, or if they are close enough in magnitude for both to affect the upper 3-dB frequency, the number of stages must be increased by a factor of 2 when determining f_2' due to the increased number of factors $1/(1 + jf/f_x)$.

A decrease in bandwidth is not always associated with an increase in the number of stages if the midband gain can remain fixed and independent of the number of stages. For instance, if a single-stage amplifier produces a gain of 100 with a bandwidth of 10,000 Hz, the resulting gain–bandwidth product is $10^2 \times 10^4 = 10^6$. For a two-stage system the same gain can be obtained by having two stages with a gain of 10 since ($10 \times 10 = 100$). The bandwidth of each stage would then increase by a factor of 10 to 100,000 due to the lower gain requirement and fixed gain–bandwidth product of 10^6. Of course, the design must be such as to permit the increased bandwidth and establish the lower gain level.

9.12 SQUARE-WAVE TESTING

A sense for the frequency response of an amplifier can be determined experimentally by applying a square-wave signal to the amplifier and noting the output response. The shape of the output waveform will reveal whether the high or low frequencies are being properly amplified. Using *square-wave testing* is significantly less time-consuming than applying a series of sinusoidal signals at different frequencies and magnitudes to test the frequency response of the amplifier.

The reason for choosing a square-wave signal for the testing process is best described by examining the *Fourier series* expansion of a square wave composed of a series of sinusoidal components of different magnitudes and frequencies. The summation of the terms of the series will result in the original waveform. In other words, even though a waveform may not be sinusoidal, it can be reproduced by a series of sinusoidal terms of different frequencies and magnitudes.

The Fourier series expansion for the square wave of Fig. 9.62 is

$$v = \frac{4}{\pi} V_m \left(\sin 2\pi f_s t + \frac{1}{3} \sin 2\pi(3f_s)t + \frac{1}{5} \sin 2\pi(5f_s)t + \frac{1}{7} \sin 2\pi(7f_s)t + \frac{1}{9} \sin 2\pi(9f_s)t + \cdots + \frac{1}{n} \sin 2\pi(nf_s)t \right) \quad \textbf{(9.71)}$$

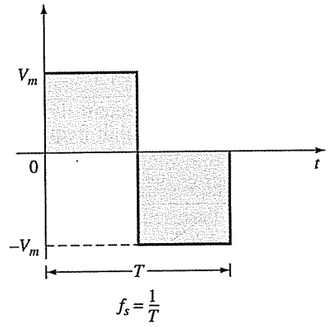


FIG. 9.62
Square wave.

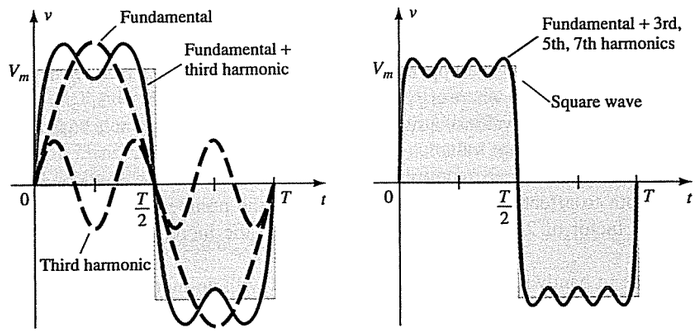


FIG. 9.63
Harmonic content of a square wave.

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The first term of the series is called the *fundamental* term and in this case has the same frequency, f_s, as the square wave. The next term has a frequency equal to three times the fundamental and is referred to as the *third harmonic*. Its magnitude is one-third the magnitude of the fundamental term. The frequencies of the succeeding terms are odd multiples of the fundamental term, and the magnitude decreases with each higher harmonic. Figure 9.63 demonstrates how the summation of terms of a Fourier series can result in a nonsinusoidal waveform. The generation of the square wave of Fig. 9.62 would require an infinite number of terms. However, the summation of just the fundamental term and the third harmonic in Fig. 9.63a clearly results in a waveform that is beginning to take on the appearance of a square wave. Including the fifth and seventh harmonics as in Fig. 9.63b takes us a step closer to the waveform of Fig. 9.62.

Since the ninth harmonic has a magnitude greater than 10% of the fundamental term $[\frac{1}{9}(100\%) = 11.1\%]$, the terms from the fundamental term through the ninth harmonic are the major contributors to the Fourier series expansion of the square-wave function. It is therefore reasonable to assume that if the application of a square wave of a particular frequency results in a nice clean square wave at the output, then the terms from the fundamental through the ninth harmonic are being amplified without visual distortion by the amplifier. For instance, if an audio amplifier with a bandwidth of 20 kHz (audio range is from 20 Hz to 20 kHz) is to be tested, the frequency of the applied signal should be at least 20 kHz/9 = 2.22 kHz.

If the response of an amplifier to an applied square wave is an undistorted replica of the input, the frequency response (or BW) of the amplifier is obviously sufficient for the applied frequency. If the response is as shown in Fig. 9.64a and b, the low frequencies are not being amplified properly and the low cutoff frequency has to be investigated. If the waveform has the appearance of Fig. 9.64c, the high-frequency components are not receiving sufficient amplification and the high-cutoff frequency (or BW) has to be reviewed.

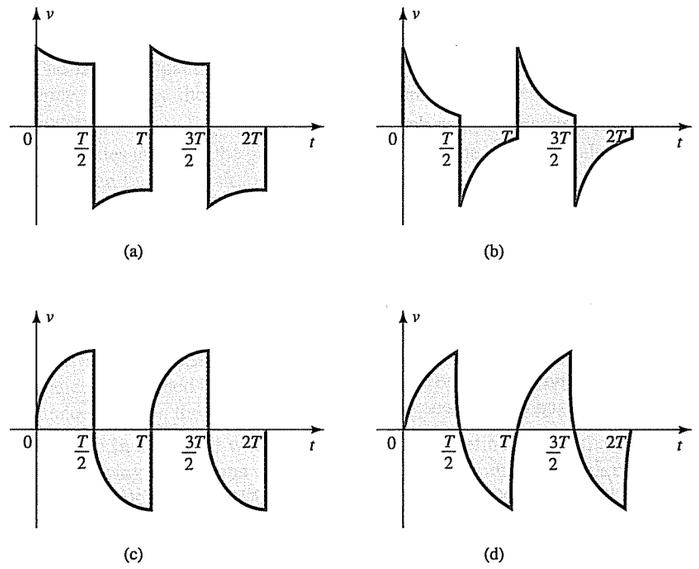


FIG. 9.64
(a) Poor low-frequency response; (b) very poor low-frequency response; (c) poor high-frequency response; (d) very poor high-frequency response.

The actual high-cutoff frequency (or BW) can be determined from the output waveform by carefully measuring the rise time defined between 10% and 90% of the peak value, as shown in Fig. 9.65. Substituting into the following equation will provide the upper cutoff

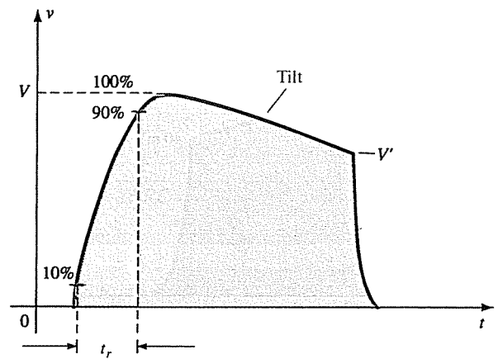


FIG. 9.65
Defining the rise time and tilt of a square wave response.

frequency, and because $\text{BW} = f_{H_i} - f_{L_o} \cong f_{H_i}$, the equation also provides an indication of the BW of the amplifier:

$$\boxed{\text{BW} \cong f_{H_i} = \frac{0.35}{t_r}} \tag{9.72}$$

The low-cutoff frequency can be determined from the output response by carefully measuring the tilt of Fig. 9.65 and substituting into one of the following equations:

$$\boxed{\%\,\text{tilt} = P\% = \frac{V - V'}{V} \times 100\%} \tag{9.73}$$

$$\boxed{\text{tilt} = P = \frac{V - V'}{V}} \quad \text{(decimal form)} \tag{9.74}$$

The low-cutoff frequency is then determined from

$$\boxed{f_{L_o} = \frac{P}{\pi} f_s} \tag{9.75}$$

EXAMPLE 9.13 The application of a 1-mV, 5-kHz square wave to an amplifier resulted in the output waveform of Fig. 9.66.

a. Write the Fourier series expansion for the square wave through the ninth harmonic.
b. Determine the bandwidth of the amplifier.
c. Calculate the low-cutoff frequency.

Solution:

a. $$v_i = \frac{4\,\text{mV}}{\pi}\left(\sin 2\pi\,(5 \times 10^3)t + \frac{1}{3}\sin 2\pi(15 \times 10^3)t + \frac{1}{5}\sin 2\pi(25 \times 10^3)t + \frac{1}{7}\sin 2\pi(35 \times 10^3)t + \frac{1}{9}\sin 2\pi(45 \times 10^3)t\right)$$

b. $$t_r = 18\,\mu\text{s} - 2\,\mu\text{s} = 16\,\mu\text{s}$$

$$\text{BW} = \frac{0.35}{t_r} = \frac{0.35}{16\,\mu\text{s}} = \mathbf{21{,}875\ Hz} \cong 4.4f_s$$

c. $$P = \frac{V - V'}{V} = \frac{50\,\text{mV} - 40\,\text{mV}}{50\,\text{mV}} = 0.2$$

$$f_{L_o} = \frac{P}{\pi} f_s = \left(\frac{0.2}{\pi}\right)(5\,\text{kHz}) = \mathbf{318.31\ Hz}$$

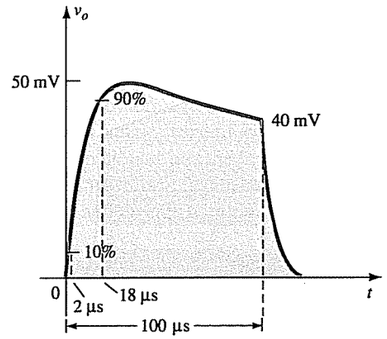


FIG. 9.66
Example 9.13.

9.13 SUMMARY

Important Conclusions and Concepts

1. The logarithm of a number gives the **power to which the base must be brought to obtain the same number.** If the base is 10, it is referred to as the **common logarithm;** if the base is $e = 2.71828\ldots$, it is called the **natural logarithm.**
2. Since the decibel rating of any piece of equipment is a **comparison between levels,** a reference level must be selected for each area of application. For audio systems the reference level is generally accepted as **1 mW.** When using voltage levels to determine the gain in dB between two points, any difference in resistance level is generally ignored.
3. The dB gain of cascaded systems is simply the **sum** of the dB gains of each stage.
4. It is the **capacitive elements** of a network that determine the **bandwidth** of a system. The **larger** capacitive elements of the basic design determine the **low**-cutoff frequency, whereas the **smaller** parasitic capacitors determine the **high**-cutoff frequencies.
5. The frequencies at which the gain drops to 70.7% of the midband value are called the **cutoff, corner, band, break,** or **half-power** frequencies.
6. The **narrower** the bandwidth, the **smaller** is the range of frequencies that will permit a transfer of power to the load that is at least 50% of the midband level.
7. A change in frequency by a factor of **two,** equivalent to **one octave,** results in a **6-dB change in gain.** For a **10:1** change in frequency, equivalent to **one decade,** there is a **20-dB change in gain.**
8. For any **inverting** amplifier, the input capacitance will be increased by a **Miller effect** capacitance determined by the **gain** of the amplifier and the **interelectrode** (parasitic) capacitance between the input and output terminals of the active device.
9. A **3-dB drop in beta** (h_{fe}) will occur at a frequency defined by f_β that is sensitive to the **dc operating conditions** of the transistor. This variation in beta can define the upper cutoff frequency of the design.
10. The **high- and low-cutoff frequencies** of an amplifier can be determined by the response of the system to a **square-wave input.** The general appearance will immediately reveal whether the low- or high-frequency response of the system is too limited for the applied frequency, whereas a more detailed examination of the response will reveal the actual bandwidth of the amplifier.

Equations

Logarithms:

$$a = b^x, \qquad x = \log_b a, \qquad \log_{10}\frac{a}{b} = \log_{10} a - \log_{10} b$$

$$\log_{10} ab = \log_{10} a + \log_{10} b, \qquad G_{\text{dB}} = 10\log_{10}\frac{P_2}{P_1} = 20\log_{10}\frac{V_2}{V_1}$$

$$G_{\text{dB}_T} = G_{\text{dB}_1} + G_{\text{dB}_2} + G_{\text{dB}_3} + \cdots + G_{\text{dB}_n}$$

Low-frequency response:

$$A_v = \frac{1}{1 - j(f_1/f)}, \qquad f_1 = \frac{1}{2\pi RC}$$

BJT low-frequency response:

$$f_{L_s} = \frac{1}{2\pi(R_s + R_i)C_s}, \qquad R_i = R_1 \| R_2 \| \beta r_e$$

$$f_{L_C} = \frac{1}{2\pi(R_O + R_L)C_C}, \qquad R_o = R_C \| r_o$$

$$f_{L_E} = \frac{1}{2\pi R_e C_E}, \qquad R_e = R_E \| \left(\frac{R_s'}{\beta} + r_e\right), \qquad R_s' = R_s \| R_1 \| R_2$$

FET low-frequency response:

$$f_{L_G} = \frac{1}{2\pi(R_{\text{sig}} + R_i)C_G}, \qquad R_i = R_G$$

$$f_{L_C} = \frac{1}{2\pi(R_o + R_L)C_C}, \qquad R_o = R_D \| r_d$$

$$f_{L_s} = \frac{1}{2\pi R_{eq} C_S}, \qquad R_{eq} = \frac{R_S}{1 + R_S(1 + g_m r_d)/(r_d + R_D \| R_L)} \cong R_S \left\| \frac{1}{g_m} \right|_{r_d \cong \infty\,\Omega}$$

Miller effect capacitance:

$$C_{M_i} = (1 - A_v)C_f, \qquad C_{M_o} = \left(1 - \frac{1}{A_v}\right)C_f$$

BJT high-frequency response:

$$A_v = \frac{1}{1 + j(f/f_2)}, \qquad f_{H_i} = \frac{1}{2\pi R_{\text{Th}_i} C_i}, \qquad R_{\text{Th}_i} = R_s \| R_1 \| R_2 \| R_i,$$

$$C_i = C_{W_i} + C_{be} + C_{M_i}$$

$$f_{H_o} = \frac{1}{2\pi R_{\text{Th}_o} C_o}, \qquad R_{\text{Th}_o} = R_C \| R_L \| r_o, \qquad C_o = C_{W_o} + C_{ce} + C_{M_o},$$

$$h_{fe} = \frac{h_{fe_{\text{mid}}}}{1 + j(f/f_\beta)}$$

$$f_\beta \cong \frac{1}{2\pi \beta_{\text{mid}} r_e (C_{be} + C_{bc})}$$

$$f_T \cong h_{fe_{\text{mid}}} f_\beta$$

FET high-frequency response:

$$f_{H_i} = \frac{1}{2\pi R_{\text{Th}_i} C_i}, \qquad R_{\text{Th}_i} = R_{\text{sig}} \| R_G, \qquad C_i = C_{W_i} + C_{gs} + C_{M_i},$$

$$C_{M_i} = (1 - A_v)C_{gd}$$

$$f_{H_o} = \frac{1}{2\pi R_{\text{Th}_o} C_o}, \qquad R_{\text{Th}_o} = R_D \| R_L \| r_d, \qquad C_o = C_{W_o} + C_{ds} + C_{M_o},$$

$$C_{M_o} = \left(1 - \frac{1}{A_v}\right)C_{gd}$$

Multistage effects:

$$f_1' = \frac{f_1}{\sqrt{2^{1/n} - 1}}, \qquad f_2' = (\sqrt{2^{1/n} - 1})f_2$$

Square-wave testing:

$$\text{BW} \cong f_{H_i} = \frac{0.35}{t_r}, \qquad f_{L_o} = \frac{P}{\pi} f_s, \qquad P = \frac{V - V'}{V}$$

9.14 COMPUTER ANALYSIS

The computer analysis of this chapter was integrated into the preceding text for emphasis and a clear demonstration of the power of the PSpice software package. The complete frequency response of a single-stage or multistage system can be determined in a relatively short period of time to verify theoretical calculations or provide an immediate indication of the low- and high-cutoff frequencies of the system. The exercises in the chapter will provide an opportunity to apply the PSpice software package to a variety of networks.

PROBLEMS

**Note:* Asterisks indicate more difficult problems.

9.2 Logarithms

1. **a.** Determine the common logarithm of the following numbers: 10^3, 50, and 0.707.
   b. Determine the natural logarithm of the numbers appearing in part (a).
   c. Compare the solutions of parts (a) and (b).
2. **a.** Determine the common logarithm of the number 2.2×10^3.
   b. Determine the natural logarithm of the number of part (a) using Eq. (9.4).
   c. Determine the natural logarithm of the number of part (a) using natural logarithms and compare with the solution of part (b).
3. Determine:
   a. $20 \log_{10} \frac{40}{8}$ using Eq. (9.6) and compare with $20 \log_{10} 5$.
   b. $10 \log_{10} \frac{1}{20}$ using Eq. (9.7) and compare with $10 \log_{10} 0.05$.
   c. $\log_{10}(40)(0.125)$ using Eq. (9.8) and compare with $\log_{10} 5$.
4. Calculate the power gain in decibels for each of the following cases.
   a. $P_o = 100\,\text{W}, P_i = 5\,\text{W}$.
   b. $P_o = 100\,\text{mW}, P_i = 5\,\text{mW}$.
   c. $P_o = 100\,\text{mW}, P_i = 20\,\mu\text{W}$.
5. Determine G_{dBm} for an output power level of 25 W.
6. Two voltage measurements made across the same resistance are $V_1 = 25\,\text{V}$ and $V_2 = 100\,\text{V}$. Calculate the power gain in decibels of the second reading over the first reading.
7. Input and output voltage measurements of $V_i = 10\,\text{mV}$ and $V_o = 25\,\text{V}$ are made. What is the voltage gain in decibels?

*8. **a.** The total decibel gain of a three-stage system is 120 dB. Determine the decibel gain of each stage if the second stage has twice the decibel gain of the first and the third has 2.7 times the decibel gain of the first.
   b. Determine the voltage gain of each stage.

*9. If the applied ac power to a system is $5\,\mu\text{W}$ at 100 mV and the output power is 48 W, determine:
   a. The power gain in decibels.
   b. The voltage gain in decibels if the output impedance is $40\,\text{k}\Omega$.
   c. The input impedance.
   d. The output voltage.

9.4 General Frequency Considerations

10. Given the characteristics of Fig. 9.67, sketch:
   a. The normalized gain.
   b. The normalized dB gain (and determine the bandwidth and cutoff frequencies).

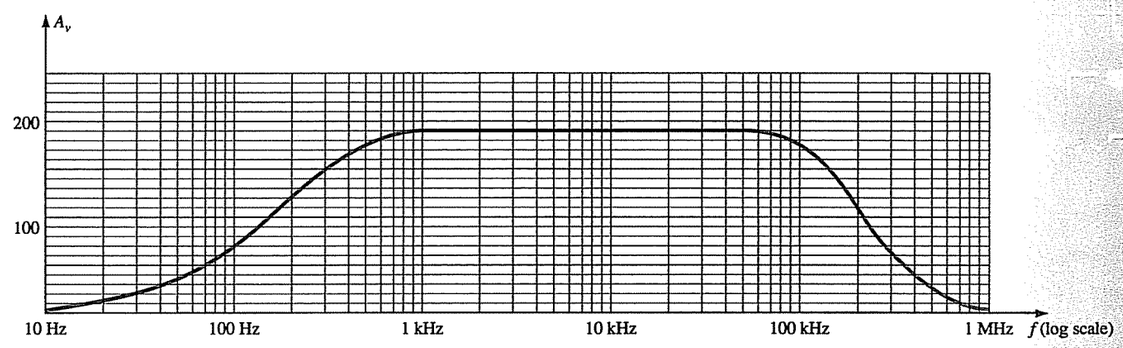


FIG. 9.67
Problem 10.

9.5 Low-Frequency Analysis–Bode Plot

11. For the network of Fig. 9.68:
   a. Determine the mathematical expression for the magnitude of the ratio V_o/V_i.
   b. Using the results of part (a), determine V_o/V_i at 100 Hz, 1 kHz, 2 kHz, 5 kHz, and 10 kHz, and plot the resulting curve for the frequency range of 100 Hz to 10 kHz. Use a log scale.
   c. Determine the break frequency.
   d. Sketch the asymptotes and locate the −3-dB point.
   e. Sketch the frequency response for V_o/V_i and compare to the results of part (b).

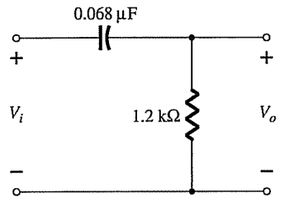


FIG. 9.68
Problems 11, 12, and 32.

12. For the network of Fig. 9.68:
- **a.** Determine the mathematical expression for the angle by which V_o leads V_i.
- **b.** Determine the phase angle at $f = 100$ Hz, 1 kHz, 2 kHz, 5 kHz, and 10 kHz, and plot the resulting curve for the frequency range of 100 Hz to 10 kHz.
- **c.** Determine the break frequency.
- **d.** Sketch the frequency response of θ for the frequency spectrum of part (b) and compare results.

13. **a.** What frequency is one octave above 5 kHz?
- **b.** What frequency is one decade below 10 kHz?
- **c.** What frequency is two octaves below 20 kHz?
- **d.** What frequency is two decades above 1 kHz?

9.6 Low-Frequency Response–BJT Amplifier

14. Repeat the analysis of Example 9.9 with $r_o = 40\,\text{k}\Omega$. What is the effect on $A_{v_{\text{mid}}}$, f_{L_S}, f_{L_C}, f_{L_E}, and the resulting cutoff frequency?

15. For the network of Fig. 9.69:
- **a.** Determine r_e.
- **b.** Find $A_{v_{\text{mid}}} = V_o/V_i$.
- **c.** Calculate Z_i.
- **d.** Find $A_{v_{S\text{mid}}} = V_o/V_s$.
- **e.** Determine f_{L_S}, f_{L_C}, and f_{L_E}.
- **f.** Determine the low cutoff frequency.
- **g.** Sketch the asymptotes of the Bode plot defined by the cutoff frequencies of part (e).
- **h.** Sketch the low-frequency response for the amplifier using the results of part (f).

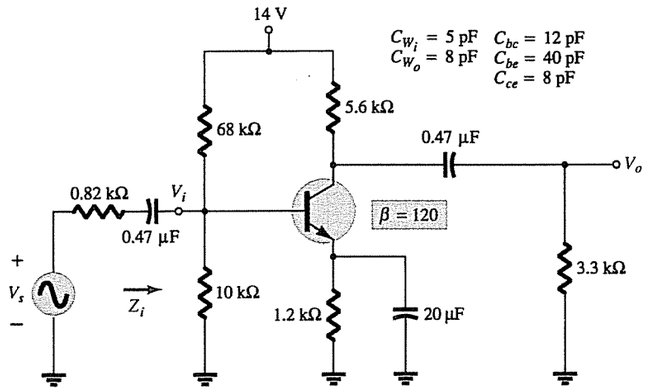


FIG. 9.69
Problems 15, 22, and 33.

***16.** Repeat Problem 15 for the emitter-stabilized network of Fig. 9.70.

***17.** Repeat Problem 15 for the emitter-follower network of Fig. 9.71.

***18.** Repeat Problem 15 for the common-base configuration of Fig. 9.72. Keep in mind that the common-base configuration is a noninverting network when you consider the Miller effect.

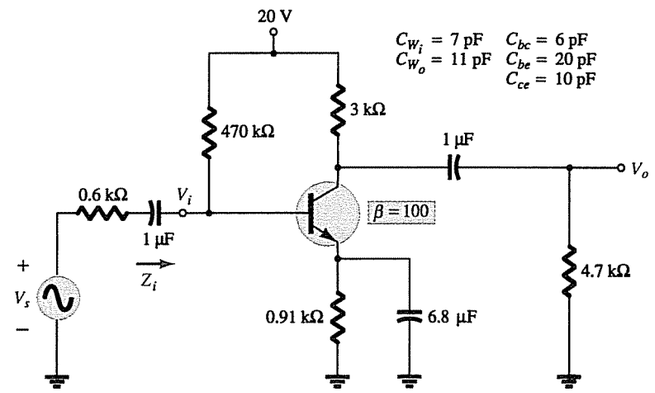


FIG. 9.70
Problems 16 and 23.

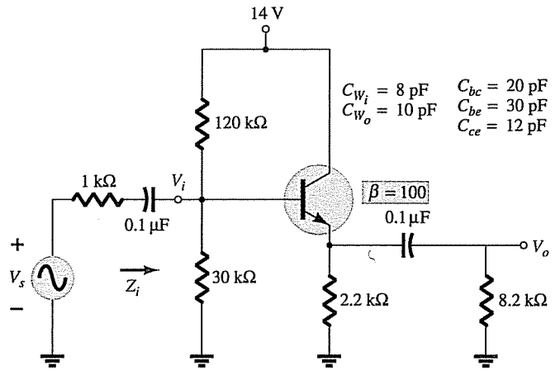


FIG. 9.71
Problems 17 and 24.

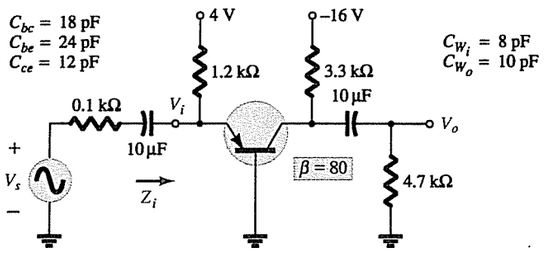


FIG. 9.72
Problems 18, 25, and 34.

9.7 Low-Frequency Response–FET Amplifier

19. For the network of Fig. 9.73:
- **a.** Determine V_{GS_Q} and I_{D_Q}.
- **b.** Find g_{m0} and g_m.
- **c.** Calculate the midband gain of $A_v = V_o/V_i$.
- **d.** Determine Z_i.
- **e.** Calculate $A_{v_s} = V_o/V_s$.
- **f.** Determine f_{L_G}, f_{L_C}, and f_{L_S}.
- **g.** Determine the low-cutoff frequency.

h. Sketch the asymptotes of the Bode plot defined by part (f).
i. Sketch the low-frequency response for the amplifier using the results of part (f).

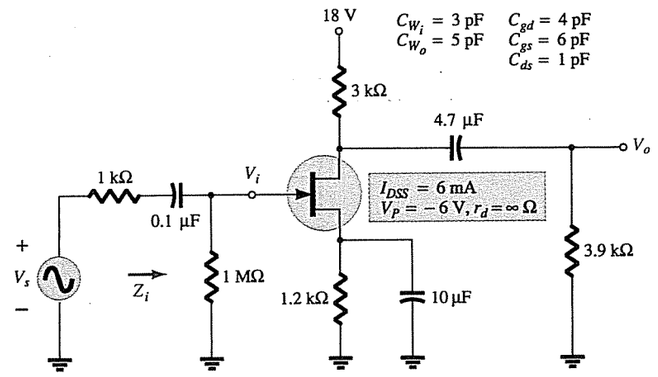


FIG. 9.73
Problems 19, 20, 26, and 35.

***20.** Repeat the analysis of Problem 19 with $r_d = 100\ \text{k}\Omega$. Does it have an effect of any consequence on the results? If so, which elements?

***21.** Repeat the analysis of Problem 19 for the network of Fig. 9.74. What effect does the voltage-divider configuration have on the input impedance and the gain A_{v_s} compared to the biasing arrangement of Fig. 9.73?

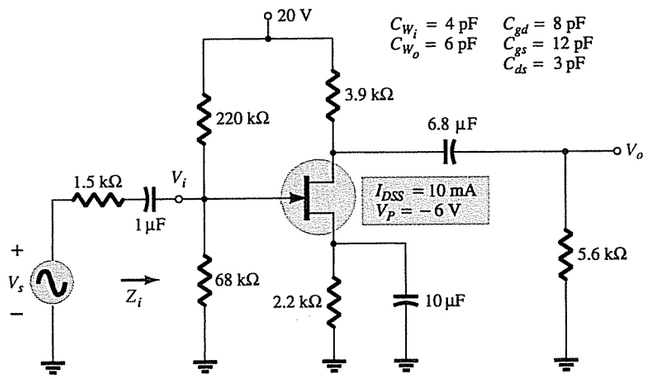


FIG. 9.74
Problems 21 and 27.

9.9 High-Frequency Response–BJT Amplifier

***22.** For the network of Fig. 9.69:
a. Determine f_{H_i} and f_{H_o}.
b. Find f_β and f_T.
c. Sketch the frequency response for the high-frequency region using a Bode plot and determine the cutoff frequency.

***23.** Repeat the analysis of Problem 22 for the network of Fig. 9.70.

***24.** Repeat the analysis of Problem 22 for the network of Fig. 9.71.

***25.** Repeat the analysis of Problem 22 for the network of Fig. 9.72.

9.10 High-Frequency Response–FET Amplifier

26. For the network of Fig. 9.73:
a. Determine g_{m_0} and g_m.
b. Find A_v and A_{v_s} in the mid-frequency range.

c. Determine f_{H_i} and f_{H_o}.
d. Sketch the frequency response for the high-frequency region using a Bode plot and determine the cutoff frequency.

***27.** Repeat the analysis of Problem 26 for the network of Fig. 9.74.

9.11 Multistage Frequency Effects

28. Calculate the overall voltage gain of four identical stages of an amplifier, each having a gain of 20.

29. Calculate the overall upper 3-dB frequency for a four-stage amplifier having an individual stage value of $f_2 = 2.5$ MHz.

30. A four-stage amplifier has a lower 3-dB frequency for an individual stage of $f_1 = 40$ Hz. What is the value of f_1 for this full amplifier?

9.12 Square-Wave Testing

***31.** The application of a 10-mV, 100-kHz square wave to an amplifier resulted in the output waveform of Fig. 9.75.
a. Write the Fourier series expansion for the square wave through the ninth harmonic.
b. Determine the bandwidth of the amplifier to the accuracy available by the waveform of Fig. 9.75.
c. Calculate the low-cutoff frequency.

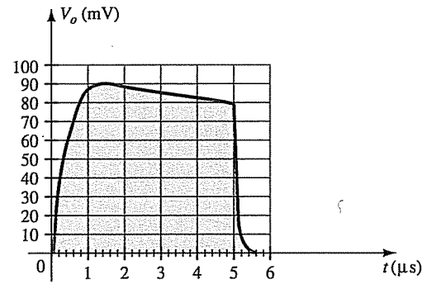


FIG. 9.75
Problem 31.

9.14 Computer Analysis

32. Using PSpice Windows, determine the frequency response of V_o/V_i for the high-pass filter of Fig. 9.68.

33. Using PSpice Windows, determine the frequency response of V_o/V_s for the BJT amplifier of Fig. 9.69.

34. Repeat Problem 33 for the network of Fig. 9.72 using Multisim.

35. Repeat Problem 33 for the JFET configuration of Fig. 9.73 using Multisim.

10 Operational Amplifiers

CHAPTER OUTLINE

10.1 Introduction
10.2 Differential Amplifier Circuit
10.3 BiFET, BiMOS, and CMOS Differential Amplifier Circuits
10.4 Op-Amp Basics
10.5 Practical Op-Amp Circuits
10.6 Op-Amp Specifications—DC Offset Parameters
10.7 Op-Amp Specifications—Frequency Parameters
10.8 Op-Amp Unit Specifications
10.9 Differential and Common-Mode Operation
10.10 Summary
10.11 Computer Analysis

10.1 INTRODUCTION

An operational amplifier, or op-amp, is a very high gain differential amplifier with high input impedance and low output impedance. Typical uses of the operational amplifier are to provide voltage amplitude changes (amplitude and polarity), oscillators, filter circuits, and many types of instrumentation circuits. An op-amp contains a number of differential amplifier stages to achieve a very high voltage gain.

Figure 10.1 shows a basic op-amp with two inputs and one output as would result using a differential amplifier input stage. Each input results in either the same or an opposite polarity (or phase) output, depending on whether the signal is applied to the plus (+) or the minus (−) input, respectively.

Single-Ended Input

Single-ended input operation results when the input signal is connected to one input with the other input connected to ground. Figure 10.2 shows the signals connected for this operation. In Fig. 10.2a, the input is applied to the plus input (with minus input at ground), which results in an output having the same polarity as the applied input signal. Figure 10.2b shows an input signal applied to the minus input, the output then being opposite in phase to the applied signal.

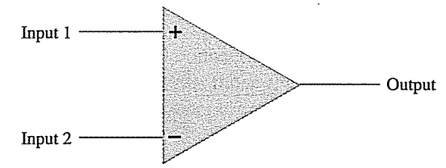


FIG. 10.1
Basic op-amp.

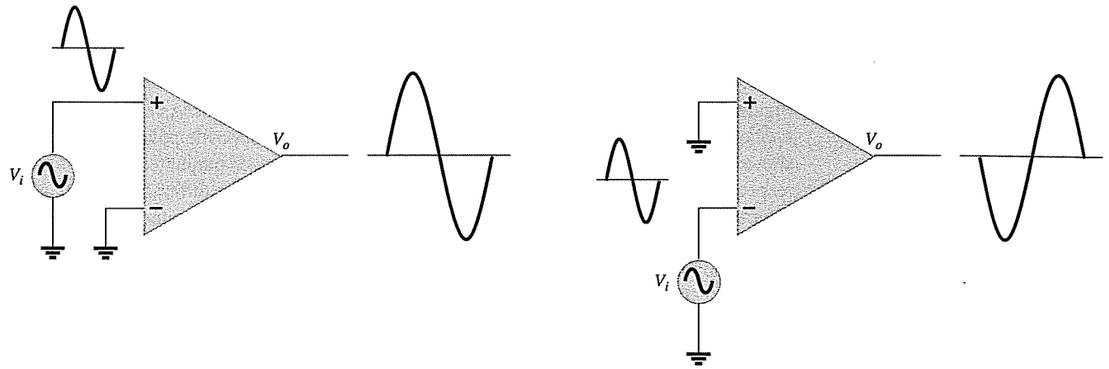


FIG. 10.2
Single-ended operation.

Multisim

Double-Ended (Differential) Input

In addition to using only one input, it is possible to apply signals at each input—this being a double-ended operation. Figure 10.3a shows an input, V_d, applied between the two input terminals (recall that neither input is at ground), with the resulting amplified output in phase with that applied between the plus and minus inputs. Figure 10.3b shows the same action resulting when two separate signals are applied to the inputs, the difference signal being $V_{i_1} - V_{i_2}$.

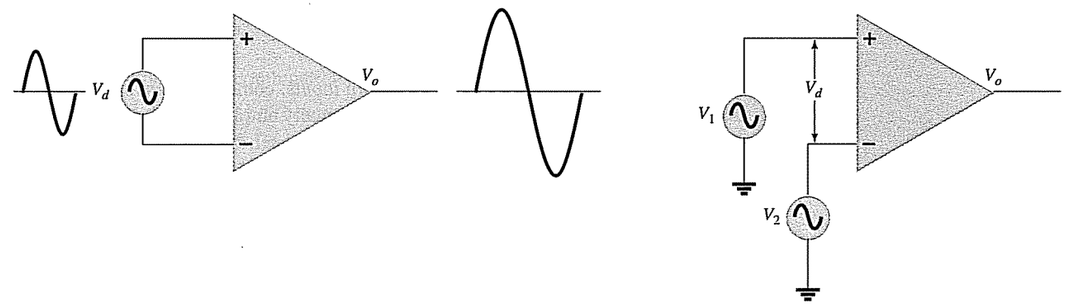


FIG. 10.3
Double-ended (differential) operation.

Double-Ended Output

Whereas the operation discussed so far has a single output, the op-amp can also be operated with opposite outputs, as shown in Fig. 10.4. An input applied to either input will result in outputs from both output terminals, these outputs always being opposite in polarity.

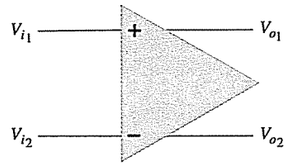


FIG. 10.4
Double-ended output.

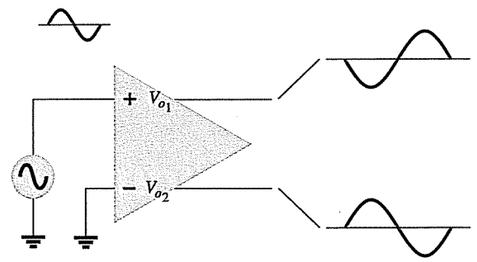


FIG. 10.5
Double-ended output with single-ended input.

Figure 10.5 shows a single-ended input with a double-ended output. As shown, the signal applied to the plus input results in two amplified outputs of opposite polarity. Figure 10.6 shows the same operation with a single output measured between output terminals (not with respect to ground). This difference output signal is $V_{o_1} - V_{o_2}$. The difference output is also referred to as a *floating signal* since neither output terminal is the ground (reference) terminal. Notice that the difference output is twice as large as either V_{o_1} or V_{o_2} because they are of opposite polarity and subtracting them results in twice their amplitude [e.g., $10\text{ V} - (-10\text{ V}) = 20\text{ V}$]. Figure 10.7 shows a differential input, differential output operation. The input is applied between the two input terminals and the output taken from between the two output terminals. This is fully differential operation.

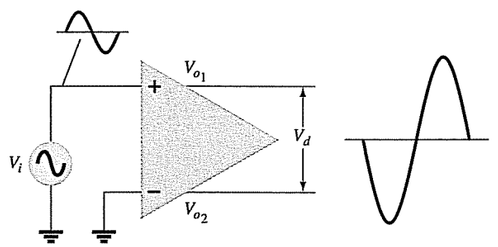


FIG. 10.6
Double-ended output.

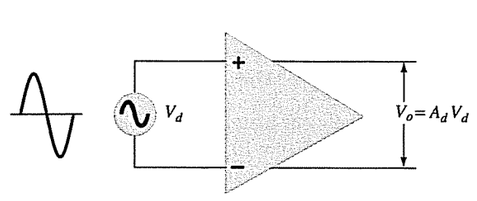


FIG. 10.7
Differential-input, differential-output operation.

Common-Mode Operation

When the same input signals are applied to both inputs, common-mode operation results, as shown in Fig. 10.8. Ideally, the two inputs are equally amplified, and since they result in opposite-polarity signals at the output, these signals cancel, resulting in 0-V output. Practically, a small output signal will result.

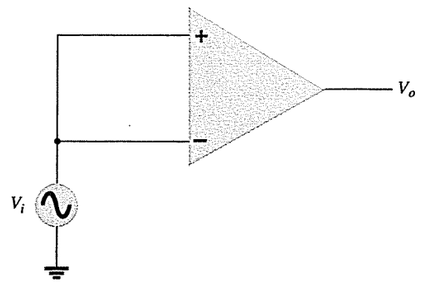


FIG. 10.8
Common-mode operation.

Common-Mode Rejection

A significant feature of a differential connection is that the signals that are opposite at the inputs are highly amplified, whereas those that are common to the two inputs are only slightly amplified—the overall operation being to amplify the difference signal while rejecting the common signal at the two inputs. Since noise (any unwanted input signal) is generally common to both inputs, the differential connection tends to provide attenuation of this unwanted input while providing an amplified output of the difference signal applied to the inputs. This operating feature is referred to as *common-mode rejection.*

10.2 DIFFERENTIAL AMPLIFIER CIRCUIT

The differential amplifier circuit is an extremely popular connection used in IC units. This connection can be described by considering the basic differential amplifier shown in Fig. 10.9. Notice that the circuit has two separate inputs and two separate outputs, and that the emitters are connected together. Whereas most differential amplifier circuits use two separate voltage supplies, the circuit can also operate using a single supply.

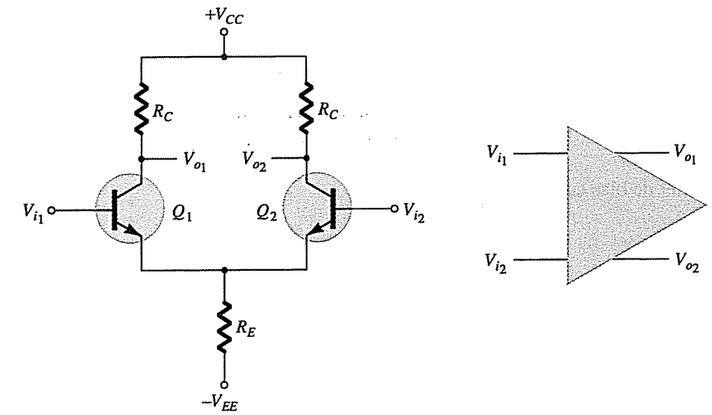


FIG. 10.9
Basic differential amplifier circuit.

A number of input signal combinations are possible:

If an input signal is applied to either input with the other input connected to ground, the operation is referred to as "single-ended."

If two opposite-polarity input signals are applied, the operation is referred to as "double-ended."

If the same input is applied to both inputs, the operation is called "common-mode."

In single-ended operation, a single input signal is applied. However, due to the common-emitter connection, the input signal operates both transistors, resulting in output from *both* collectors.

In double-ended operation, two input signals are applied, the difference of the inputs resulting in outputs from both collectors due to the difference of the signals applied to both inputs.

In common-mode operation, the common input signal results in opposite signals at each collector, these signals canceling, so that the resulting output signal is zero. As a practical matter, the opposite signals do not completely cancel, and a small signal results.

The main feature of the differential amplifier is the very large gain when opposite signals are applied to the inputs as compared to the very small gain resulting from common inputs. The ratio of this difference gain to the common gain is called *common-mode rejection.*

DC Bias

Let's first consider the dc bias operation of the circuit of Fig. 10.9. With ac inputs obtained from voltage sources, the dc voltage at each input is essentially connected to 0 V, as shown in Fig. 10.10. With each base voltage at 0 V, the common-emitter dc bias voltage is

$$V_E = 0\,\text{V} - V_{BE} = -0.7\,\text{V}$$

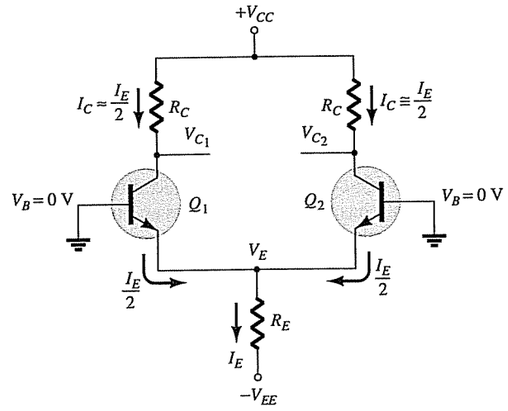


FIG. 10.10
DC bias of differential amplifier circuit.

The emitter dc bias current is then

$$I_E = \frac{V_E - (-V_{EE})}{R_E} \approx \frac{V_{EE} - 0.7\,\text{V}}{R_E} \qquad \textbf{(10.1)}$$

Assuming that the transistors are well matched (as would occur in an IC unit), we obtain

$$I_{C_1} = I_{C_2} = \frac{I_E}{2} \qquad \textbf{(10.2)}$$

resulting in a collector voltage of

$$V_{C_1} = V_{C_2} = V_{CC} - I_C R_C = V_{CC} - \frac{I_E}{2} R_C \qquad \textbf{(10.3)}$$



EXAMPLE 10.1 Calculate the dc voltages and currents in the circuit of Fig. 10.11.

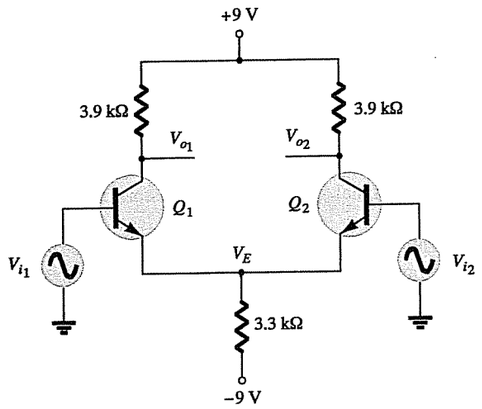


FIG. 10.11
Differential amplifier circuit for Example 10.1.

Solution:

$$\text{Eq. (10.1):}\quad I_E = \frac{V_{EE} - 0.7\,\text{V}}{R_E} = \frac{9\,\text{V} - 0.7\,\text{V}}{3.3\,\text{k}\Omega} \approx \mathbf{2.5\,mA}$$

The collector current is then

$$\text{Eq. (10.2):}\quad I_C = \frac{I_E}{2} = \frac{2.5\,\text{mA}}{2} = \mathbf{1.25\,mA}$$

resulting in a collector voltage of

$$\text{Eq. (10.3):}\quad V_C = V_{CC} - I_C R_C = 9\,\text{V} - (1.25\,\text{mA})(3.9\,\text{k}\Omega) \approx \mathbf{4.1\,V}$$

The common-emitter voltage is thus −0.7 V, whereas the collector bias voltage is near 4.1 V for both outputs.

AC Operation of Circuit

An ac connection of a differential amplifier is shown in Fig. 10.12. Separate input signals are applied as V_{i_1} and V_{i_2}, with separate outputs resulting as V_{o_1} and V_{o_2}. To carry out ac analysis, we redraw the circuit in Fig. 10.13. Each transistor is replaced by its ac equivalent.

Single-Ended AC Voltage Gain To calculate the single-ended ac voltage gain, V_o/V_i, apply signal to one input with the other connected to ground, as shown in Fig. 10.14. The ac

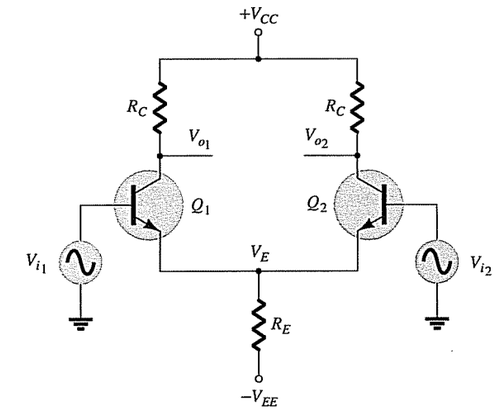


FIG. 10.12
AC connection of differential amplifier.

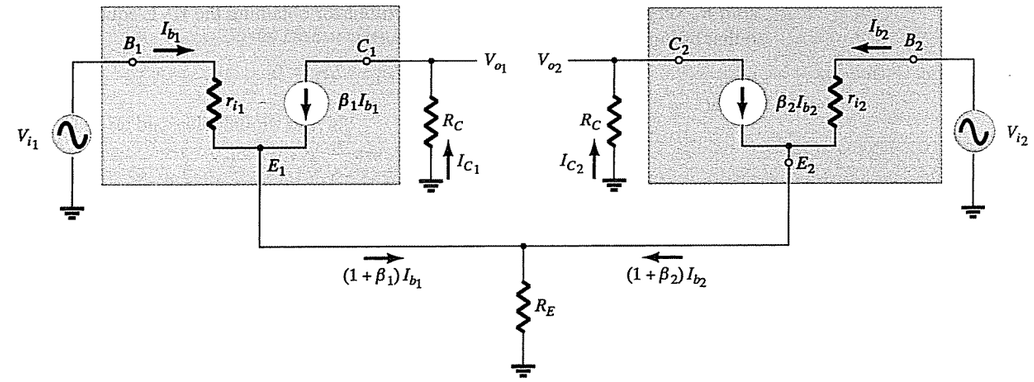


FIG. 10.13
AC equivalent of differential amplifier circuit.

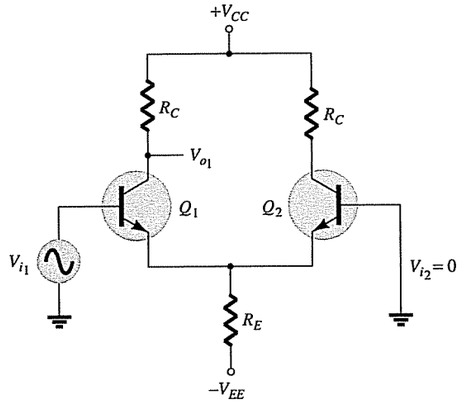


FIG. 10.14
Connection to calculate $A_{v_1} = V_{o_1}/V_{i_1}$.

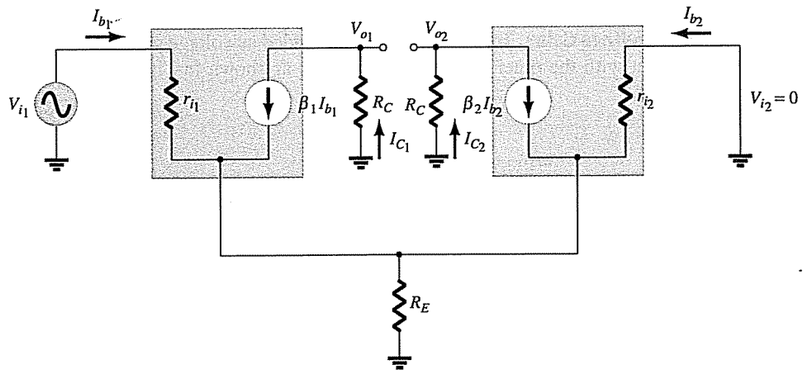


FIG. 10.15
AC equivalent of circuit in Fig. 10.14.

equivalent of this connection is drawn in Fig. 10.15. The ac base current can be calculated using the base 1 input Kirchhoff voltage loop (KVL) equation. If one assumes that the two transistors are well matched, then

$$I_{b_1} = I_{b_2} = I_b$$
$$r_{i_1} = r_{i_2} = r_i$$

With R_E very large (ideally infinite), the circuit for obtaining the KVL equation simplifies to that of Fig. 10.16, from which we can write

$$V_{i_1} - I_b r_i - I_b r_i = 0$$

so that

$$I_b = \frac{V_{i_1}}{2r_i}$$

If we also assume that

$$\beta_1 = \beta_2 = \beta$$

then

$$I_C = \beta I_b = \beta \frac{\beta V_{i_1}}{2r_i}$$

and the output voltage magnitude at either collector is

$$V_o = I_C R_C = \beta \frac{V_{i_1}}{2r_1} R_C = \frac{\beta R_C}{2\beta r_e} V_i$$

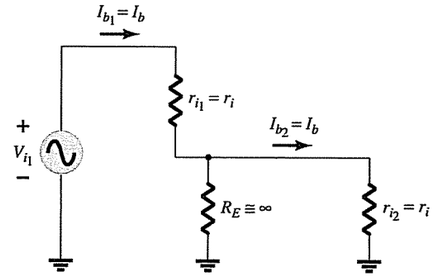


FIG. 10.16
Partial circuit for calculating I_b.

for which the single-ended voltage gain magnitude at either collector is

$$\boxed{A_v = \frac{V_o}{V_{i_1}} = \frac{R_C}{2r_e}} \qquad \textbf{(10.4)}$$

EXAMPLE 10.2 Calculate the single-ended output voltage V_{o_1} for the circuit of Fig. 10.17.



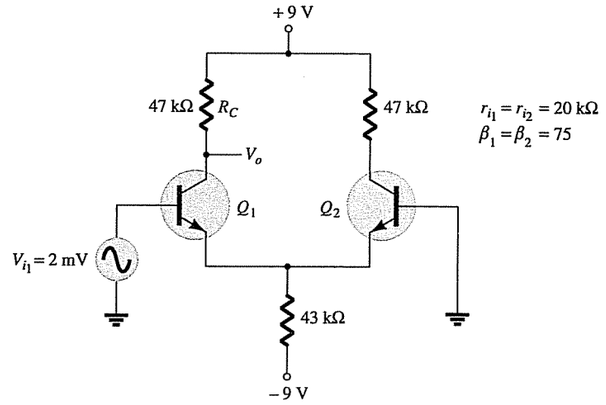


FIG. 10.17
Circuit for Examples 10.2 and 10.3.

Solution: The dc bias calculations provide

$$I_E = \frac{V_{EE} - 0.7\,\text{V}}{R_E} = \frac{9\,\text{V} - 0.7\,\text{V}}{43\,\text{k}\Omega} = 193\,\mu\text{A}$$

The collector dc current is then

$$I_C = \frac{I_E}{2} = 96.5\,\mu\text{A}$$

so that $V_C = V_{CC} - I_C R_C = 9\,\text{V} - (96.5\,\mu\text{A})(47\,\text{k}\Omega) = 4.5\,\text{V}$

The value of r_e is

$$r_e = \frac{26}{0.0965} \cong 269\,\Omega$$

The ac voltage gain magnitude can be calculated using Eq. (10.31):

$$A_v = \frac{R_C}{2r_e} = \frac{(47\,\text{k}\Omega)}{2(269\,\Omega)} = 87.4$$

providing an output ac voltage of magnitude

$$V_o = A_v V_i = (87.4)(2\,\text{mV}) = 174.8\,\text{mV} = \mathbf{0.175\ V}$$

Double-Ended AC Voltage Gain A similar analysis can be used to show that for the condition of signals applied to both inputs, the differential voltage gain magnitude is

$$\boxed{A_d = \frac{V_o}{V_d} = \frac{\beta R_C}{2r_i}} \qquad \textbf{(10.5)}$$

where $V_d = V_{i_1} - V_{i_2}$.

Common-Mode Operation of Circuit

Whereas a differential amplifier provides large amplification of the difference signal applied to both inputs, it should also provide as small an amplification of the signal common to both inputs. An ac connection showing common input to both transistors is shown in Fig. 10.18. The ac equivalent circuit is drawn in Fig. 10.19, from which we can write

$$I_b = \frac{V_i - 2(\beta + 1)I_b R_E}{r_i}$$

which can be rewritten as

$$I_b = \frac{V_i}{r_i + 2(\beta + 1)R_E}$$

The output voltage magnitude is then

$$V_o = I_C R_C = \beta I_b R_C = \frac{\beta V_i R_C}{r_i + 2(\beta + 1)R_E}$$

providing a voltage gain magnitude of

$$\boxed{A_c = \frac{V_o}{V_i} = \frac{\beta R_C}{r_i + 2(\beta + 1)R_E}} \qquad \textbf{(10.6)}$$

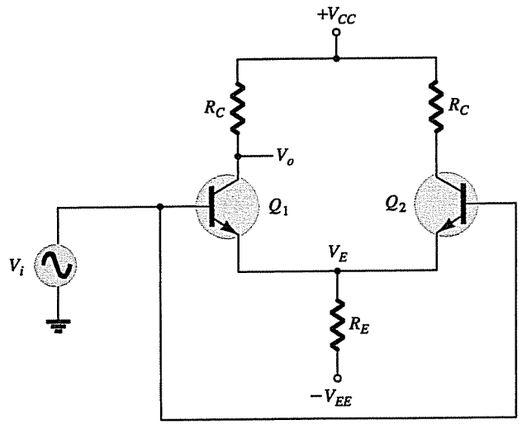


FIG. 10.18
Common-mode connection.

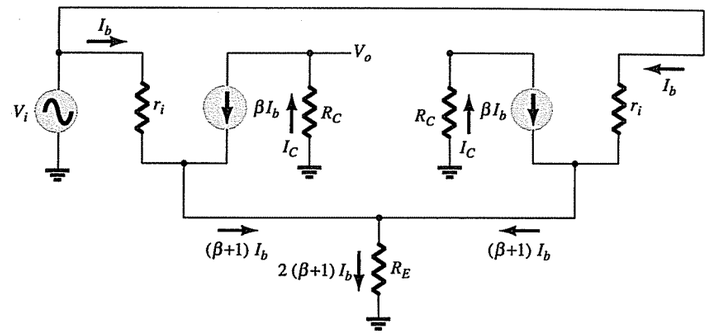


FIG. 10.19
AC circuit in common-mode connection.

EXAMPLE 10.3 Calculate the common-mode gain for the amplifier circuit of Fig. 10.17.

Solution:

Eq. (10.6): $$A_c = \frac{V_o}{V_i} = \frac{\beta R_C}{r_i + 2(\beta + 1)R_E} = \frac{75(47\,\text{k}\Omega)}{20\,\text{k}\Omega + 2(76)(43\,\text{k}\Omega)} = \mathbf{0.54}$$

PSpice

Use of Constant-Current Source

A good differential amplifier has a very large difference gain A_d, which is much larger than the common-mode gain A_c. The common-mode rejection ability of the circuit can be considerably improved by making the common-mode gain as small as possible (ideally, 0). From Eq. (10.6), we see that the larger R_E, the smaller is A_c. One popular method for increasing the ac value of R_E is using a constant-current source circuit. Figure 10.20 shows a differential amplifier with constant-current source to provide a large value of resistance from common emitter to ac ground. The major improvement of this circuit over that in Fig. 10.9 is the much larger ac impedance for R_E obtained using the constant-current source. Figure 10.21 shows the ac equivalent circuit for the circuit of Fig. 10.20. A practical constant-current source is shown as a high impedance, in parallel with the constant current.

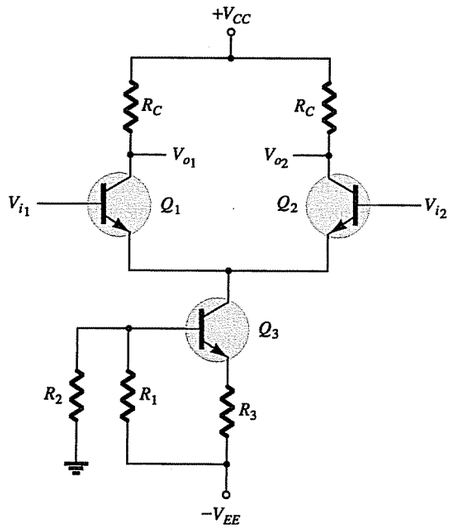


FIG. 10.20
Differential amplifier with constant-current source.

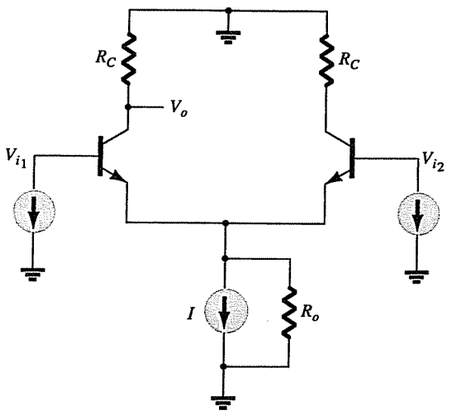


FIG. 10.21
AC equivalent of the circuit of Fig. 10.20.

EXAMPLE 10.4 Calculate the common-mode gain for the differential amplifier of Fig. 10.22.

PSpice

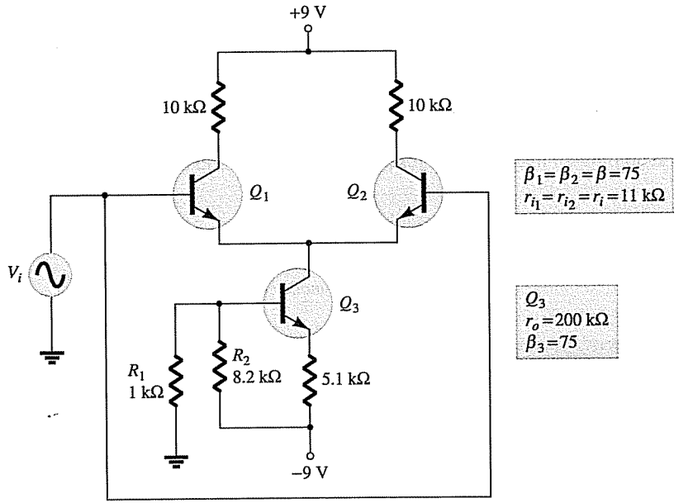


FIG. 10.22
Circuit for Example 10.4.

Solution: Using $R_E = r_o = 200\,\text{k}\Omega$ gives

$$A_c = \frac{\beta R_C}{r_i + 2(\beta + 1)R_E} = \frac{75(10\,\text{k}\Omega)}{11\,\text{k}\Omega + 2(76)(200\,\text{k}\Omega)} = \mathbf{24.7 \times 10^{-3}}$$

10.3 BIFET, BIMOS, AND CMOS DIFFERENTIAL AMPLIFIER CIRCUITS

Whereas the preceding section provided an introduction to the differential amplifier using bipolar devices, units commercially available also use JFET and MOSFET transistors to build these types of circuits. An IC unit containing a differential amplifier built using both bipolar (Bi) and junction field-effect (FET) transistors is referred to as a *BiFET circuit.* An IC unit made using both bipolar (Bi) and MOSFET (MOS) transistors is called a *BiMOS circuit.* Finally, a circuit built using opposite-type MOSFET transistors is a *CMOS circuit.*

The CMOS is a form of circuit popular in digital circuitry and uses both *n*-channel and *p*-channel enhancement MOSFET transistors (see Fig. 10.23). This complementary MOSFET or CMOS circuit uses these opposite (or complementary)-type transistors. The input V_i is applied to both gates with the output taken from the connected drains. Before going into the operation of the CMOS circuit, let's review the operation of the enhancement MOSFET transistors.

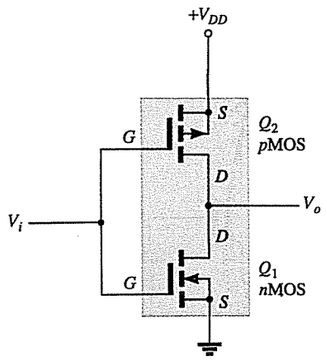


FIG. 10.23
CMOS inverter circuit.

*n*MOS On/Off Operation

The drain characteristic of an *n*-channel enhancement MOSFET or *n*MOS transistor is shown in Fig. 10.24a. With 0 V applied to the gate–source, there is no drain current. Not until V_{GS} is raised past the device threshold level V_T does any current result. With an input of, say, +5 V, the *n*MOS device is fully on with current I_D present. In summary:

An input of 0 V leaves the nMOS "off," whereas an input of +5V turns the nMOS on.

*p*MOS On/Off Operation

The drain characteristic for a *p*-channel MOSFET or *p*MOS transistor is shown in Fig. 10.24b. When 0 V is applied, the device is "off" (no drain current present), whereas for an input of −5 V (greater than the threshold voltage), the device is "on" with drain current

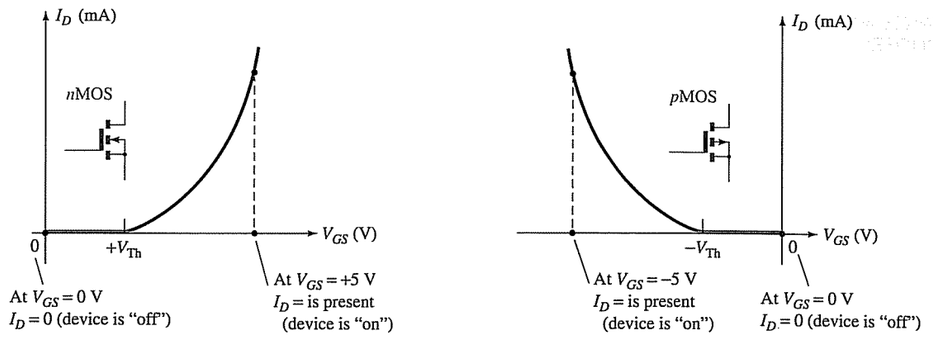


FIG. 10.24
Enhancement MOSFET characteristic showing off and on conditions: (a) nMOS; (b) pMOS.

present. In summary:

V_{GS} = 0 V leaves pMOS "off;" V_{GS} = −5 V turns pMOS on.

Consider next how the actual CMOS circuit of Fig. 10.25 operates for input of 0 V or +5 V.

0-V Input

When 0 V is applied as input to the CMOS circuit, it provides 0 V to both *n*MOS and *p*MOS gates. Figure 10.25a shows that

$$\text{For } n\text{MOS } (Q_1): \quad V_{GS} = V_i - 0\,\text{V} = 0\,\text{V} - 0\,\text{V} = 0\,\text{V}$$
$$\text{For } p\text{MOS } (Q_2): \quad V_{GS} = V_i - (+5\,\text{V}) = 0\,\text{V} - 5\,\text{V} = -5\,\text{V}$$

Input of 0 V to an *n*MOS transistor Q_1 leaves that device "off." The same 0-V input, however, results in the gate–source voltage of *p*MOS transistor Q_2 being −5 V (gate at 0 V is 5 V less than source at +5 V), resulting in that device turning on. The output, V_o, is then +5 V.

+5-V Input

When V_i = +5 V, it provides +5 V to both gates. Figure 10.25b shows that

$$\text{For } n\text{MOS } (Q_1): \quad V_{GS} = V_i - 0\,\text{V} = +5\,\text{V} - 0\,\text{V} = +5\,\text{V}$$
$$\text{For } p\text{MOS } (Q_2): \quad V_{GS} = V_i - (+5\,\text{V}) = +5\,\text{V} - 5\,\text{V} = 0\,\text{V}$$

This input results in transistor Q_1 being turned on and transistor Q_2 remaining off, the output then near 0 V, through conducting transistor Q_2. The CMOS connection of Fig. 10.23 provides operation as a logic inverter with V_o the opposite of V_i, as shown in Table 10.1.

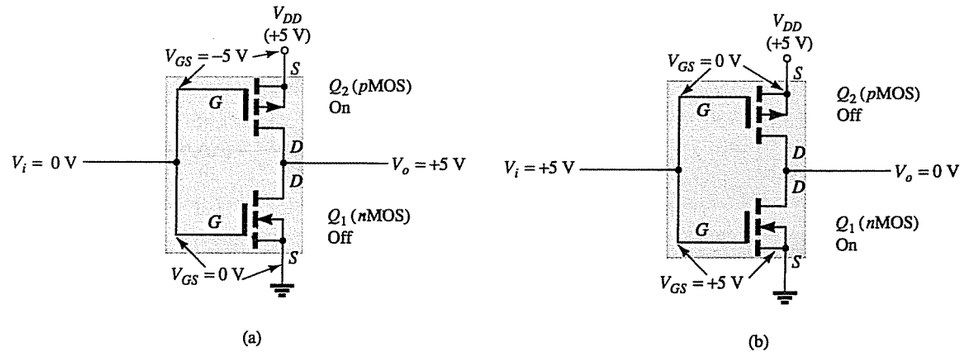


FIG. 10.25
Operation of CMOS circuit: (a) output +5 V; (b) output 0 V.

TABLE 10.1
Operation of CMOS Circuit

V_i (V)	Q_1	Q_2	V_o (V)
0	Off	On	+5
+5	On	Off	0

The circuits used below to show the various multidevice circuits are mostly symbolic, since the actual circuits used in ICs are much more complex. Figure 10.26 shows a BiFET circuit with JFET transistors at the inputs and bipolar transistors to provide the current source (using a current mirror circuit). The current mirror ensures that each JFET is operated at the same bias current. For ac operation, the JFET provides a high input impedance (much higher than that provided using only bipolar transistors).

Figure 10.27 shows a circuit using MOSFET input transistors and bipolar transistors for the current sources, the BiMOS unit providing even higher input impedance than the BiFET due to the use of MOSFET transistors.

Finally, a differential amplifier circuit can be built using complementary MOSFET transistors as shown in Fig. 10.28. The *p*MOS transistors provide the opposite inputs, whereas the *n*MOS transistors operate as the constant-current source. A single output is

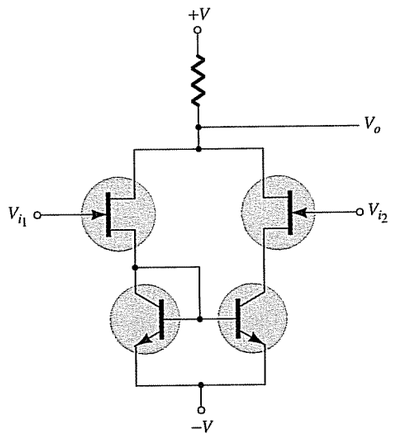


FIG. 10.26
BiFET differential amplifier circuit.

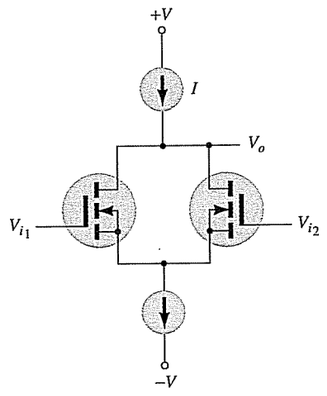


FIG. 10.27
BiMOS differential amplifier circuit.

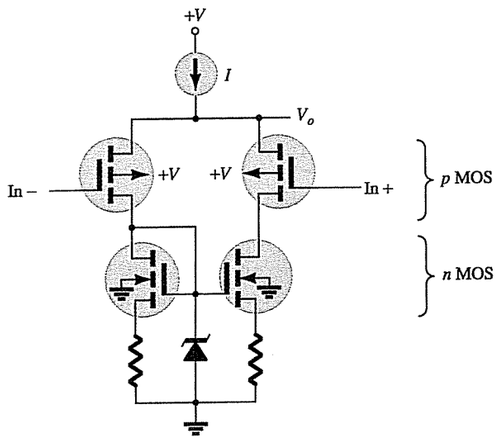


FIG. 10.28
CMOS differential amplifier.

taken from the common point between *n*MOS and *p*MOS transistors on one side of the circuit. This type of CMOS differential amplifier is particularly well suited for battery operation due to the low power dissipation of a CMOS circuit.

10.4 OP-AMP BASICS

An operational amplifier is a very high gain amplifier having very high input impedance (typically a few megohms) and low output impedance (less than 100 Ω). The basic circuit is made using a difference amplifier having two inputs (plus and minus) and at least one output. Figure 10.29 shows a basic op-amp unit. As discussed earlier, the plus (+) input produces an output that is in phase with the signal applied, whereas an input to the minus (−) input results in an opposite-polarity output. The ac equivalent circuit of the op-amp is shown in Fig. 10.30a. As shown, the input signal applied between input terminals sees an input impedance R_i that is typically very high. The output voltage is shown to be the amplifier gain times the input signal taken through an output impedance R_o, which is typically very low. An ideal op-amp circuit, as shown in Fig. 10.30b, would have infinite input impedance, zero output impedance, and infinite voltage gain.

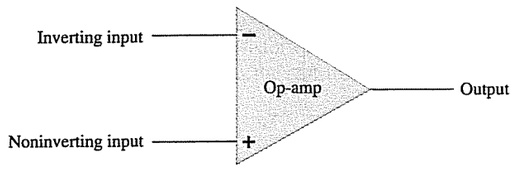


FIG. 10.29
Basic op-amp.

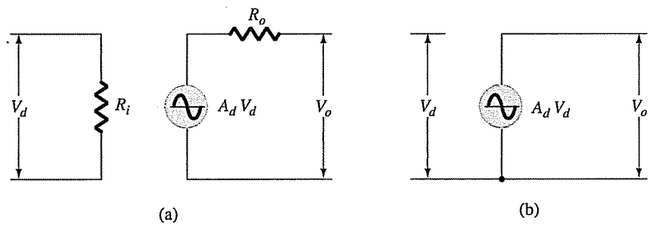


FIG. 10.30
AC equivalent of op-amp circuit: (a) practical; (b) ideal.

Basic Op-Amp

The basic circuit connection using an op-amp is shown in Fig. 10.31. The circuit shown provides operation as a constant-gain multiplier. An input signal V_1 is applied through resistor R_1 to the minus input. The output is then connected back to the same minus input through resistor R_f. The plus input is connected to ground. Since the signal V_1 is essentially applied to the minus input, the resulting output is opposite in phase to the input signal. Figure 10.32a shows the op-amp replaced by its ac equivalent circuit. If we use the ideal

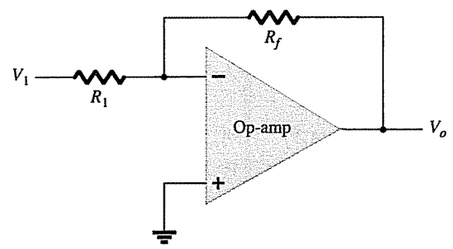


FIG. 10.31
Basic op-amp connection.

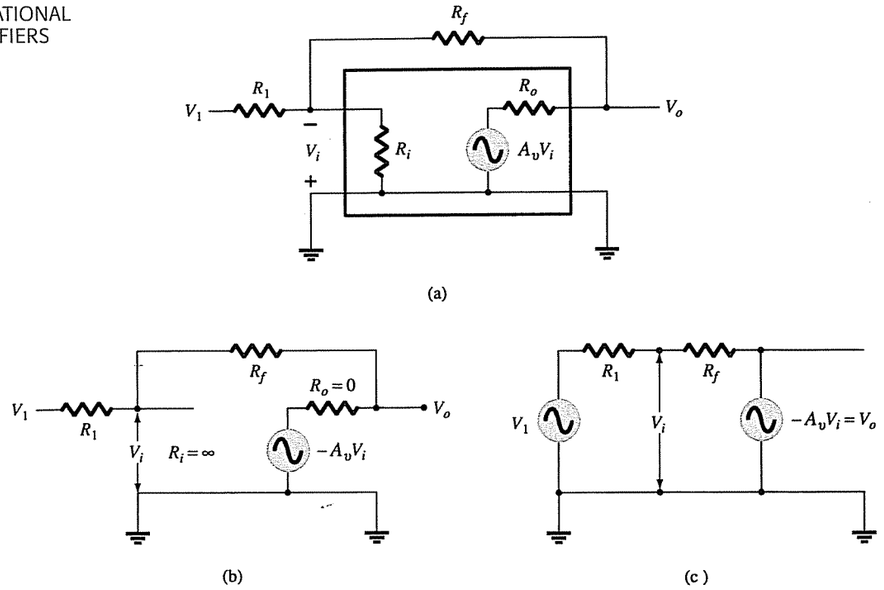


FIG. 10.32
Operation of op-amp as constant-gain multiplier: (a) op-amp ac equivalent circuit; (b) ideal op-amp equivalent circuit; (c) redrawn equivalent circuit.

op-amp equivalent circuit, replacing R_i by an infinite resistance and R_o by a zero resistance, the ac equivalent circuit is that shown in Fig. 10.32b. The circuit is then redrawn, as shown in Fig. 10.32c, from which circuit analysis is carried out.

Using superposition, we can solve for the voltage V_1 in terms of the components due to each of the sources. For source V_1 only ($-A_vV_i$ set to zero),

$$V_{i_1} = \frac{R_f}{R_1 + R_f} V_1$$

For source $-A_vV_i$ only (V_1 set to zero),

$$V_{i_2} = \frac{R_1}{R_1 + R_f}(-A_vV_i)$$

The total voltage V_i is then

$$V_i = V_{i_1} + V_{i_2} = \frac{R_f}{R_1 + R_f} V_1 + \frac{R_1}{R_1 + R_f}(-A_vV_i)$$

which can be solved for V_i as

$$V_i = \frac{R_f}{R_f + (1 + A_v)R_1} V_1 \tag{10.7}$$

If $A_v \gg 1$ and $A_vR_1 \gg R_f$, as is usually true, then

$$V_i = \frac{R_f}{A_vR_1} V_1$$

Solving for V_o/V_i, we get

$$\frac{V_o}{V_i} = \frac{-A_vV_i}{V_i} = \frac{-A_v}{V_i}\frac{R_fV_1}{A_vR_1} = -\frac{R_f}{R_1}\frac{V_1}{V_i}$$

so that

$$\boxed{\frac{V_o}{V_1} = -\frac{R_f}{R_1}} \tag{10.8}$$

The result in Eq. (10.8) shows that the ratio of overall output to input voltage is dependent only on the values of resistors R_1 and R_f—provided that A_v is very large.

Unity Gain

If $R_f = R_1$, the gain is

$$\text{Voltage gain} = -\frac{R_f}{R_1} = -1$$

so that the circuit provides a unity voltage gain with 180° phase inversion. If R_f is exactly R_1, the voltage gain is exactly 1.

Constant-Magnitude Gain

If R_f is some multiple of R_1, the overall amplifier gain is a constant. For example, if $R_f = 10R_1$, then

$$\text{Voltage gain} = -\frac{R_f}{R_1} = -10$$

and the circuit provides a voltage gain of exactly 10 along with an 180° phase inversion from the input signal. If we select precise resistor values for R_f and R_1, we can obtain a wide range of gains, the gain being as accurate as the resistors used and is only slightly affected by temperature and other circuit factors.

Virtual Ground

The output voltage is limited by the supply voltage of, typically, a few volts. As stated before, voltage gains are very high. If, for example, $V_o = -10$ V and $A_v = 20{,}000$, the input voltage is

$$V_i = \frac{-V_o}{A_v} = \frac{10\text{ V}}{20{,}000} = 0.5\text{ mV}$$

If the circuit has an overall gain (V_o/V_1) of, say, 1, the value of V_1 is 10 V. Compared to all other input and output voltages, the value of V_i is then small and may be considered 0 V.

Note that although $V_i \approx 0$ V, it is not exactly 0 V. (The output voltage is a few volts due to the very small input V_i times a very large gain A_v.) The fact that $V_i \approx 0$ V leads to the concept that at the amplifier input there exists a virtual short-circuit or virtual ground.

The concept of a virtual short implies that although the voltage is nearly 0 V, there is no current through the amplifier input to ground. Figure 10.33 depicts the virtual ground concept. The heavy line is used to indicate that we may consider that a short exists with $V_i \approx 0$ V but that this is a virtual short so that no current goes through the short to ground. Current goes only through resistors R_1 and R_f as shown.

Using the virtual ground concept, we can write equations for the current I as follows:

$$I = \frac{V_1}{R_1} = -\frac{V_o}{R_f}$$

which can be solved for V_o/V_1:

$$\frac{V_o}{V_1} = -\frac{R_f}{R_1}$$

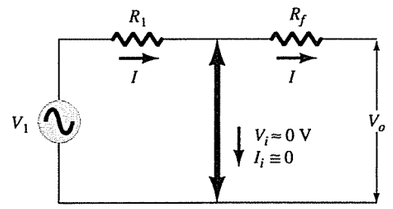


FIG. 10.33
Virtual ground in an op-amp.

The virtual ground concept, which depends on A_v being very large, allowed a simple solution to determine the overall voltage gain. It should be understood that although the circuit of Fig. 10.33 is not physically correct, it does allow an easy means for determining the overall voltage gain.

10.5 PRACTICAL OP-AMP CIRCUITS

The op-amp can be connected in a large number of circuits to provide various operating characteristics. In this section, we cover a few of the most common of these circuit connections.

Inverting Amplifier

The most widely used constant-gain amplifier circuit is the inverting amplifier, as shown in Fig. 10.34. The output is obtained by multiplying the input by a fixed or constant gain, set by the input resistor (R_1) and feedback resistor (R_f)—this output also being inverted from the input. Using Eq. (10.8), we can write

$$V_o = -\frac{R_f}{R_1}V_1$$

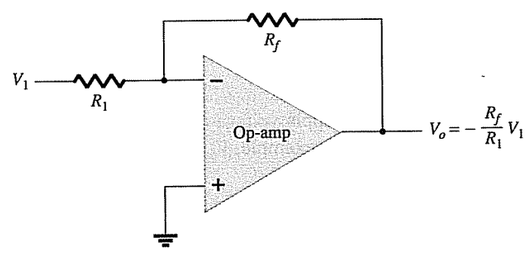


FIG. 10.34
Inverting constant-gain multiplier.

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EXAMPLE 10.5 If the circuit of Fig. 10.34 has $R_1 = 100\,\text{k}\Omega$ and $R_f = 500\,\text{k}\Omega$, what output voltage results for an input of $V_1 = 2\,\text{V}$?

Solution:

$$\text{Eq. (10.8):} \quad V_o = -\frac{R_f}{R_1}V_1 = -\frac{500\,\text{k}\Omega}{100\,\text{k}\Omega}(2\,\text{V}) = \mathbf{-10\,V}$$

Noninverting Amplifier

The connection of Fig. 10.35a shows an op-amp circuit that works as a noninverting amplifier or constant-gain multiplier. It should be noted that the inverting amplifier connection is more widely used because it has better frequency stability (discussed later). To determine the voltage gain of the circuit, we can use the equivalent representation shown in Fig. 10.35b. Note that the voltage across R_1 is V_1 since $V_i \approx 0\,\text{V}$. This must be equal to the output voltage, through a voltage divider of R_1 and R_f, so that

$$V_1 = \frac{R_1}{R_1 + R_f}V_o$$

which results in

$$\boxed{\frac{V_o}{V_1} = \frac{R_1 + R_f}{R_1} = 1 + \frac{R_f}{R_1}} \qquad \textbf{(10.9)}$$

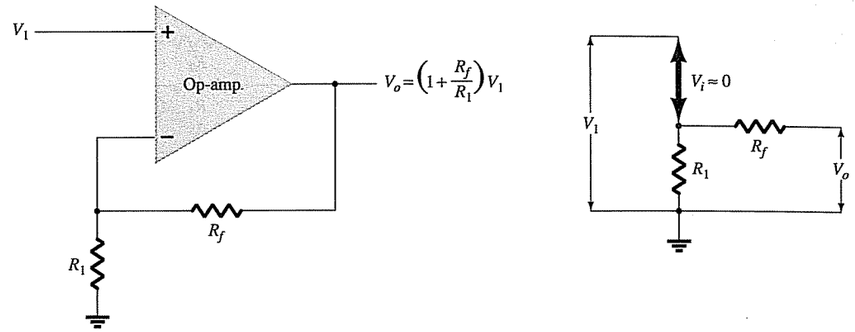


FIG. 10.35
Noninverting constant-gain multiplier.

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EXAMPLE 10.6 Calculate the output voltage of a noninverting amplifier (as in Fig. 10.35) for values of $V_1 = 2\,\text{V}$, $R_f = 500\,\text{k}\Omega$, and $R_1 = 100\,\text{k}\Omega$.

Solution:

$$\text{Eq. (10.9):} \quad V_o = \left(1 + \frac{R_f}{R_1}\right)V_1 = \left(1 + \frac{500\,\text{k}\Omega}{100\,\text{k}\Omega}\right)(2\,\text{V}) = 6(2\,\text{V}) = \mathbf{+12\,V}$$

Unity Follower

The unity-follower circuit, as shown in Fig. 10.36a, provides a gain of unity (1) with no polarity or phase reversal. From the equivalent circuit (see Fig. 10.36b) it is clear that

$$\boxed{V_o = V_1} \qquad \textbf{(10.10)}$$

and that the output is the same polarity and magnitude as the input. The circuit operates like an emitter- or source-follower circuit except that the gain is exactly unity.

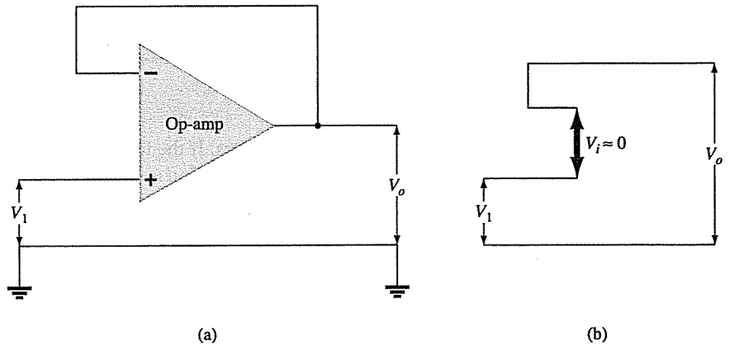


FIG. 10.36
(a) Unity follower; (b) virtual-ground equivalent circuit.

Summing Amplifier

Probably the most used of the op-amp circuits is the summing amplifier circuit shown in Fig. 10.37a. The circuit shows a three-input summing amplifier circuit, which provides a means of algebraically summing (adding) three voltages, each multiplied by a constant-gain

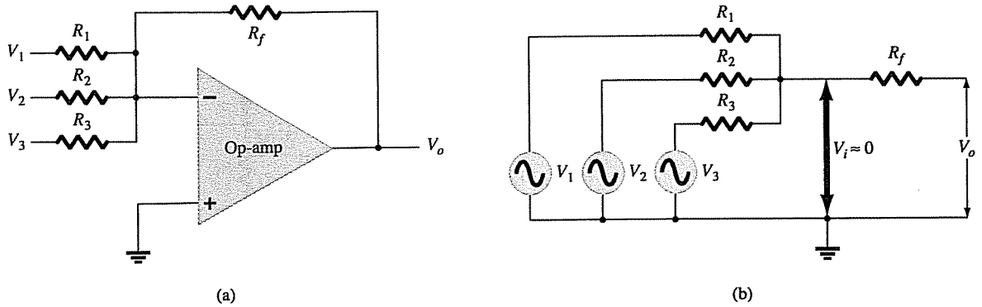


FIG. 10.37
(a) Summing amplifier; (b) virtual-ground equivalent circuit.

factor. Using the equivalent representation shown in Fig. 10.37b, we can express the output voltage in terms of the inputs as

$$V_o = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right) \tag{10.11}$$

In other words, each input adds a voltage to the output multiplied by its separate constant-gain multiplier. If more inputs are used, they each add an additional component to the output.

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EXAMPLE 10.7 Calculate the output voltage of an op-amp summing amplifier for the following sets of voltages and resistors. Use $R_f = 1\,\text{M}\Omega$ in all cases.

a. $V_1 = +1\,\text{V}, V_2 = +2\,\text{V}, V_3 = +3\,\text{V}, R_1 = 500\,\text{k}\Omega, R_2 = 1\,\text{M}\Omega, R_3 = 1\,\text{M}\Omega$.
b. $V_1 = -2\,\text{V}, V_2 = +3\,\text{V}, V_3 = +1\,\text{V}, R_1 = 200\,\text{k}\Omega, R_2 = 500\,\text{k}\Omega, R_3 = 1\,\text{M}\Omega$.

Solution: Using Eq. (10.11), we obtain

a. $$V_o = -\left[\frac{1000\,\text{k}\Omega}{500\,\text{k}\Omega}(+1\,\text{V}) + \frac{1000\,\text{k}\Omega}{1000\,\text{k}\Omega}(+2\,\text{V}) + \frac{1000\,\text{k}\Omega}{1000\,\text{k}\Omega}(+3\,\text{V})\right]$$
$$= -[2(1\,\text{V}) + 1(2\,\text{V}) + 1(3\,\text{V})] = \mathbf{-7\,V}$$

b. $$V_o = -\left[\frac{1000\,\text{k}\Omega}{200\,\text{k}\Omega}(-2\,\text{V}) + \frac{1000\,\text{k}\Omega}{500\,\text{k}\Omega}(+3\,\text{V}) + \frac{1000\,\text{k}\Omega}{1000\,\text{k}\Omega}(+1\,\text{V})\right]$$
$$= -[5(-2\,\text{V}) + 2(3\,\text{V}) + 1(1\,\text{V})] = \mathbf{+3\,V}$$

Integrator

So far, the input and feedback components have been resistors. If the feedback component used is a capacitor, as shown in Fig. 10.38a, the resulting connection is called an *integrator.* The virtual-ground equivalent circuit (Fig. 10.38b) shows that an expression for the voltage between input and output can be derived in terms of the current I from input to output. Recall that virtual ground means that we can consider the voltage at the junction of R and X_C to be ground (since $V_i \approx 0\,\text{V}$) but that no current goes into ground at that point. The capacitive impedance can be expressed as

$$X_C = \frac{1}{j\omega C} = \frac{1}{sC}$$

where $s = j\omega$ is in the Laplace notation.* Solving for V_o/V_1 yields

$$I = \frac{V_1}{R} = -\frac{V_o}{X_C} = \frac{-V_o}{1/sC} = -sCV_o$$

*Laplace notation allows expressing differential or integral operations, which are part of calculus, in algebraic form using the operator s. Readers unfamiliar with calculus should ignore the steps leading to Eq. (10.13) and follow the physical meaning used thereafter.

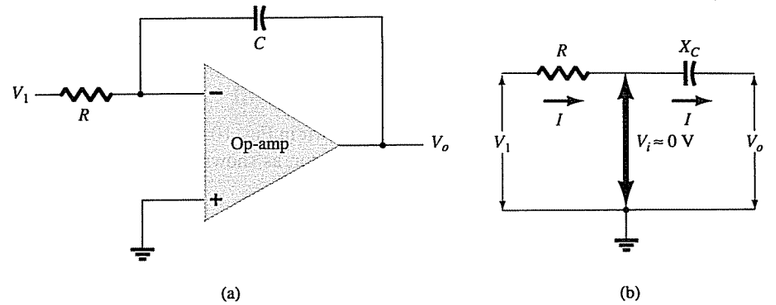


FIG. 10.38
Integrator.

$$\frac{V_o}{V_1} = \frac{-1}{sCR} \tag{10.12}$$

This expression can be rewritten in the time domain as

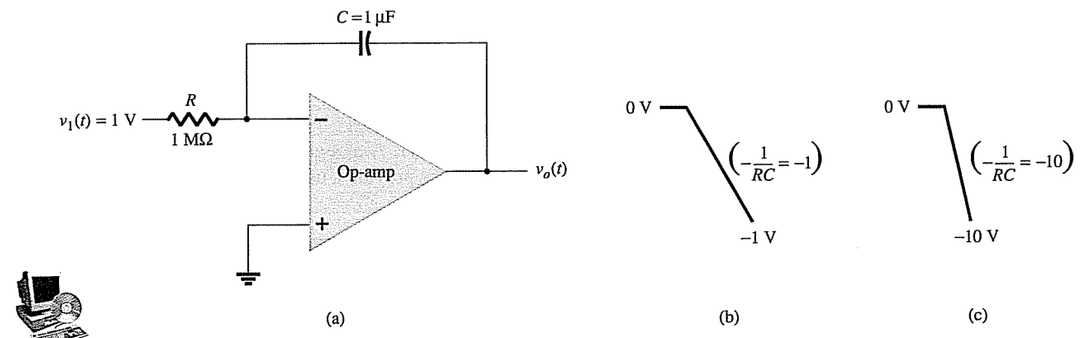
$$v_o(t) = -\frac{1}{RC}\int v_1(t)\,dt \tag{10.13}$$

Equation (10.13) shows that the output is the integral of the input, with an inversion and scale multiplier of $1/RC$. The ability to integrate a given signal provides the analog computer with the ability to solve differential equations and therefore provides the ability to electrically solve analogs of physical system operation.

The integration operation is one of summation, summing the area under a waveform or a curve over a period of time. If a fixed voltage is applied as input to an integrator circuit, Eq. (10.13) shows that the output voltage grows over a period of time, providing a ramp voltage. Equation (10.13) can thus be understood to show that the output voltage ramp (for a fixed input voltage) is opposite in polarity to the input voltage and is multiplied by the factor $1/RC$. Although the circuit of Fig. 10.38 can operate on many varied types of input signals, the following examples will use only a fixed input voltage, resulting in a ramp output voltage.

As an example, consider an input voltage $V_1 = 1\,\text{V}$ to the integrator circuit of Fig. 10.39a. The scale factor of $1/RC$ is

$$-\frac{1}{RC} = \frac{1}{(1\,\text{M}\Omega)(1\,\mu\text{F})} = -1$$



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FIG. 10.39
Operation of integrator with step input.

so that the output is a negative ramp voltage as shown in Fig. 10.39b. If the scale factor is changed by making $R = 100\,\text{k}\Omega$, for example, then

$$-\frac{1}{RC} = \frac{1}{(100\,\text{k}\Omega)(1\,\mu\text{F})} = -10$$

and the output is then a steeper ramp voltage, as shown in Fig. 10.39c.

More than one input may be applied to an integrator, as shown in Fig. 10.40, with the resulting operation given by

$$v_o(t) = -\left[\frac{1}{R_1C}\int v_1(t)\,dt + \frac{1}{R_2C}\int v_2(t)\,dt + \frac{1}{R_3C}\int v_3(t)\,dt\right] \qquad \textbf{(10.14)}$$

An example of a summing integrator as used in an analog computer is given in Fig. 10.40. The actual circuit is shown with input resistors and feedback capacitor, whereas the analog-computer representation indicates only the scale factor for each input.

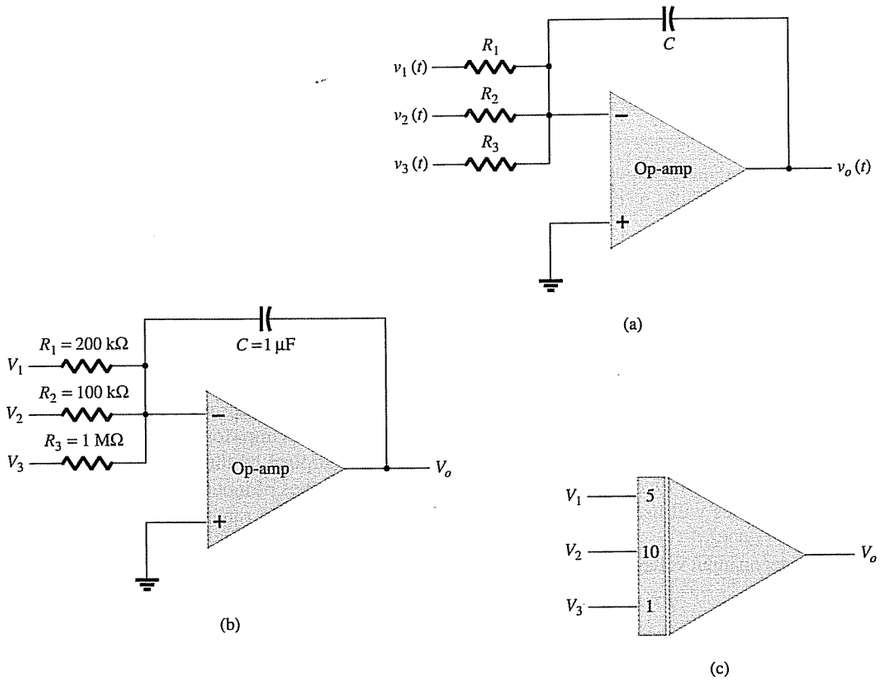


FIG. 10.40
(a) Summing-integrator circuit; (b) component values; (c) analog-computer, integrator-circuit representation.

Differentiator

A differentiator circuit is shown in Fig. 10.41. Although it is not as useful as the circuit forms covered above, the differentiator does provide a useful operation, the resulting relation for the circuit being

$$\boxed{v_o(t) = -RC\frac{dv_1(t)}{dt}} \qquad \textbf{(10.15)}$$

where the scale factor is $-RC$.

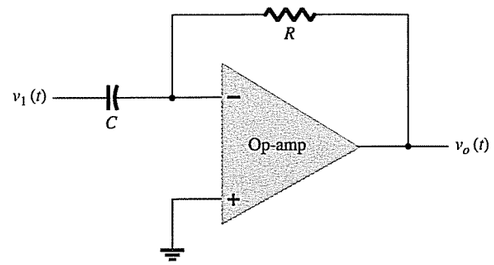


FIG. 10.41
Differentiator circuit.

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10.6 OP-AMP SPECIFICATIONS—DC OFFSET PARAMETERS

Before going into various practical applications using op-amps, we should become familiar with some of the parameters used to define the operation of the unit. These specifications include both dc and transient or frequency operating features, as covered next.

Offset Currents and Voltages

Although the op-amp output should be 0 V when the input is 0 V, in actual operation there is some offset voltage at the output. For example, if one connected 0 V to both op-amp inputs and then measured 26 mV(dc) at the output, this would represent 26 mV of unwanted voltage generated by the circuit and not by the input signal. Since the user may connect the amplifier circuit for various gain and polarity operations, however, the manufacturer specifies an input offset voltage for the op-amp. The output offset voltage is then determined by the input offset voltage and the gain of the amplifier, as connected by the user.

The output offset voltage can be shown to be affected by two separate circuit conditions: (1) an input offset voltage V_{IO} and (2) an offset current due to the difference in currents resulting at the plus (+) and minus (−) inputs.

Input Offset Voltage V_{IO} The manufacturer's specification sheet provides a value of V_{IO} for the op-amp. To determine the effect of this input voltage on the output, consider the connection shown in Fig. 10.42. Using $V_o = AV_i$, we can write

$$V_o = AV_i = A\left(V_{IO} - V_o\frac{R_1}{R_1 + R_f}\right)$$

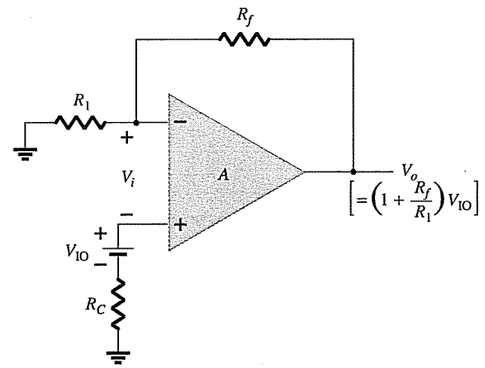


FIG. 10.42
Operation showing effect of input offset voltage V_{IO}.

Solving for V_o, we get

$$V_{o_y} = V_{IO}\frac{A}{1 + A\left[R_1/(R_1 + R_f)\right]} \approx V_{IO}\frac{A}{A\left[R_1/(R_1 + R_f)\right]}$$

from which we can write

$$\boxed{V_o(\text{offset}) = V_{IO}\frac{R_1 + R_f}{R_1}} \qquad \textbf{(10.16)}$$

Equation (10.16) shows how the output offset voltage results from a specified input offset voltage for a typical amplifier connection of the op-amp.

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EXAMPLE 10.8 Calculate the output offset voltage of the circuit in Fig. 10.43. The op-amp spec lists $V_{IO} = 1.2\,\text{mV}$.

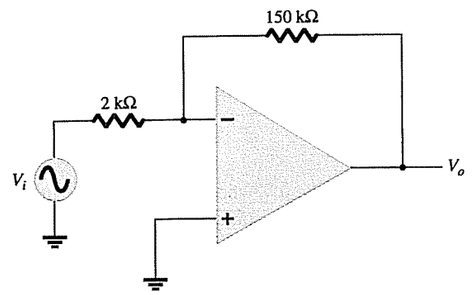


FIG. 10.43
Op-amp connection for Examples 10.8 and 10.9.

Solution:

Eq. (10.16): $V_o(\text{offset}) = V_{IO}\dfrac{R_1 + R_f}{R_1} = (1.2\,\text{mV})\left(\dfrac{2\,\text{k}\Omega + 150\,\text{k}\Omega}{2\,\text{k}\Omega}\right) = \mathbf{91.2\,mV}$

Output Offset Voltage Due to Input Offset Current I_{IO} An output offset voltage will also result due to any difference in dc bias currents at both inputs. Since the two input transistors are never exactly matched, each will operate at a slightly different current. For a typical op-amp connection, such as that shown in Fig. 10.44, an output offset voltage can be determined as follows. Replacing the bias currents through the input resistors by the voltage drop that each develops as shown in Fig. 10.45, we can determine the expression for

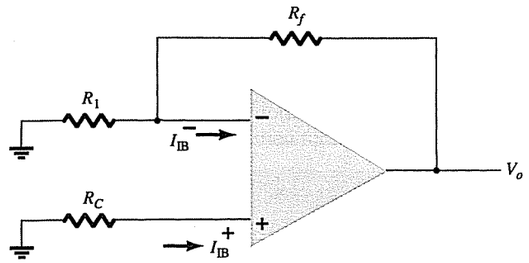


FIG. 10.44
Op-amp connection showing input bias currents.

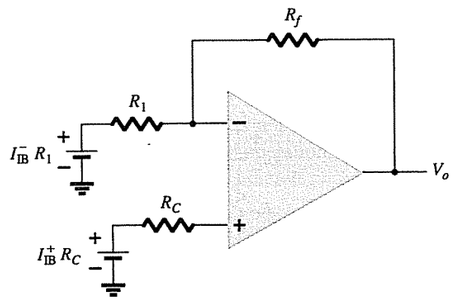


FIG. 10.45
Redrawn circuit of Fig. 10.44.

the resulting output voltage. Using superposition, we see that the output voltage due to input bias current I_{IB}^+, denoted by V_o^+, is given by

$$V_o^+ = I_{IB}^+ R_C\left(1 + \frac{R_f}{R_1}\right)$$

whereas the output voltage due to only I_{IB}^-, denoted by V_o^-, is given by

$$V_o^- = I_{IB}^- R_1\left(-\frac{R_f}{R_1}\right)$$

for a total output offset voltage of

$$V_o(\text{offset due to } I_{IB}^+ \text{ and } I_{IB}^-) = I_{IB}^+ R_C\left(1 + \frac{R_f}{R_1}\right) - I_{IB}^- R_1\frac{R_f}{R_1} \qquad \textbf{(10.17)}$$

Since the main consideration is the difference between the input bias currents rather than each value, we define the offset current I_{IO} by

$$I_{IO} = I_{IB}^+ - I_{IB}^-$$

Since the compensating resistance R_C is usually approximately equal to the value of R_1, using $R_C = R_1$ in Eq. (10.17), we can write

$$\begin{aligned} V_o(\text{offset}) &= I_{IB}^+(R_1 + R_f) - I_{IB}^- R_f \\ &= I_{IB}^+ R_f - I_{IB}^- R_f = R_f(I_{IB}^+ - I_{IB}^-) \end{aligned}$$

resulting in

$$\boxed{V_o(\text{offset due to } I_{IO}) = I_{IO} R_f} \qquad \textbf{(10.18)}$$

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EXAMPLE 10.9 Calculate the offset voltage for the circuit of Fig. 10.43 for op-amp specification listing $I_{IO} = 100\,\text{nA}$.

Solution: Eq. (10.18): $V_o = I_{IO} R_f = (100\,\text{nA})(150\,\text{k}\Omega) = \mathbf{15\,mV}$

Total Offset Due to V_{IO} and I_{IO} Since the op-amp output may have an output offset voltage due to both factors covered above, the total output offset voltage can be expressed as

$$|V_o(\text{offset})| = |V_o(\text{offset due to } V_{IO})| + |V_o(\text{offset due to } I_{IO})| \qquad \textbf{(10.19)}$$

The absolute magnitude is used to accommodate the fact that the offset polarity may be either positive or negative.

EXAMPLE 10.10 Calculate the total offset voltage for the circuit of Fig. 10.46 for an op-amp with specified values of input offset voltage $V_{IO} = 4\,\text{mV}$ and input offset current $I_{IO} = 150\,\text{nA}$.

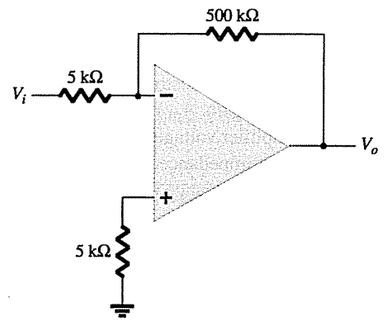


FIG. 10.46
Op-amp circuit for Example 10.10.

Solution: The offset due to V_{IO} is

$$\text{Eq. (10.16):}\quad V_o(\text{offset due to } V_{IO}) = V_{IO}\frac{R_1 + R_f}{R_1} = (4\text{ mV})\left(\frac{5\text{ k}\Omega + 500\text{ k}\Omega}{5\text{ k}\Omega}\right)$$
$$= 404\text{ mV}$$
$$\text{Eq. (10.18):}\quad V_o(\text{offset due to } I_{IO}) = I_{IO}R_f = (150\text{ nA})(500\text{ k}\Omega) = 75\text{ mV}$$

resulting in a total offset

$$\text{Eq. (10.19):}\quad V_o(\text{total offset}) = V_o(\text{offset due to } V_{IO}) + V_o(\text{offset due to } I_{IO})$$
$$= 404\text{ mV} + 75\text{ mV} = \mathbf{479\text{ mV}}$$

Input Bias Current, I_{IB} A parameter related to I_{IO} and the separate input bias currents I_{IB}^+ and I_{IB}^- is the average bias current defined as

$$I_{IB} = \frac{I_{IB}^+ + I_{IB}^-}{2} \qquad \textbf{(10.20)}$$

One could determine the separate input bias currents using the specified values I_{IO} and I_{IB}. It can be shown that for $I_{IB}^+ > I_{IB}^-$

$$I_{IB}^+ = I_{IB} + \frac{I_{IO}}{2} \qquad \textbf{(10.21)}$$

$$I_{IB}^- = I_{IB} - \frac{I_{IO}}{2} \qquad \textbf{(10.22)}$$

EXAMPLE 10.11 Calculate the input bias currents at each input of an op-amp having specified values of $I_{IO} = 5$ nA and $I_{IB} = 30$ nA.

Solution: Using Eq. (10.21), we obtain

$$I_{IB}^+ = I_{IB} + \frac{I_{IO}}{2} = 30\text{ nA} + \frac{5\text{ nA}}{2} = \mathbf{32.5\text{ nA}}$$

$$I_{IB}^- = I_{IB} - \frac{I_{IO}}{2} = 30\text{ nA} - \frac{5\text{ nA}}{2} = \mathbf{27.5\text{ nA}}$$

10.7 OP-AMP SPECIFICATIONS–FREQUENCY PARAMETERS

An op-amp is designed to be a high-gain, wide-bandwidth amplifier. This operation tends to be unstable (oscillate) due to positive feedback (see Chapter 14). To ensure stable operation, op-amps are built with internal compensation circuitry, which also causes the very high open-loop gain to diminish with increasing frequency. This gain reduction is referred to as *roll-off*. In most op-amps, roll-off occurs at a rate of 20 dB per decade (−20 dB/decade) or 6 dB per octave (−6 dB/octave). (Refer to Chapter 9 for introductory coverage of dB and frequency response.)

Note that although op-amp specifications list an open-loop voltage gain (A_{VD}), the user typically connects the op-amp using feedback resistors to reduce the circuit voltage gain to a much smaller value (closed-loop voltage gain, A_{CL}). A number of circuit improvements result from this gain reduction. First, the amplifier voltage gain is a more stable, precise value set by the external resistors; second, the input impedance of the circuit is increased over that of the op-amp alone; third, the circuit output impedance is reduced from that of the op-amp alone; and finally, the frequency response of the circuit is increased over that of the op-amp alone.

Gain–Bandwidth

Because of the internal compensation circuitry included in an op-amp, the voltage gain drops off as frequency increases. Op-amp specifications provide a description of the gain versus bandwidth. Figure 10.47 provides a plot of gain versus frequency for a typical op-amp. At low frequency down to dc operation the gain is that value listed by the manufacturer's

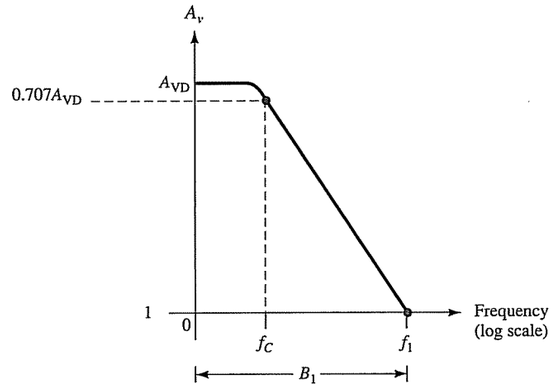


FIG. 10.47
Gain versus frequency plot.

specification A_{VD} (voltage differential gain) and is typically a very large value. As the frequency of the input signal increases, the open-loop gain drops off until it finally reaches the value of 1 (unity). The frequency at this gain value is specified by the manufacturer as the unity-gain bandwidth, B_1. Although this value is a frequency (see Fig. 10.47) at which the gain becomes 1, it can be considered a bandwidth, since the frequency band from 0 Hz to the unity-gain frequency is also a bandwidth. One could therefore refer to the point at which the gain reduces to 1 as the unity-gain frequency (f_1) or unity-gain bandwidth (B_1).

Another frequency of interest, as shown in Fig. 10.47, is that at which the gain drops by 3 dB (or to 0.707 the dc gain, A_{VD}), this being the cutoff frequency of the op-amp, f_C. In fact, the unity-gain frequency and cutoff frequency are related by

$$\boxed{f_1 = A_{VD}f_C} \qquad \textbf{(10.22)}$$

Equation (10.22) shows that the unity-gain frequency may also be called the gain–bandwidth product of the op-amp.

EXAMPLE 10.12 Determine the cutoff frequency of an op-amp having specified values $B_1 = \mathbf{1\text{ MHz}}$ and $A_{VD} = 200$ V/mV.


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Solution: Since $f_1 = B_1 = 1$ MHz, we can use Eq. (10.22) to calculate

$$f_C = \frac{f_1}{A_{VD}} = \frac{1\text{ MHz}}{200\text{ V/mV}} = \frac{1 \times 10^6}{200 \times 10^3} = \mathbf{5\text{ Hz}}$$

Slew Rate (SR)

Another parameter reflecting the op-amp's ability to handle varying signals is the slew rate, defined as

Slew rate = maximum rate at which amplifier output can change in volts per microsecond (V/μs)

$$\boxed{\text{SR} = \frac{\Delta V_o}{\Delta t}\ \text{V}/\mu\text{s}} \quad \text{with } t \text{ in } \mu\text{s} \qquad \textbf{(10.23)}$$

The slew rate provides a parameter specifying the maximum rate of change of the output voltage when driven by a large step-input signal.* If one tried to drive the output at a

*The closed-loop gain is that obtained with the output connected back to the input in some way.

rate of voltage change greater than the slew rate, the output would not be able to change fast enough and would not vary over the full range expected, resulting in signal clipping or distortion. In any case, the output would not be an amplified duplicate of the input signal if the op-amp slew rate were to be exceeded.

EXAMPLE 10.13 For an op-amp having a slew rate of SR $= 2\ \text{V}/\mu\text{s}$, what is the maximum closed-loop voltage gain that can be used when the input signal varies by 0.5 V in 10 μs?

Solution: Since $V_o = A_{\text{CL}}V_i$, we can use

$$\frac{\Delta V_o}{\Delta t} = A_{\text{CL}}\frac{\Delta V_i}{\Delta t}$$

from which we get

$$A_{\text{CL}} = \frac{\Delta V_o/\Delta t}{\Delta V_i/\Delta t} = \frac{\text{SR}}{\Delta V_i/\Delta t} = \frac{2\ \text{V}/\mu\text{s}}{0.5\ \text{V}/10\ \mu\text{s}} = \mathbf{40}$$

Any closed-loop voltage gain of magnitude greater than 40 would drive the output at a rate greater than the slew rate allows, so the maximum closed-loop gain is 40.

Maximum Signal Frequency

The maximum frequency at which an op-amp may operate depends on both the bandwidth (BW) and slew rate (SR) parameters of the op-amp. For a sinusoidal signal of general form

$$v_o = K\sin(2\pi ft)$$

the maximum voltage rate of change can be shown to be

$$\text{signal maximum rate of change} = 2\pi fK \qquad \text{V/s}$$

To prevent distortion at the output, the rate of change must also be less than the slew rate, that is,

$$2\pi fK \le \text{SR}$$
$$\omega K \le \text{SR}$$

so that

$$\boxed{f \le \frac{\text{SR}}{2\pi K} \quad \text{Hz} \qquad \omega \le \frac{\text{SR}}{K} \quad \text{rad/s}} \tag{10.24}$$

Additionally, the maximum frequency f in Eq. (10.24) is also limited by the unity-gain bandwidth.

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EXAMPLE 10.14 For the signal and circuit of Fig. 10.48, determine the maximum frequency that may be used. Op-amp slew rate is SR $= 0.5\ \text{V}/\mu\text{s}$.

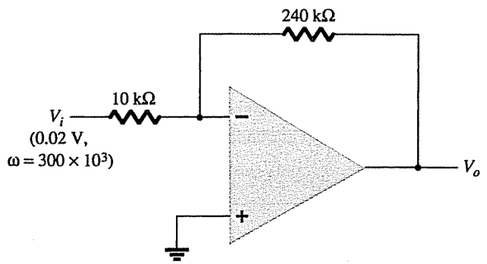


FIG. 10.48
Op-amp circuit for Example 10.14.

Solution: For a gain of magnitude

$$A_{\text{CL}} = \left|\frac{R_f}{R_1}\right| = \frac{240\ \text{k}\Omega}{10\ \text{k}\Omega} = 24$$

the output voltage provides

$$K = A_{\text{CL}}V_i = 24(0.02\ \text{V}) = 0.48\ \text{V}$$

$$\text{Eq. (10.24):}\ \omega \le \frac{\text{SR}}{K} = \frac{0.5\ \text{V}/\mu\text{s}}{0.48\ \text{V}} = \mathbf{1.1 \times 10^6\ rad/s}$$

Since the signal frequency $\omega = 300 \times 10^3$ rad/s is less than the maximum value determined above, no output distortion will result.

10.8 OP-AMP UNIT SPECIFICATIONS

In this section, we discuss how the manufacturer's specifications are read for a typical op-amp unit. A popular bipolar op-amp IC is the 741, described by the information provided in Fig. 10.49. The op-amp is available in a number of packages, an 8-pin DIP and a 10-pin flatpack being among the more usual forms.

Absolute Maximum Ratings

The absolute maximum ratings provide information on what largest voltage supplies may be used, how large the input signal swing may be, and at how much power the device is capable of operating. Depending on the particular version of 741 used, the largest supply voltage is a dual supply of ±18 V or ±22 V. In addition, the IC can internally dissipate from 310 mW to 570 mW, depending on the IC package used. Table 10.2 summarizes some typical values to use in examples and problems.

TABLE 10.2
Absolute Maximum Ratings

Supply voltage	±22 V
Internal power dissipation	500 mW
Differential input voltage	±30 V
Input voltage	±15 V

EXAMPLE 10.15 Determine the current draw from a dual power supply of ±12 V if the IC dissipates 500 mW.

Solution: If we assume that each supply provides half the total power to the IC, then

$$P = VI$$
$$250\ \text{mW} = 12\ \text{V}(I)$$

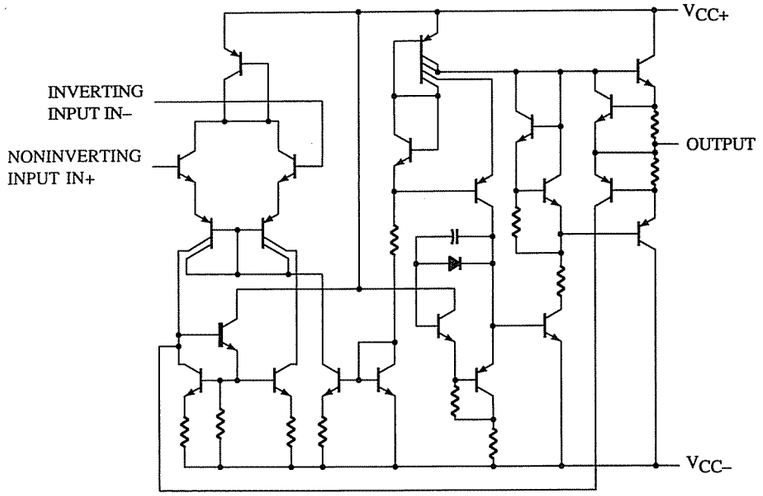
so that each supply must provide a current of

$$I = \frac{250\ \text{mW}}{12\ \text{V}} = \mathbf{20.83\ mA}$$

Electrical Characteristics

Electrical characteristics include many of the parameters covered earlier in this chapter. The manufacturer provides some combination of typical, minimum, or maximum values for various parameters as deemed most useful. A summary is provided in Table 10.3.

V_{IO} Input offset voltage: The input offset voltage is seen to be typically 1 mV, but can go as high as 6 mV. The output offset voltage is then computed based on the circuit used. If the worst condition possible is of interest, the maximum value should be used. Typical values are those more commonly expected when using the op-amp.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		uA741M	uA741C	UNIT
Supply voltage V_{CC+} (see Note 1)		22	18	V
Supply voltage V_{CC-} (see Note 1)		– 22	– 18	V
Differential input voltage (see Note 2)		± 30	± 30	V
Input voltage any input (see Notes 1 and 3)		± 15	± 15	V
Voltage between either offset null terminal (N1/N2) and V_{CC-}		± 0.5	± 0.5	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 5)		500	500	mW
Operating free-air temperature range		– 55 to 125	0 to 70	°C
Storage temperature range		– 65 to 150	– 65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	FH, FK, J, JG, or U package	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D, N, or P package		260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either power supply. For the uA741M only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.
5. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2. In the J and JG packages, uA741M chips are alloy mounted; uA741C chips are glass mounted.

FIG. 10.49
741 op-amp specifications.

I_{IO} Input offset current: The input offset current is listed to be typically 20 nA, whereas the largest value expected is 200 nA.

I_{IB} Input bias current: The input bias current is typically 80 nA and may be as large as 500 nA.

V_{ICR} Common-mode input voltage range: This parameter lists the range over which the input voltage may vary (using a supply of ±15 V), about ±12 V to ±13 V. Inputs larger in amplitude than this value will probably result in output distortion and should be avoided.

V_{OM} Maximum peak output voltage swing: This parameter lists the largest amount the output may vary (using a ±15-V supply). Depending on the circuit closed-loop gain, the input signal should be limited to keep the output from varying by an amount no larger than ±12 V in the worst case, or by ±14 V typically.

electrical characteristics at specified free-air temperature, V_{CC+} = 15 V, V_{CC-} = – 15 V

PARAMETER		TEST CONDITIONS †		uA741M MIN	uA741M TYP	uA741M MAX	uA741C MIN	uA741C TYP	uA741C MAX	UNIT
V_{IO}	Input offset voltage	V_O = 0	25°C		1	5		1	6	mV
			Full range			6			7.5	
$\Delta V_{IO(adj)}$	Offset voltage adjust range	V_O = 0	25°C		± 15			± 15		mV
I_{IO}	Input offset current	V_O = 0	25°C		20	200		20	200	nA
			Full range			500			300	
I_{IB}	Input bias current	V_O = 0	25°C		80	500		80	500	nA
			Full range			1500			800	
V_{ICR}	Common-mode input voltage range		25°C	± 12	± 13		± 12	± 13		V
			Full range	± 12			± 12			
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	25°C	± 12	± 14		± 12	± 14		V
		R_L ≥ 10 kΩ	Full range	± 12			± 12			
		R_L = 2 kΩ	25°C	± 10	± 13		± 10	± 13		
		R_L ≥ 2 kΩ	Full range	± 10			± 10			
A_{VD}	Large-signal differential voltage amplification	R_L ≥ 2 kΩ	25°C	50	200		20	200		V/mV
		V_O = ± 10 V	Full range	25			15			
r_i	Input resistance		25°C	0.3	2		0.3	2		MΩ
r_o	Output resistance	V_O = 0 See note 6	25°C		75			75		Ω
C_i	Input capacitance		25°C		1.4			1.4		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR\,min}$	25°C	70	90		70	90		dB
			Full range	70			70			
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	V_{CC} = ± 9 V to ± 15 V	25°C		30	150		30	150	μV/V
			Full range			150			150	
I_{OS}	Short-circuit output current		25°C		± 25	± 40		± 25	± 40	mA
I_{CC}	Supply current	No load, V_O = 0	25°C		1.7	2.8		1.7	2.8	mA
			Full range			3.3			3.3	
P_D	Total power dissipation	No load, V_O = 0	25°C		50	85		50	85	mW
			Full range			100			100	

operating characteristics, V_{CC+} = 15 V, V_{CC-} = – 15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	uA741M MIN	uA741M TYP	uA741M MAX	uA741C MIN	uA741C TYP	uA741C MAX	UNIT
t_r	Rise time	V_I = 20 mV, R_L = 2 kΩ,		0.3			0.3		μs
	Overshoot factor	C_L = 100 pF, See Figure 1		5%			5%		
SR	Slew rate at unity gain	V_I = 10 V, R_L = 2 kΩ, C_L = 100 pF, See Figure 1		0.5			0.5		V/μs

FIG. 10.49
Continued.

A_{VD} Large-signal differential voltage amplification: This is the open-loop voltage gain of the op-amp. Although a minimum value of 20 V/mV, or 20,000 V/V is listed, the manufacturer also lists a typical value of 200 V/mV, or 200,000 V/V.

r_i Input resistance: The input resistance of the op-amp when measured under open-loop conditions is typically 2 MΩ, but could be as little as 0.3 MΩ or 300 kΩ. In a closed-loop circuit, this input impedance can be much larger, as discussed previously.

r_o Output resistance: The op-amp output resistance is listed as typically 75 Ω. No minimum or maximum value is given by the manufacturer for this op-amp. Again,

TABLE 10.3
μA741 Electrical Characteristics: V_{CC} = ±15 V, T_A = 25°C

Characteristic	Minimum	Typical	Maximum	Unit
V_{IO} Input offset voltage		1	6	mV
I_{IO} Input offset current		20	200	nA
I_{IB} Input bias current		80	500	nA
V_{ICR} Common-mode input voltage range	±12	±13		V
V_{OM} Maximum peak output voltage swing	±12	±14		V
A_{VD} Large-signal differential voltage amplification	20	200		V/mV
r_i Input resistance	0.3	2		MΩ
r_o Output resistance		75		Ω
C_i Input capacitance		1.4		pF
CMRR Common-mode rejection ratio	70	90		dB
I_{CC} Supply current		1.7	2.8	mA
P_D Total power dissipation		50	85	mW

in a closed-loop circuit, the output impedance can be lower, depending on the circuit gain.

C_i **Input capacitance:** For high-frequency considerations, it is helpful to know that the input to the op-amp has typically 1.4 pF of capacitance, a generally small value compared even to stray wiring.

CMRR Common-mode rejection ratio: This parameter is seen to be typically 90 dB, but could go as low as 70 dB. Since 90dB is equivalent to 31,622.78, the op-amp amplifies noise (common inputs) by over 30,000 times less than difference inputs.

I_{CC} **Supply current:** The op-amp draws a total of 2.8 mA, typically from the dual voltage supply, but the current drawn could be as little as 1.7 mA. This parameter helps the user determine the size of the voltage supply to use. It also can be used to calculate the power dissipated by the IC ($P_D = 2V_{CC}I_{CC}$).

P_D **Total power dissipation:** The total power dissipated by the op-amp is typically 50 mW but could go as high as 85 mW. Referring to the previous parameter, we see that the op-amp will dissipate about 50 mW when drawing about 1.7 mA using a dual 15-V supply. At smaller supply voltages, the current drawn will be less and the total power dissipated will also be less.

EXAMPLE 10.16 Using the specifications listed in Table 10.3, calculate the typical output offset voltage for the circuit connection of Fig. 10.50.

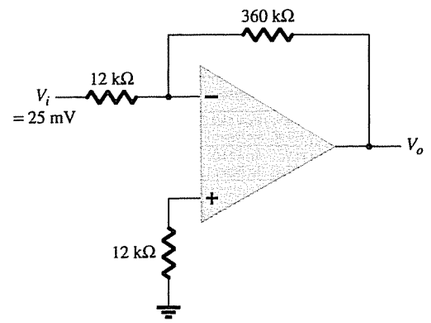


FIG. 10.50
Op-amp circuit for Examples 10.16, 10.17, and 10.19.

Solution: The output offset due to V_{IO} is calculated to be

$$\text{Eq. (10.16):} \quad V_o(\text{offset}) = V_{IO}\frac{R_1 + R_f}{R_1} = (1\,\text{mV})\left(\frac{12\,\text{k}\Omega + 360\,\text{k}\Omega}{12\,\text{k}\Omega}\right) = 31\,\text{mV}$$

The output voltage due to I_{IO} is calculated to be

$$\text{Eq. (10.18):} \quad V_o(\text{offset}) = I_{IO}R_f = 20\,\text{nA}(360\,\text{k}\Omega) = 7.2\,\text{mV}$$

Assuming that these two offsets are the same polarity at the output, we obtain for the total output offset voltage

$$V_o(\text{offset}) = 31\,\text{mV} + 7.2\,\text{mV} = \mathbf{38.2\,mV}$$

EXAMPLE 10.17 For the typical characteristics of the 741 op-amp ($r_o = 75\,\Omega, A = 200\,\text{k}\Omega$), calculate the following values for the circuit of Fig. 10.50:

a. A_{CL}.
b. Z_i.
c. Z_o.

Solution:

a. Eq. (10.8): $\dfrac{V_o}{V_i} = -\dfrac{R_f}{R_1} = -\dfrac{360\,\text{k}\Omega}{12\,\text{k}\Omega} = \mathbf{-30} \cong \dfrac{1}{\beta}$

b. $Z_i = R_1 = \mathbf{12\,k\Omega}$

c. $Z_o = \dfrac{r_o}{(1 + \beta A)} = \dfrac{75\,\Omega}{1 + \left(\dfrac{1}{30}\right)(200\,\text{k}\Omega)} = \mathbf{0.011\,\Omega}$

Operating Characteristics

Another group of values used to describe the operation of the op-amp over varying signals is provided in Table 10.4.

TABLE 10.4
Operating Characteristics: $V_{CC} = \pm 15\,V, T_A = 25°C$

Parameter	Minimum	Typical	Maximum	Unit
B_1 Unity gain bandwidth		1		MHz
t_r Rise time		0.3		μs

EXAMPLE 10.18 Calculate the cutoff frequency of an op-amp having characteristics given in Tables 10.3 and 10.4.

Solution:

$$\text{Eq. (10.22):} \quad f_C = \frac{f_1}{A_{VD}} = \frac{B_1}{A_{VD}} = \frac{1\,\text{MHz}}{20{,}000} = \mathbf{50\,Hz}$$

EXAMPLE 10.19 Calculate the maximum frequency of the input signal for the circuit in Fig. 10.50 with an input of $V_i = 25\,\text{mV}$.

Solution: For a closed-loop gain of $A_{CL} = 30$ and an input of $V_i = 25\,\text{mV}$, the output gain factor is calculated to be

$$K = A_{CL}V_i = 30(25\,\text{mV}) = 750\,\text{mV} = 0.750\,\text{V}$$

Using Eq. (10.24), we obtain the maximum signal frequency f_{max} as

$$f_{max} = \frac{SR}{2\pi K} = \frac{0.5\,\text{V}/\mu\text{s}}{2\pi(0.750\,\text{V})} = \mathbf{106\,kHz}$$

Op-amp Performance

The manufacturer provides a number of graphical descriptions to describe the performance of the op-amp. Figure 10.51 includes some typical performance curves comparing various characteristics as a function of supply voltage. The open-loop voltage gain is seen to get larger with a larger supply voltage value. Whereas the previous tabular information provided information at a particular supply voltage, the performance curve shows how the voltage gain is affected by using a range of supply voltage values.

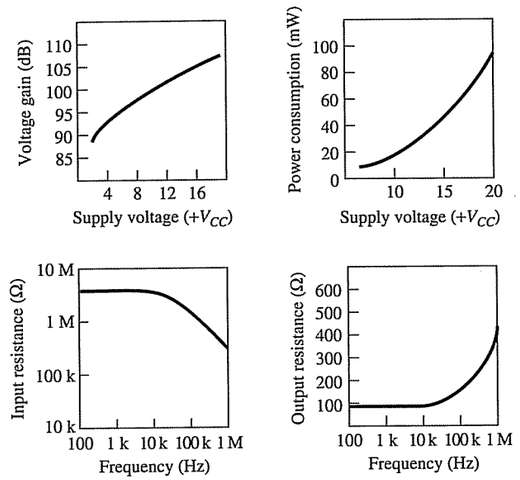


FIG. 10.51
Performance curves.

EXAMPLE 10.20 Using Fig. 10.51, determine the open-loop voltage gain for a supply voltage of $V_{CC} = \pm 12$ V.

Solution: From the curve in Fig. 10.51, $A_{VD} \approx 104$ dB. This is a linear voltage gain of

$$A_{VD}\,(\text{dB}) = 20 \log_{10} A_{VD}$$
$$104 \text{ dB} = 20 \log A_{VD}$$
$$A_{VD} = \text{antilog}\frac{104}{20} = \mathbf{158.5 \times 10^3}$$

Another performance curve in Fig. 10.51 shows how power consumption varies as a function of supply voltage. As shown, the power consumption increases with larger values of supply voltage. For example, whereas the power dissipation is about 50 mW at $V_{CC} = \pm 15$ V, it drops to about 5 mW with $V_{CC} = \pm 5$ V. Two other curves show how the input and output resistances are affected by frequency: The input impedance drops and the output resistance increases at higher frequency.

10.9 DIFFERENTIAL AND COMMON-MODE OPERATION

One of the more important features of a differential circuit connection, as provided in an op-amp, is the circuit's ability to greatly amplify signals that are opposite at the two inputs while only slightly amplifying signals that are common to both inputs. An op-amp provides an output component that is due to the amplification of the difference of the signals applied to the plus and minus inputs and a component due to the signals common to both inputs. Since amplification of the opposite input signals is much greater than that of the common input signals, the circuit provides a common-mode rejection as described by a numerical value called the common-mode rejection ratio (CMRR).

Differential Inputs

When separate inputs are applied to the op-amp, the resulting difference signal is the difference between the two inputs.

$$\boxed{V_d = V_{i_1} - V_{i_2}} \qquad \textbf{(10.25)}$$

Common Inputs

When both input signals are the same, a common signal element due to the two inputs can be defined as the average of the sum of the two signals.

$$\boxed{V_c = \tfrac{1}{2}(V_{i_1} + V_{i_2})} \qquad \textbf{(10.26)}$$

Output Voltage

Since any signals applied to an op-amp in general have both in-phase and out-of-phase components, the resulting output can be expressed as

$$\boxed{V_o = A_d V_d + A_c V_c} \qquad \textbf{(10.27)}$$

where V_d = difference voltage given by Eq. (10.25)
V_c = common voltage given by Eq. (10.26)
A_d = differential gain of the amplifier
A_c = common-mode gain of the amplifier

Opposite-Polarity Inputs

If opposite-polarity inputs applied to an op-amp are ideally opposite signals, $V_{i_1} = -V_{i_2} = V_s$, the resulting difference voltage is

$$\text{Eq. (10.25):} \quad V_d = V_{i_1} - V_{i_2} = V_s - (-V_s) = 2V_s$$

and the resulting common voltage is

$$\text{Eq. (10.26):} \quad V_c = \tfrac{1}{2}(V_{i_1} + V_{i_2}) = \tfrac{1}{2}[V_s + (-V_s)] = 0$$

so that the resulting output voltage is

$$\text{Eq. (10.27):} \quad V_o = A_d V_d + A_c V_c = A_d(2V_s) + 0 = 2A_d V_s$$

This shows that when the inputs are an ideal opposite signal (no common element), the output is the differential gain times twice the input signal applied to one of the inputs.

Same-Polarity Inputs

If the same-polarity inputs are applied to an op-amp, $V_{i_1} = V_{i_2} = V_s$, the resulting difference voltage is

$$\text{Eq. (10.25):} \quad V_d = V_{i_1} - V_{i_2} = V_s - V_s = 0$$

and the resulting common voltage is

$$\text{Eq. (10.26):} \quad V_c = \tfrac{1}{2}(V_{i_1} + V_{i_2}) = \tfrac{1}{2}(V_s + V_s) = V_s$$

so that the resulting output voltage is

$$\text{Eq. (10.27):} \quad V_o = A_d V_d + A_c V_c = A_d(0) + A_c V_s = A_c V_s$$

This shows that when the inputs are ideal in-phase signals (no difference signal), the output is the common-mode gain times the input signal V_s, which shows that only common-mode operation occurs.

Common-Mode Rejection

The solutions above provide the relationships that can be used to measure A_d and A_c in op-amp circuits.

1. *To measure A_d:* Set $V_{i_1} = -V_{i_2} = V_s = 0.5$ V, so that

$$\text{Eq. (10.25):} \quad V_d = (V_{i_1} - V_{i_2}) = (0.5\text{ V} - (-0.5\text{ V}) = 1\text{ V}$$

and

$$\text{Eq. (10.26):} \quad V_c = \tfrac{1}{2}(V_{i_1} + V_{i_2}) = \tfrac{1}{2}[0.5\text{ V} + (-0.5\text{ V})] = 0\text{ V}$$

Under these conditions the output voltage is

$$\text{Eq. (10.27):} \quad V_o = A_d V_d + A_c V_c = A_d(1\text{ V}) + A_c(0) = A_d$$

Thus, setting the input voltages $V_{i_1} = -V_{i_2} = 0.5\,\text{V}$ results in an output voltage numerically equal to the value of A_d.

2. *To measure* A_c: Set $V_{i_1} = V_{i_2} = V_s = 1\,\text{V}$, so that

$$\text{Eq. (10.25):} \quad V_d = (V_{i_1} - V_{i_2}) = (1\,\text{V} - 1\,\text{V}) = 0\,\text{V}$$

and $$\text{Eq. (10.26):} \quad V_c = \tfrac{1}{2}(V_{i_1} + V_{i_2}) = \tfrac{1}{2}(1\,\text{V} + 1\,\text{V}) = 1\,\text{V}$$

Under these conditions the output voltage is

$$\text{Eq. (10.27):} \quad V_o = A_d V_d + A_c V_c = A_d(0\,\text{V}) + A_c(1\,\text{V}) = A_c$$

Thus, setting the input voltages $V_{i_1} = V_{i_2} = 1\,\text{V}$ results in an output voltage numerically equal to the value of A_c.

Common-Mode Rejection Ratio

Having obtained A_d and A_c (as in the measurement procedure discussed above), we can now calculate a value for the common-mode rejection ratio (CMRR), which is defined by the following equation:

$$\boxed{\text{CMRR} = \frac{A_d}{A_c}} \tag{10.27}$$

The value of CMRR can also be expressed in logarithmic terms as

$$\boxed{\text{CMRR (log)} = 20\log_{10}\frac{A_d}{A_c}} \quad \text{(dB)} \tag{10.28}$$

EXAMPLE 10.21 Calculate the CMRR for the circuit measurements shown in Fig. 10.52..

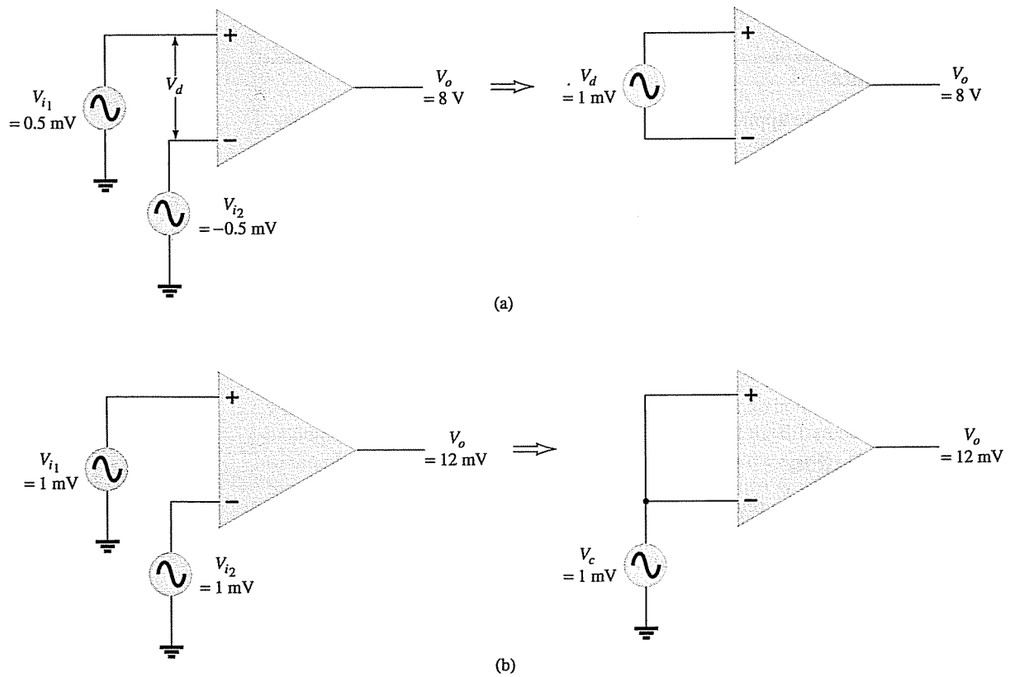


FIG. 10.52
(a) Differential and (b) common-mode operation.

Solution: From the measurement shown in Fig. 10.52a, using the procedure in step 1 above, we obtain

$$A_d = \frac{V_o}{V_d} = \frac{8\,\text{V}}{1\,\text{mV}} = 8000$$

The measurement shown in Fig. 10.52b, using the procedure in step 2 above, gives us

$$A_c = \frac{V_o}{V_c} = \frac{12\,\text{mV}}{1\,\text{mV}} = 12$$

Using Eq. (10.28), we obtain the value of CMRR,

$$\text{CMRR} = \frac{A_d}{A_c} = \frac{8000}{12} = \mathbf{666.7}$$

which can also be expressed as

$$\text{CMRR} = 20\log_{10}\frac{A_d}{A_c} = 20\log_{10}666.7 = \mathbf{56.48\,dB}$$

It should be clear that the desired operation will have A_d very large with A_c very small. That is, the signal components of opposite polarity will appear greatly amplified at the output, whereas the signal components that are in phase will mostly cancel out so that the common-mode gain A_c is very small. Ideally, the value of the CMRR is infinite. Practically, the larger the value of CMRR, the better is the circuit operation.

We can express the output voltage in terms of the value of CMRR as follows:

$$\text{Eq. (12.22):} \quad V_o = A_d V_d + A_c V_c = A_d V_d\left(1 + \frac{A_c V_c}{A_d V_d}\right)$$

Using Eq. (12.24), we can write the above as

$$\boxed{V_o = A_d V_d\left(1 + \frac{1}{\text{CMRR}}\frac{V_c}{V_d}\right)} \tag{10.29}$$

Even when both V_d and V_c components of signal are present, Eq. (10.29) shows that for large values of CMRR, the output voltage will be due mostly to the difference signal, with the common-mode component greatly reduced or rejected. Some practical examples should help clarify this idea.

EXAMPLE 10.22 Determine the output voltage of an op-amp for input voltages of $V_{i_1} = 150\,\mu\text{V}$ and $V_{i_2} = 140\,\mu\text{V}$. The amplifier has a differential gain of $A_d = 4000$ and the value of CMRR is:

a. 100.
b. 10^5.

Solution:

$$\text{Eq. (10.25):} \quad V_d = V_{i_1} - V_{i_2} = (150 - 140)\,\mu\text{V} = 10\,\mu\text{V}$$

$$\text{Eq. (10.26):} \quad V_c = \frac{1}{2}(V_{i_1} + V_{i_2}) = \frac{150\,\mu\text{V} + 140\,\mu\text{V}}{2} = 145\,\mu\text{V}$$

a.
$$\text{Eq. (10.29):} \quad V_o = A_d V_d\left(1 + \frac{1}{\text{CMRR}}\frac{V_c}{V_d}\right)$$
$$= (4000)(10\,\mu\text{V})\left(1 + \frac{1}{100}\frac{145\,\mu\text{V}}{10\,\mu\text{V}}\right)$$
$$= 40\,\text{mV}(1.145) = \mathbf{45.8\,mV}$$

b. $V_o = (4000)(10\,\mu\text{V})\left(1 + \frac{1}{10^5}\frac{145\,\mu\text{V}}{10\,\mu\text{V}}\right) = 40\,\text{mV}(1.000145) = \mathbf{40.006\,mV}$

Example 10.22 shows that the larger the value of CMRR, the closer is the output voltage to the difference input times the difference gain with the common-mode signal being rejected.

10.10 SUMMARY

Important Conclusions and Concepts

1. Differential operation involves the use of opposite-polarity inputs.
2. Common-mode operation involves the use of the same-polarity inputs.
3. Common-mode rejection compares the gain for differential inputs to that for common inputs.
4. An op-amp is an **op**erational **amp**lifier.
5. The basic features of an op-amp are:
   Very high input impedance (typically megohms)
   Very high voltage gain (typically a few hundred thousand and greater)
   Low output impedance (typically less than 100 Ω)
6. Virtual ground is a concept based on the practical fact that the differential input voltage between plus (+) and minus (−) inputs is nearly (virtually) zero volts—when calculated as the output voltage (at most, that of the voltage supply) divided by the very high voltage gain of the op-amp.
7. Basic op-amp connections include:
   Inverting amplifier
   Noninverting amplifier
   Unity-gain amplifier
   Summing amplifier
   Integrator amplifier
8. Op-amp specs include:
   Offset voltages and currents
   Frequency parameters
   Gain–bandwidth
   Slew rate

Equations

$$\text{CMRR} = 20 \log_{10} \frac{A_d}{A_c}$$

Inverting amplifier:

$$\frac{V_o}{V_i} = -\frac{R_f}{R_1}$$

Noninverting amplifier:

$$\frac{V_o}{V_i} = 1 + \frac{R_f}{R_1}$$

Unity follower:

$$V_o = V_1$$

Summing amplifier:

$$V_o = -\left(\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3\right)$$

Integrator amplifier:

$$v_o(t) = -\frac{1}{RC} \int v_1(t)\, dt$$

$$\text{Slew rate (SR)} = \frac{\Delta V_o}{\Delta t} \qquad \text{V}/\mu\text{s}$$

PSpice Windows

Program 10.1—Inverting Op-Amp An inverting op-amp, shown in Fig. 10.53, is considered first. With the dc voltage display turned on, the result after running an analysis shows that for an input of 2 V and a circuit gain of −5,

$$A_v = -R_F/R_1 = -500\,\text{k}\Omega/100\,\text{k}\Omega = -5$$

The output is exactly −10 V:

$$V_o = A_v V_i = -5(2\,\text{V}) = -10\,\text{V}$$

The input to the minus terminal is −50.01 μV, which is virtually ground, or 0 V.

A practical inverting op-amp circuit is drawn in Fig. 10.54. Using the same resistor values as in Fig. 10.53 with a practical op-amp unit, the μA741, we obtain the resulting output of −9.96 V, near the ideal value of −10 V. This slight difference from the ideal is due to the actual gain and input impedance of the μA741 op-amp unit.

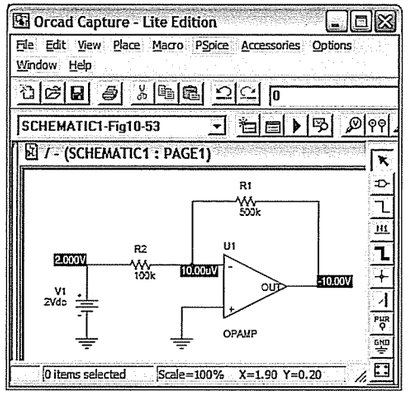


FIG. 10.53
Inverting op-amp using ideal model.

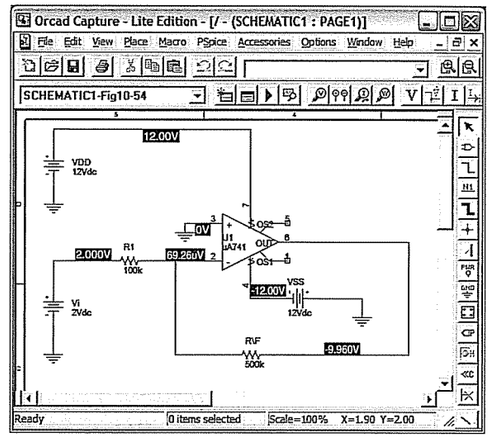


FIG. 10.54
Practical inverting op-amp circuit.

Before the analysis is done, selecting **Analysis Setup, Transfer Function,** and then **Output** of **V(RF:2)** and **Input Source** of V_i will provide the small-signal characteristics in the output listing. The circuit gain is seen to be

$$V_o/V_i = -5$$

Input resistance at $V_i = 1 \times 10^5$

Output resistance at $V_o = 4.95 \times 10^{-3}$

Program 10.2—Noninverting Op-Amp Figure 10.55 shows a noninverting op-amp circuit. The bias voltages are displayed on the figure. The theoretical gain of the amplifier circuit should be

$$A_v = (1 + R_F/R_1) = 1 + 500\,\text{k}\Omega/100\,\text{k}\Omega = 6$$

For an input of 2 V, the resulting output will be

$$V_o = A_v V_i = 5(2\,\text{V}) = 10\,\text{V}$$

The output is noninverted from the input.

Program 10.3—Summing Op-Amp Circuit A summing op-amp circuit such as that in Example 10.3 is shown in Fig. 10.56. Bias voltages also are displayed in Fig. 10.56, showing the resulting output at 3 V, as was calculated in Example 10.3. Notice how well the virtual ground concept works with the minus input being only 3.791 μV.

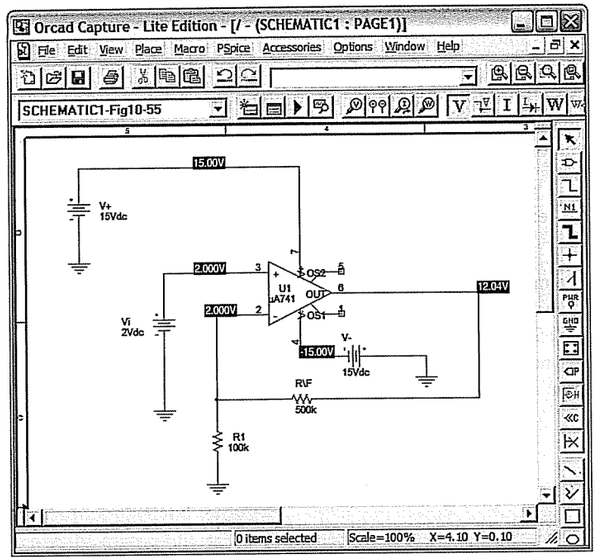


FIG. 10.55
Design Center schematic for noninverting op-amp circuit.

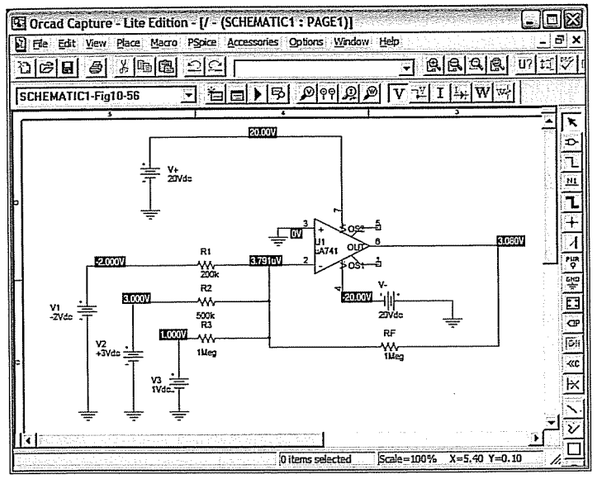


FIG. 10.56
Summing amplifier for Program 10.3.

FIG. 10.57
Unity-gain amplifier.

Program 10.4—Unity-Gain Op-Amp Circuit Figure 10.57 shows a unity-gain op-amp circuit with bias voltages displayed. For an input of +2 V, the output is exactly +2 V.

Program 10.5—Op-Amp Integrator Circuit An op-amp integrator circuit is shown in Fig. 10.58. The input is selected as **VPULSE,** which is set to be a step input as follows: Set **ac** = 0, **dc** = 0, **V1** = 0 V, **V2** = 2 V, **TD** = 0, **TR** = 0, **TF** = 0, **PW** = 10 ms, and **PER** = 20 ms. This provides a step from 0 to 2 V, with no time delay, rise time, or fall time, having a period of 10 ms and repeating after a period of 20 ms. For this problem, the voltage rises instantly to 2 V, then stays there for a sufficiently long time for the output to drop

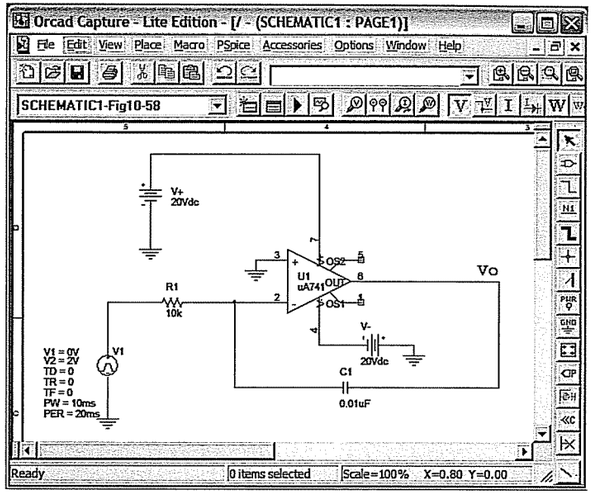


FIG. 10.58
Op-amp integrator circuit.

as a ramp voltage from the maximum supply level of +20 V to the lowest level of −20 V. Theoretically, the output for the circuit of Fig. 10.58 is

$$v_o(t) = -1/RC \int v_i(t)\, dt$$

$$v_o(t) = -1/(10\,\text{k}\Omega)(0.01\,\mu\text{F}) \int 2\, dt = -10{,}000 \int 2\, dt = -20{,}000t$$

This is a negative ramp voltage dropping at a rate (slope) of −20,000 V/s. This ramp voltage will drop from +20 V to −20 V in

$$40\ \text{V}/20{,}000 = 2 \times 10^{-3} = 2\ \text{ms}$$

Figure 10.59 shows the input step waveform and the resulting output ramp waveform obtained using **PROBE.**

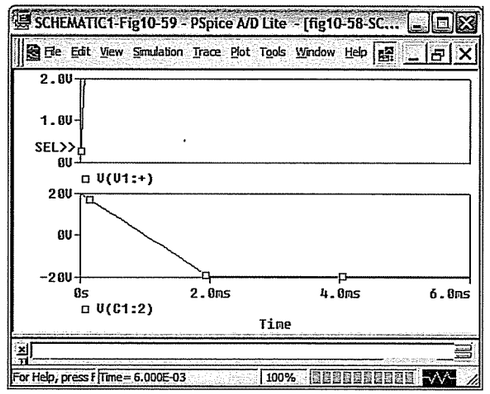
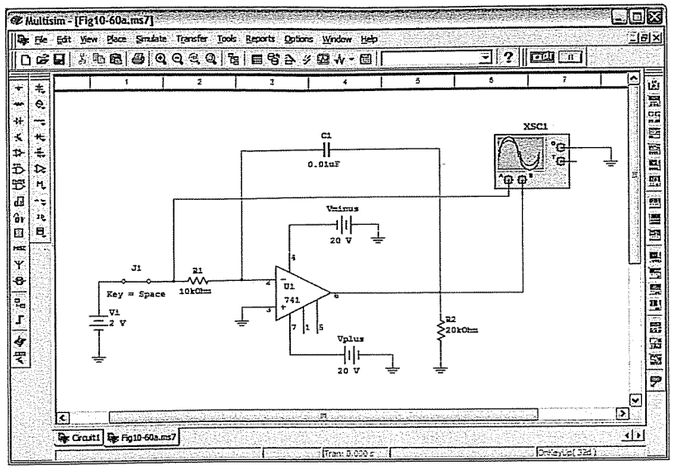


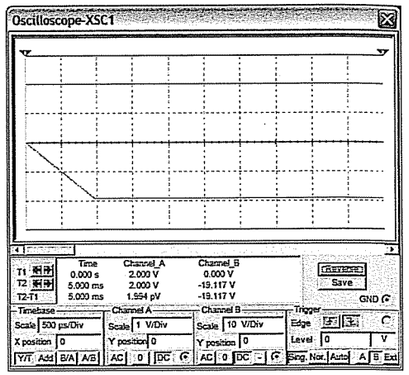
FIG. 10.59
Probe waveform for integrator circuit.

Multisim

The same integrator circuit can be constructed and operated using Multisim. Figure 10.60a shows the integrator circuit built using Multisim, with an oscilloscope connected to the op-amp output. The oscilloscope graph obtained is shown in Fig. 10.60b, the linear output waveform going from +20 V down to −20 V in a period of about 2 ms.



(a)



(b)

FIG. 10.60
Multisim integrator circuit: (a) circuit; (b) waveform.

Program 10.6–Multistage Op-Amp Circuit A multistage op-amp circuit is shown in Fig. 10.61. The input to stage 1 of 200 mV provides an output of 200 mV to stages 2 and 3. Stage 2 is an inverting amplifier with gain $-200\,\text{k}\Omega/20\,\text{k}\Omega = -10$, with an output from stage 2 of $-10(200\,\text{mV}) = -2\,\text{V}$. State 3 is a noninverting amplifier with gain of $(1 + 200\,\text{k}\Omega/10\,\text{k}\Omega = 21)$, resulting in an output of $21(200\,\text{mV}) = 4.2\,\text{V}$.

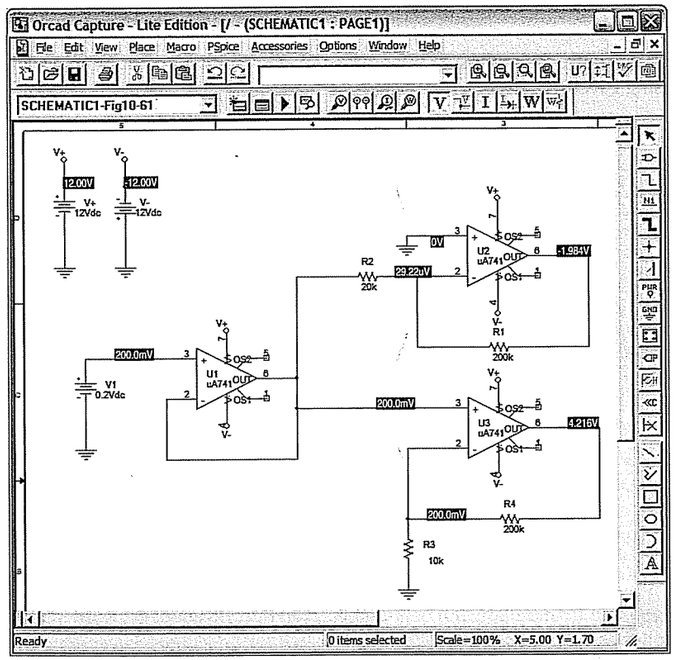


FIG. 10.61
Multistage op-amp circuit.

PROBLEMS

**Note:* Asterisks indicate more difficult problems.

10.5 Practical Op-Amp Circuits

1. What is the output voltage in the circuit of Fig. 10.62.

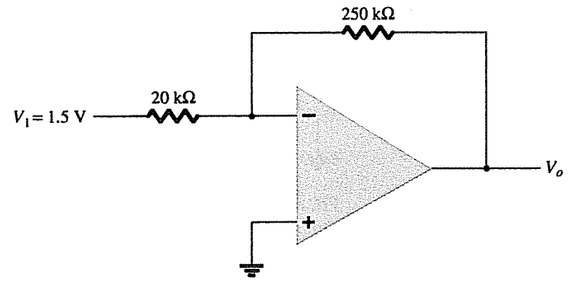


FIG. 10.62
Problems 1 and 23.

2. What is the range of the voltage-gain adjustment in the circuit of Fig. 10.63.

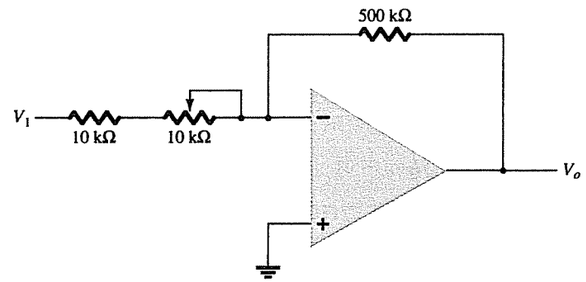


FIG. 10.63
Problem 2.

3. What input voltage results in an output of 2 V in the circuit of Fig. 10.64?

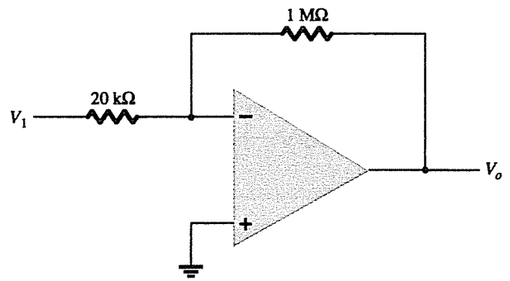


FIG. 10.64
Problem 3.

4. What is the range of the output voltage in the circuit of Fig. 10.65 if the input can vary from 0.1 to 0.5 V?

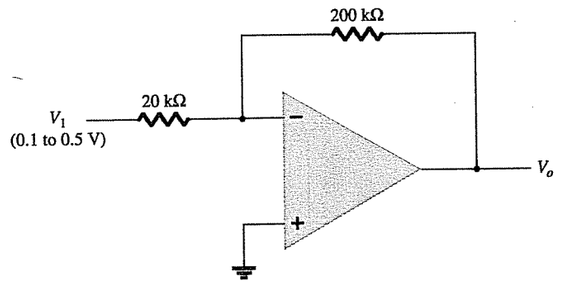


FIG. 10.65
Problem 4.

5. What output voltage results in the circuit of Fig. 10.66 for an input of $V_1 = -0.3$ V?

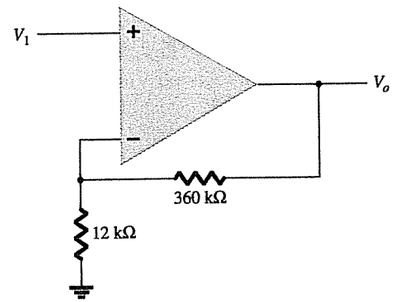


FIG. 10.66
Problems 5, 6, and 24.

6. What input must be applied to the input of Fig. 10.66 to result in an output of 2.4 V?

7. What range of output voltage is developed in the circuit of Fig. 10.67?

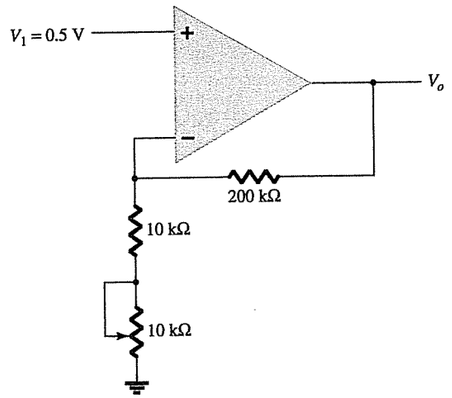


FIG. 10.67
Problem 7.

8. Calculate the output voltage developed by the circuit of Fig. 10.68 for $R_f = 330$ kΩ.

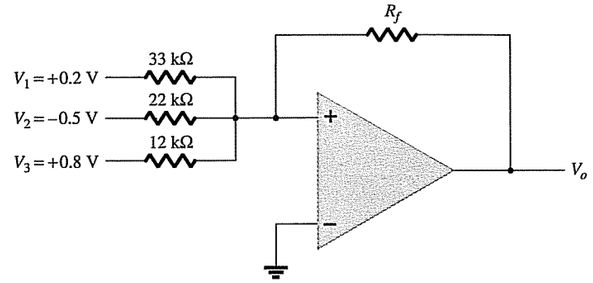


FIG. 10.68
Problems 8, 9, and 25.

9. Calculate the output voltage of the circuit in Fig. 10.68 for $R_f = 68$ kΩ.

10. Sketch the output waveform resulting in Fig. 10.69.

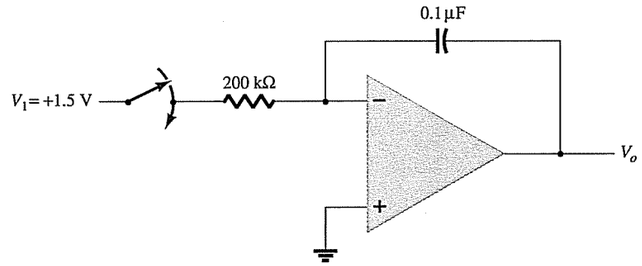


FIG. 10.69
Problem 10.

11. What output voltage results in the circuit of Fig. 10.70 for $V_1 = +0.5$ V?

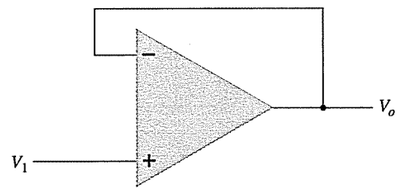


FIG. 10.70
Problem 11.

12. Calculate the output voltage for the circuit of Fig. 10.71.

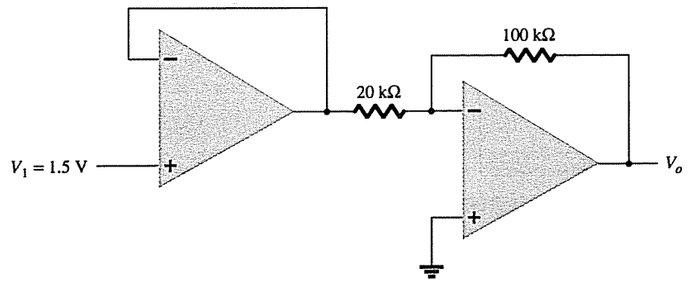


FIG. 10.71
Problems 12 and 26.

13. Calculate the output voltages V_2 and V_3 in the circuit of Fig. 10.72.

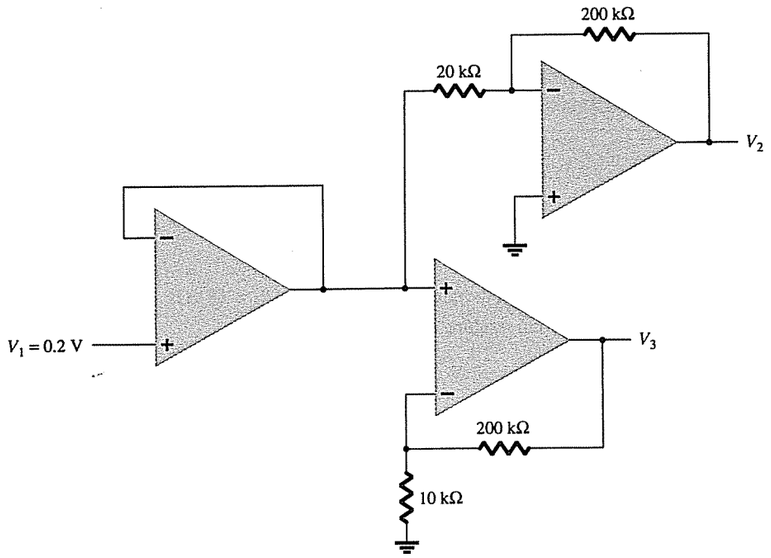


FIG. 10.72
Problem 13.

14. Calculate the output voltage, V_o, in the circuit of Fig. 10.73.

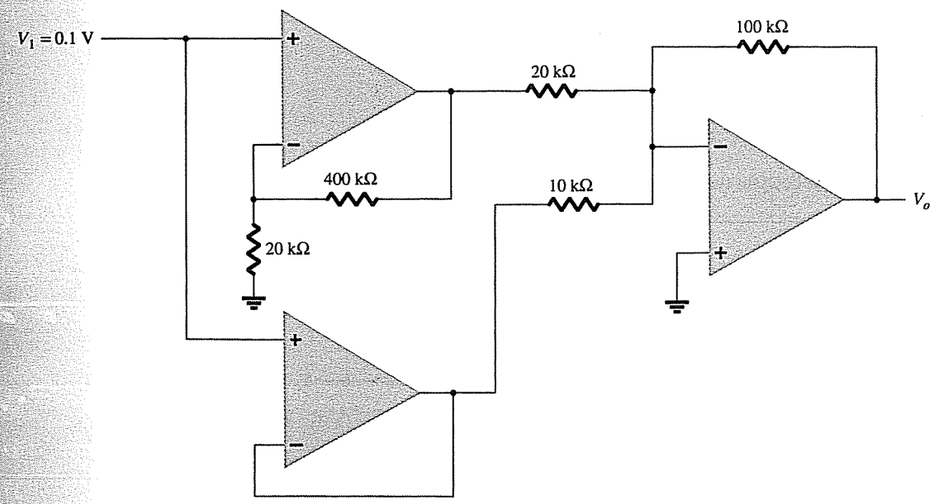


FIG. 10.73
Problems 14 and 27.

15. Calculate V_o in the circuit of Fig. 10.74.

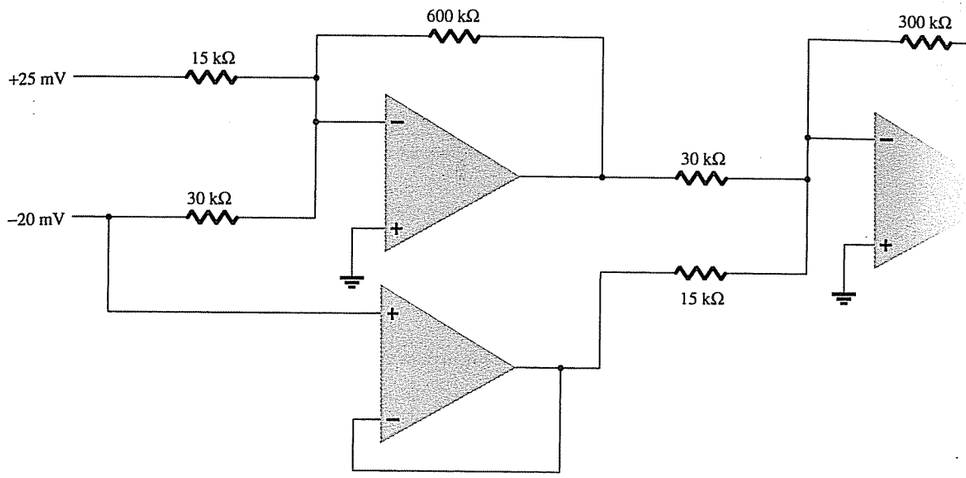


FIG. 10.74
Problem 15.

10.6 Op-Amp Specifications–DC Offset Parameters

***16.** Calculate the total offset voltage for the circuit of Fig. 10.75 for an op-amp with specified values of input offset voltage $V_{IO} = 6$ mV and input offset current $I_{IO} = 120$ nA.

***17.** Calculate the input bias current at each input of an op-amp having specified values of $I_{IO} = 4$ nA and $I_{IB} = 20$ nA.

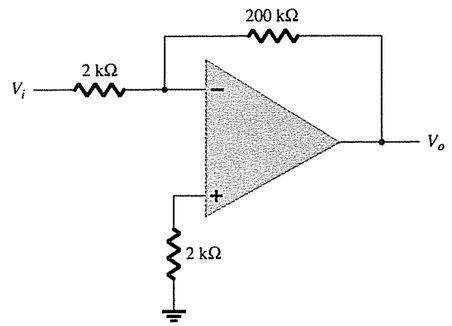


FIG. 10.75
Problems 16, 20, 21, and 22.

10.7 Op-Amp Specifications–Frequency Parameters

18. Determine the cutoff frequency of an op-amp having specified values $B_1 = 800$ kHz and $A_{VD} = 150$ V/mV.

***19.** For an op-amp having a slew rate of SR = 2.4 V/μs, what is the maximum closed-loop voltage gain that can be used when the input signal varies by 0.3 V in 10 μs?

***20.** For an input of $V_1 = 50$ mV in the circuit of Fig. 10.75, determine the maximum frequency that may be used. The op-amp slew rate SR = 0.4 V/μs.

*21. Using the specifications listed in Table 10.3, calculate the typical offset voltage for the circuit connection of Fig. 10.75.

*22. For the typical characteristics of the 741 op-amp, calculate the following values for the circuit of Fig. 10.75:
a. A_{CL}.
b. Z_i.
c. Z_o.

10.9 Differential and Common-Mode Operation

23. Calculate the CMRR (in dB) for the circuit measurements of $V_d = 1\,\text{mV}$, $V_o = 120\,\text{mV}$, and $V_C = 1\,\text{mV}$, $V_o = 20\,\mu\text{V}$.

24. Determine the output voltage of an op-amp for input voltages of $V_{i_1} = 200\,\mu\text{V}$ and $V_{i_2} = 140\,\mu\text{V}$. The amplifier has a differential gain of $A_d = 6000$ and the value of CMRR is:
a. 200.
b. 10^5.

10.11 Computer Analysis

*25. Use Schematic Capture or Multisim to draw a circuit to determine the output voltage in the circuit of Fig. 10.62.

*26. Use Schematic Capture or Multisim to calculate the output voltage in the circuit of Fig. 10.66 for the input of $V_i = 0.5\,\text{V}$.

*27. Use Schematic Capture or Multisim to calculate the output voltage in the circuit of Fig. 10.68 for $R_f = 68\,\text{k}\Omega$.

*28. Use Schematic Capture or Multisim to calculate the output voltage in the circuit of Fig. 10.71.

*29. Use Schematic Capture or Multisim to calculate the output voltage in the circuit of Fig. 10.73.

*30. Use Schematic Capture or Multisim to calculate the output voltage in the circuit of Fig. 10.74.

*31. Use Schematic Capture or Multisim to obtain the output waveform for a 2-V step input to an integrator circuit, as shown in Fig. 10.39 with values of $R = 40\,\text{k}\Omega$ and $C = 0.003\,\mu\text{F}$.

11 Op-Amp Applications

CHAPTER OUTLINE

11.1 Constant-Gain Multiplier
11.2 Voltage Summing
11.3 Voltage Buffer
11.4 Controlled Sources
11.5 Instrumentation Circuits
11.6 Active Filters
11.7 Summary
11.8 Computer Analysis

11.1 CONSTANT-GAIN MULTIPLIER

One of the most common op-amp circuits is the inverting constant-gain multiplier, which provides a precise gain or amplification. Figure 11.1 shows a standard circuit connection, with the resulting gain being given by

$$A = -\frac{R_f}{R_1} \tag{11.1}$$

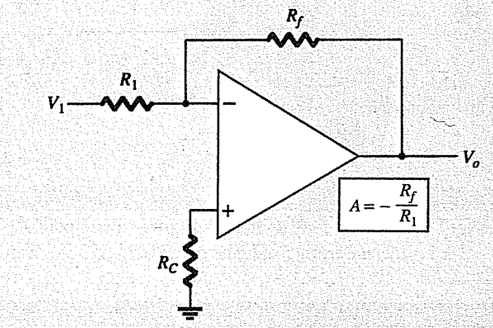


FIG. 11.1
Fixed-gain amplifier.